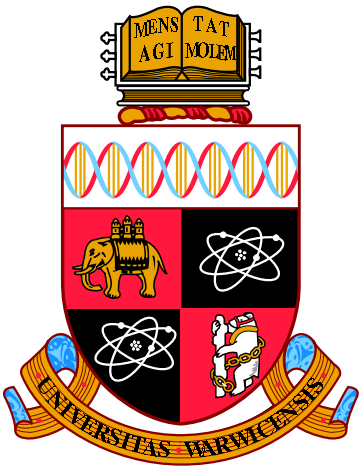

The Characterisation, Modelling and Detection of Series Arc Faults in Aircraft Electrical Power Distribution Systems Featuring Solid State Power Controllers (SSPCs)

by

Peter James Handy

Thesis

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WARWICK

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Declarations

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. The author wishes to declare that with the exception of commonly understood and accepted ideas or where reference is made to the work of others, the work presented in this thesis is his own, and includes nothing which is the outcome of work done in collaboration. This thesis has not been submitted in part, or in whole, to any other university for a degree, diploma or other qualification.

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Peter James Handy
May 2016

To my fiancée Natalie, and also to my parents Jane and John.

Abstract

Electrical power demand in aircraft has grown significantly over the last century, and this trend continues with the More Electric Aircraft (MEA) and All Electric Aircraft (AEA) concepts. Higher voltages such as 270VDC are required to deliver additional power to loads and to optimise aircraft mass. Increased voltages inflict more stress on the Electrical Wiring Interconnect System (EWIS) and increase the impact of series arc faults caused by wiring defects. Solid State Power Controllers (SSPCs) are used to provide fast protection in high voltage distribution systems. The aim of this work is the characterisation, modelling, simulation and detection of series arc faults in 28VDC and 270VDC electrical power distribution systems featuring SSPCs.

The majority of passive detection schemes in the literature were designed based on empirical data rather than well characterised electric arc parameters, and thus nuisance trips are unavoidable. To address this series arc faults in 28VDC and 270VDC solid state power distribution systems were characterised using the SAE5692 "Loose terminal" method [8], and it was found that 270VDC arc faults cause a minimal ∼5.6% reduction in loop current and load voltage compared with ∼54% in 28VDC systems. SSPC output voltage transients caused by series arcs were found to be limited by the presence of SSPC snubbers. Increasing the system loop inductance was found to improve series arc stability resulting in fewer arc quench events. Increasing the capacitive load reduces arc stability and causes arcs to quench more readily thus simplifying detection. These results were later used to experimentally validate a novel series arc fault SPICE model based on the static Nottingham V-I model [9] and wider solid state electrical system model.

The arc current and SSPC output voltage results were also used to create a prototype passive series arc fault detection system, which has been demonstrated to SAE5692 under laboratory conditions [8]. A novel multilayer PCB current sensor was developed and experimentally validated for this prototype.

To further reduce nuisance trips an innovative active arc fault perturbation scheme was simulated and experimentally demonstrated using SSPC modulation to stimulate and detect arc quench. Another novel complementary series arc fault prevention / confirmation scheme was simulated and experimentally validated using SSPC leakage currents. To minimise nuisance trips due to manufacturing and installation errors a unique Built-In Test (BIT) scheme was also developed and experimentally validated using the SSPC to create artificial current and voltage stimuli.

Keywords:
series arc fault, series arc fault detection, solid state power controllers (SSPCs), fault interruption, power system protection, high voltage

Abbreviations

AC	Alternating Current
ADC	Analogue to Digital Converter
AEA	All Electric Aircraft
AEPHM	Aircraft Electrical Power Systems Prognostics and Health Management
AFCB	Arc Fault Circuit Breaker
AFCI	Arc Fault Circuit Interrupters
AFD	Arc Fault Detection
AFRL	Air Force Research Laboratory
AM	Amplitude Modulation
ANN	Artificial Neural Network
ANSI	American National Standards Institute
APEC	Applied Power Electronics Conference (and Exposition)
APL	Applied Physics Laboratory
APPEEC	Asia-Pacific Power and Energy Engineering Conference
APU	Auxiliary Power Unit
ARP	Aerospace Recommended Practice
ASIC	Application Specific Integrated Circuit
ASTM	American Society for Testing and Materials

AWG	American Wire Gauge
BIT	Built-In Test
BP	Back Propagation (Neural Network)
BPL	Broadband over the Power Line
BPNN	Back Propagation Neural Network
CAA	Civil Aviation Authority
CCVS	Current Controlled Voltage Source
CCF	Common Cause Failures
CDF	Cumulative Distribution Function
CF	Constant Frequency
CIGRE	Conseil International des Grands Réseaux Electriques
CIPS	Conference on Integrated Power Electronics Systems
CMD	(International Conference on) Condition Monitoring and Diagnosis
CMOS	Complimentary Metal Oxide Semiconductor
COTS	Commercial Off-The-Shelf
CPE	(Conference-Workshop) Compatibility and Power Electronics
CRC	Chemical Rubber Company (Press)
CSD	Constant Speed Drive
CT	Current Transformer
CW	Continuous Wave
CWT	Continuous Wavelet Transform
DAC	Digital to Analogue Converter
DAL	Design Assurance Level
DC	Direct Current
DFT	Discrete Fourier Transform

DMA Direct Memory Access

DMM Digital Multi Meter

DPSP (Conference on) Developments in Power System Protection

DoD Department of Defense

DWT Discrete Wavelet Transform

EADS European Aeronautic Defence and Space (Company)

EAPAS Enhanced Airworthiness Program for Airplane Systems

EASA European Aviation Safety Agency

eECS electrical Environmental Control System

ECS Environmental Control System

EE Electrical Equipment (as in EE bay)

EHA Electro-Hydrostatic Actuation

ELM Edge-Localized Mode

EMC Electro Magnetic Compatibility

EMF Electromotive Force

EMI Electro Magnetic Interference

EPE European (Conference on) Power Electronics (and Applications)

EPV Electrical Power Variation

ESARS Electrical Systems for Aircraft, Railway and Ship Propulsion

ESD Electrostatic Discharge

ESSCIRC European Solid-State Circuits Conference

ESTC Electronics System(-Integration) Technology Conference

ESTS Electric Ship Technologies Symposium

eWIPS electrical Wing Ice Protection System

EWIS Electrical Wiring Interconnection System

FAA	Federal Aviation Authority
FAR	Federal Aviation Requirements
FDR	Frequency Domain Reflectometry
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FMCW	Frequency Modulated Continuous Wave
FMEA	Failure Mode and Effects Analysis
FMECA	Failure Mode, Effects and Criticality Analysis
FPGA	Field Programmable Gate Array
FQIS	Fuel Quantity Indicating System
FSK	Frequency Shift Keying
FSM	Finite State Machine
GA	Genetic Algorithm
GE	General Electric
GMR	Giant Magnetoresistance
GWIT	Goodrich Wire Integrity Tool
HF	High Frequency
HIF	High Impedance Fault
HiPot	High Potential (Wire Tester)
HR	Human Resources
I2MTC	International Instrumentation and Measurement Technology Conference (Conference)
IAS	Industry Applications Society (Conference)
IBIT	Initiated Built-In Test
ICACC	International Conference on Advanced Computer Control

ICC	International Conference on Communications
ICEC	International Conference on Electrical Contacts
ICEICE	International Conference on Electric Information and Control Engineering
ICIEA	International Conference on Industrial Electronics and Applications
IDG	Integrated Drive Generator
IEE	Institute of Electrical Engineers
IEEE	Institute of Electrical and Electronics Engineers
IET	Institute of Engineering and Technology
IF	Intermediate Frequency
IIR	Infinite Impulse Response
IMTC	(IEEE) Instrumentation and Measurement Technology Conference
IP	Intellectual Property
IPC	Association Connecting Electronics Industries
ISGT	Innovative Smart Grid Technologies
ISIE	International Symposium on Industrial Electronics
ISR	Interrupt Service Routine
ISSPA	International Symposium on Signal Processing and its Applications
ITAR	International Traffic in Arms Regulations
IUPAC	International Union of Pure and Applied Chemistry
IUPEC	International Universities Power Engineering Conference
IWIES	International Workshop on Intelligent Energy Systems
JAR	Joint Aviation Requirements
JSF	Lockheed Martin F-35 Joint Strike Fighter
JTFDR	Joint Time Frequency Domain Reflectometry

kSPS kilo Samples Per Second

LEHV Low Energy High Voltage

LC Inductor-Capacitor (Network)

LR Inductor-Resistor (Network)

LRU Line Replacement Unit

LSB Least Significant Bit

LUT Look-Up Table

MCR Multi-Carrier Reflectometry

MCU Microcontroller Unit

MDL Minimum Description Length

MEA More Electric Aircraft

MET Micro Energy Tool

MLCC Multi Layer Chip Capacitor

MOET More Open Electrical Technologies (Programme)

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MOV Metal Oxide Varistor

MPT Modular Power Tile

MSE Mean Square Error

MSPS Mega Samples Per Second

MSB Most Significant Bit

MTBF Mean Time Between Failure

MTTF Mean Time To Failure

NASA National Aeronautics and Space Administration

NDR Noise Domain Reflectometry

NEC National Electrical Code

NFPA National Fire Protection Association

NTSB National Transportation Safety Board

PAS (IEEE Transactions on) Power Apparatus and Systems

PASD Pulse Arrested Spark Discharge

PCB Printed Circuit Board

PCIC Petroleum and Chemical Industry Conference

PCIM Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management

PDF Probability Density Function

PDFDR Phase Detection Frequency Domain Reflectometry

PEEC Partial Element Equivalent Circuit

PEMC Power Electronics and Motion Control Conference

PEPDC Primary Electrical Power Distribution Centre (Programme)

PEPSC Primary Electrical Power Solid (state power) Controller (Programme)

PES Power Electronics Society

PESC Power Electronics Specialists Conference

PHM Prognostics and Health Management (PHM)

PIC Programmable Interface Controller

PN Pseudo-random Noise

PPE Personal Protective Equipment

PV Photovoltaic

PVSC Photovoltaic Specialists Conference

PWL Piece Wise Linear

PWM Pulse Width Modulation

RC Resistor-Capacitor (Network)

RF Radio Frequency

RL Resistor-Inductor (Network)

RLC Resistor-Inductor-Capacitor (Network)

RMS Root Mean Square

RTCA Radio Technical Commission for Aeronautics

SAE Society of Automotive Engineers

SAS (IEEE) Sensors Applications Symposium

SCB Slow Charge Breakdown

SDR Software Defined Radio

SPICE Simulation Program with Integrated Circuit Emphasis

SPST Single Pole Single Throw

SSEDU Solid State Electrical Distribution Unit (Programme)

SSPC Solid State Power Controller

SSPM Solid State Power Manager

SSTDR Spread Spectrum Time Domain Reflectometry

STDR Sequence Time Domain Reflectometry

STFT Short Time Fourier Transform

SWR Standing Wave Reflectometry

TDR Time Domain Reflectometry

TDV Time Domain Vernier

TFDR Time-Frequency Domain Reflectometry

TID Thermal Ionisation Detector

TRL Technology Readiness Level

TRU Transformer Rectifier Unit

TVS Transient Voltage Suppressor

TWA Trans World Airlines

UAL United Airlines

UCAV Unmanned Combat Air Vehicle

UHF Ultra High Frequency

UK United Kingdom

UL Underwriters Laboratories

US United States (of America)

UV Ultraviolet (Light)

UUT Unit Under Test

VAC Volts AC

VDC Volts DC

VCVS Voltage Controlled Voltage Source

VF Variable Frequency

VHF Very High Frequency

VMC Vehicle Management Computer

VOP Velocity of Propagation

VSCF Variable Speed Constant Frequency

WDD Weights Direct Determination

WIPS Wing Ice Protection System

WVU West Virginia University

Chapter 1

An Introduction to Arc Faults

1.1 A Brief History of Aircraft Electrification

Aircraft electrical power systems have developed significantly over time, beginning with First World War aircraft which derived low voltage DC electrical power from crude assemblies of separate cells bolted together by inter-cell connectors. The first aircraft batteries of any significance emerged in the mid-1930s in the form of 12V 40A-hr, 12V 25A-hr and 12V 15 A-hr batteries which were developed in conjunction with the Royal Academy of Engineering [10, p. 401]. In these early aircraft electrical power was required solely to power the main engine ignition system, however as time progressed there was a greater demand for electrical power as more electrical loads such as lights and instruments were introduced. The increasing demand for electrical power in low voltage DC systems resulted in the need to deliver additional current from the power sources to the loads, which drove the requirement to increase the cross sectional area of the electrical wiring in order to manage resistive power losses and hence wire temperatures. By the 1940s and 1950s twin 28VDC generators were commonplace on twin engine aircraft where one or two 28VDC batteries were also fitted along with an inverter to supply 115VAC to the flight instruments [11]. This increase in voltage to 28VDC and 115VAC resulted in the ability to deliver higher power levels to electrical loads over modest electrical wire gauges.

There was a major advance in aircraft electrical power systems during the development of the British V-bombers in the 1940s and 1950s where the Vickers Valiant B.1 illustrated in Figure 1.1 featured four three-phase 115VAC 400Hz 22.5kVA generators to satisfy the requirements of high power loads such as electrically actuated landing gear, radar and electronic warfare jamming equipment [12]. The Handley Page Victor V-bomber required four three-phase 115VAC 400Hz 50kVA generators to satisfy the fast growing demand for electrical power. A further development on the Vickers VC10 transport aircraft increased AC electrical system demand further by using electrically powered flight control actuators which replaced centralised hydraulic systems.

Figure 1.1: Vickers Valiant B.1 at Filton Airfield, Filton, Bristol, England, 1961 (Image Released Into Public Domain Courtesy of Ian Dunster, Wikipedia User *Arpingstone*)

Aircraft such as the McDonnell Douglas F-4 Phantom introduced high power 115VAC 400Hz AC generation systems which used a relatively unreliable hydro-mechanical Constant Speed Drive (CSD) to convert from rotational motion, which varies with engine speed, to constant frequency 400Hz AC which is more electrical load friendly. The availability of comparably reliable solid state switching technology has allowed electronic Variable Speed / Constant Frequency (VSCF) to be realised electronically thus replacing the hydro-mechanical CSD function. The VSCF technology is used on the McDonnell Douglas F/A-18 in a main generator application, and on the Boeing 777 in a backup AC power generation application. The 115VAC 400Hz Integrated Drive Generator (IDG) incorporating a variable frequency AC generator and Constant Speed Drive (CSD) within one compact unit is in common use on the Eurofighter Typhoon, Airbus A340 (2 × 90kVA), Boeing 717 (2 × 40kVA), Boeing 737NG (2 × 90kVA) Boeing 747-X (4 × 120kVA), Boeing 767-400 (2 × 120kVA), Boeing 777 (2 × 120kVA) and McDonnell Douglas MD-12 (4 × 120kVA).

As the requirement for electrical power increased further aircraft such as the Lockheed Martin F-22 and F-35 Joint Strike Fighter (JSF) illustrated in Figure 1.2 have opted to increase generator voltage levels to 270VDC in order to reduce weight, voltage drops, power dissipation and wire gauges. Both aircraft have two main generators where the F-22 and F-35 have 2 × 70kW and 2 × ∼80kW generators respectively. In addition to the main generators both the F-22 and F-35 feature significant energy storage in the form of 28VDC Lithium Ion batteries used for backup and transient fill-in purposes, where the more recent F-35 also features the first aerospace-grade 270VDC Lithium Ion battery. The presence of high voltage, high power, high energy density Lithium Ion batteries in the airframe drives a focus on electrical systems safety, since short circuits can easily lead to electrical fires. The electrical loads requiring power on the F-22 and F-35 include avionics, Electro-Hydrostatic Actuator (EHA) driven primary

flight surfaces, radar and electronic countermeasures, where the F-35 also features a demanding electric engine start function.

Figure 1.2: Lockheed Martin F-35 Joint Strike Fighter (Public Domain Image Courtesy of Senior Airman Julianne Showalter, U. S. Air Force)

The drive for a More Electric Aircraft (MEA) has led to major development in the form of the Boeing 787 illustrated in Figure 1.3 which made its first scheduled flight in August 2014. In similarity with the F-22 and F-35 the designers opted to make radical changes to the aircraft architecture and introduced electric engine start, electric Environmental Control Systems (eECS), electric cabin pressurisation, electric Wing Ice Protection Systems (eWIPS) electrically driven hydraulic pumps and electric brakes [13]. The electrification of the ECS, cabin pressurisation and WIPS functions has allowed the elimination of the pneumatic bleed system on the main engines which allows the engine to run more efficiently, thus reducing fuel burn, running costs and environmental impact. To achieve this the Boeing 787 is the first commercial airplane to use a 230VAC variable frequency (VF) distribution system and features 2 $\times$ 250kVA generators on the main engines and 2 $\times$ 225kVA generators on the Auxiliary Power Unit (APU) thus representing a twofold increase in power from the Boeing 777 platform [13]. The aircraft features 115VAC and 28VDC power conversion equipment such that power can be derived from the 230VAC distribution buses to power legacy loads and avionics equipment. The Boeing 787 is also the first civil aircraft to feature +/-270VDC power which is derived from the 230VAC bus and is used to drive adjustable speed motors used for $\sim$10 loads including the Nitrogen generating system for fuel tank inerting, ECS, engine start and hydraulic electric motor pump. However, a critical observation is that +/-270VDC power is confined to the Electrical Equipment (EE) bay and is not distributed throughout the airframe [14].

Figure 1.3: The Third Boeing 787 Prototype N787BX at the 2010 Farnborough Airshow (Image Courtesy of Wikipedia User *MilborneOne* Under the Creative Commons Attribution-Share Alike 3.0 Unported License)

The trade between AC and DC systems has long been argued since the "war of currents" era where Tesla and Westinghouse advocated the use of AC power and Edison promoted DC power for terrestrial power distribution [15]. This trade is still carried out to this day and it can be seen that some airframers have opted to pursue high voltage DC systems, and others have implemented high voltage AC systems. An interesting consideration regarding electrical power distribution is the effect of AC losses in the electrical wiring due to the skin effect. The skin depth δ for AC currents in a given conductor can be calculated in accordance with Equation (1.1) [16].

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{1.1}$$

where... ρ is the resistivity of the conductor (Ω·m), f is the frequency (Hz) and μ is the absolute magnetic permeability (H/m).

In contrast to terrestrial 50/60Hz high voltage AC systems the skin depth δ in a 400Hz AC electrical power distribution system is significant. Skin depth δ in such a system can be calculated by Equation (1.2) assuming the use of pure copper cables with resistivity ρ_{copper} and assuming that the relative permeability of copper can be approximated to that of free space.

$$\delta = \sqrt{\frac{\rho_{copper}}{\pi f \mu_0}} = \sqrt{\frac{1.68 \times 10^{-8}}{\pi \times 400 \times (4\pi \times 10^{-7})}} = 3.3mm \tag{1.2}$$

A skin depth δ of 3.3mm implies that the skin effect has little influence of conductors of diameter $\leq$6.6mm, and is more significant in larger conductors such as generator feeders and primary power output feeders. Higher power loads require more current and thus wider diameter cables, therefore the line voltage in AC systems should be carefully selected to optimise cable diameters and minimise skin effect losses. High voltage DC systems are therefore comparatively simpler and more attractive.

1.2 Future Trends in Aircraft Electrification

After reviewing the history of aircraft electrification it can be seen that the trend of increasing aircraft electrical power demand has continued to the present day as more aircraft systems are electrified. There is enthusiasm in the industry to further reduce fuel burn and to increase efficiency by pursuing the All Electric Aircraft (AEA). Beyond the great achievement of the Boeing 787 electrical system, a future concept for the AEA is environmentally-friendly electric taxi technology which reduces the period that the aircraft engines need to run when the aircraft is on the taxi way [17]. In addition to pollution caused by the running of the main engines another major contributor to airport emissions is the operation of the Auxiliary Power Unit (APU) which is typically used for main engine start. Stored energy in the form of a fuel cell has been considered for engine start in order to reduce APU emissions [18].

While advances are being made in the development of the more electric engine, where mechanical components are replaced with electronic components, this drives a requirement for power electronics components and systems which are capable of withstanding the harsh environmental conditions where high temperatures are prevalent in a non-pressurised area of the airframe [19]. Figure 1.4 illustrates the full-electric Airbus E-Fan concept aircraft which demonstrates that electric propulsion technology is advancing and thus the demand for electrical power is increasing further [20; 21].

Figure 1.4: Airbus E-Fan Full-Electric Technology Demonstrator in Flight at the Berlin Air Show, 2014 (Image Courtesy of Wikipedia User *Bernd Sieker* Under the Creative Commons Attribution-Share Alike 2.0 Generic License)

The continuing trend of increasing electrical power requirements and the corresponding increasing voltage levels has resulted in concern regarding the safety, reliability and robustness of the electrical power system. This is further exacerbated by the desire to optimise aircraft weight by distributing high voltage 230VAC and +/-270VDC power throughout the aircraft [22]. The availability of high performance, high voltage Silicon (Si) and Silicon Carbide (SiC) semiconductors has enabled the realisation of Solid State Power Controllers (SSPCs) which have provided the ability to rigorously monitor, control and protect both the low and high voltage aircraft electrical power distribution systems. Overcurrent protection of aircraft wiring using I^2t trip protection in SSPCs and circuit breakers is well understood and simple to implement. There are now concerns over other failure modes such as corona discharge, which is exacerbated by the presence of high voltages in low pressure / high altitude environments, and arc faults which require considerable further analysis [23].

1.3 The Electrical Wiring Interconnect System (EWIS)

Electrical wiring is an area of both academic and industrial engineering research which has seen a great level of investment in recent years. The majority of electrical power distribution systems use electrical wiring, and as such the research covers everything from the vast power distribution grids providing domestic power for homes, to smaller electrical power distribution systems on air, sea and land vehicles.

The Electrical Wiring Interconnect System (EWIS) on modern aircraft is designed to function safely and reliably for the full design life of the aircraft [24]. However, aircraft are now operated beyond their original design life due to economic and environmental constraints. As an example of electrical complexity in an aerospace application, one Airbus A380 alone houses 1,150 electrical functions, 98,000 wires with 40,000 connectors, and ∼530 kilometers (330 miles) of wire [25].

Faults in the EWIS are of great concern to the safety and reliability of both commercial and military aircraft. Faults in aircraft wiring have been implicated in a number of severe aircraft accidents, the most notable of which are the Swiss Air-111, TWA-800, and UAL-811 flights where in each case the aircraft was lost [26; 27; 28]. Following these tragic events the Federal Aviation Administration (FAA) launched an ageing aircraft programme where electrical wiring failure modes in ageing aircraft were researched intensively. In 2008 the FAA released the final report of the aircraft wiring degradation study which highlighted the causes and effects of different EWIS failure modes. One widely recognised EWIS failure mode that has received significant focus is the “arc fault”.

The Boeing 787 currently uses +/-270VDC electrical power which is confined to the EE bay. In future aircraft there is a desire to distribute 270VDC and +/-270VDC

throughout the airframe in the quest for further weight reduction and thus efficiency improvements. A major concern is that as the voltage levels used in the distribution of electrical power through the airframe increase, the impact and probability of electric breakdown events and "arc faults" escalates. It is therefore necessary to understand how to manage these new threats and how to engineer a safe and reliable electrical power distribution system and EWIS, beginning with a definition of the electric arc phenomena.

1.4 Definition of the Electric Arc

A review of the literature identified that the definition of the electric arc is highly dependent upon the physical and electrical behaviour of the electric arc. A literature search of reference books, technical papers and historical publications reveals that there are various different definitions of the "electric arc", where no absolute and precise definition was found. Firstly, the IUPAC Compendium of Analytical nomenclature states [29]:

> *"An electrical arc is a self-sustaining electrical discharge between at least two electrodes and is characterised by a comparatively small cathode fall voltage, a low burning voltage and a relatively high current density. The burning voltage of an arc is the voltage across the electrode gap during an arc discharge."*

C. D. Child proposes that it is not known who first created the electric arc because the electric arc and the spark had not been differentiated [30]. Child later proposes that a spark is defined as a short-duration electrical breakdown, and that the electric arc is defined as a continuous breakdown event. R. T. Compton was faced with the same issue when attempting to define the "electric arc", and states [31]:

> *"An arc is a discharge of electricity, between electrodes in a gas or vapor, which has a voltage drop at the cathode of the order of the minimum ionizing or minimum exciting potential of the gas or vapor."*

Finally J. B. Calvert defines the electric arc based on a characterisation of the static arc current / voltage electrical circuit behaviour thus [1]:

> *"The arc discharge is a high-current, low-voltage discharge, in contrast with the low-current, high-voltage glow discharge."*

Calvert also characterises the impedance of an electric arc as a negative differential impedance and this behaviour can be clearly seen in Figure 1.5 between points B' and C.

The definitions provided for the electric arc are all subtly different and different researchers attempt to define the arc based upon different physical characteristics where a summary of these characteristics is given in Table 1.1.

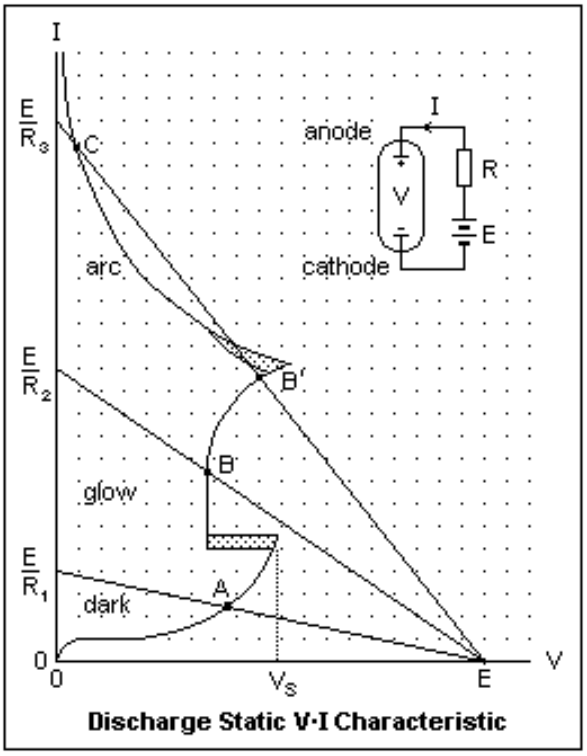


Figure 1.5: Characterisation of Discharge Types In Static V-I Behaviour [1]

Defining Characteristic	**Description**
Electrodes	An electric arc occurs between two electrodes, an anode and a cathode.
Magnitude of Electric Arc Current / Voltage	An electric arc is a Low voltage, high current event in comparison to other gas discharges.
Dependence on Physical Arc System	The electric arc has a cathode voltage drop of the order of the minimum exciting potential of a given gas.
Current Density	The current density of the electric arc is high with respect to other types of gas discharge.
Arc Impedance	The electric arc exhibits a negative differential impedance characteristic.
Duration	The electric arc is a continuous discharge event.

Table 1.1: Summary of the Possible Defining Characteristics of Electric Arcs

1.5 Definition of the Arc Fault

The term "arc fault" is a general term which covers two well-defined fault conditions, the series arc fault and the parallel arc fault, where these scenarios are summarised in Sections 1.5.1 and 1.5.2 respectively. Similarly the terms "arc fault detection" and "arc fault protection" are defined in Section 1.5.3.

1.5.1 Series Arc Fault

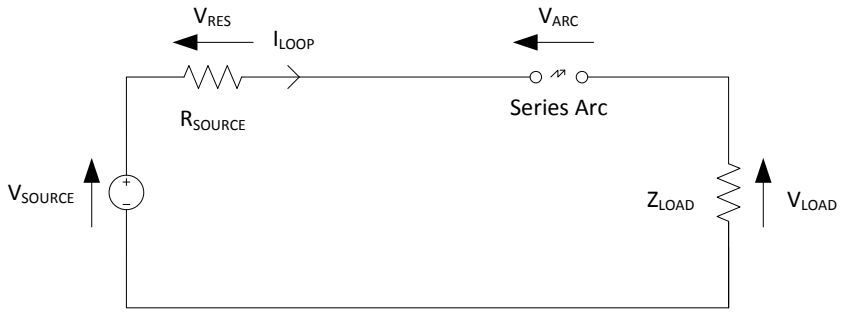


Figure 1.6: A Simple Power Supply Loop Illustrating A Series Arc Fault

A series arc fault can be defined as an arc fault which manifests itself in series with the load in a typical electrical power distribution system [32; 33; 34]. By analysing the simple series arc fault example in Figure 1.6 it can be determined that arc power in this scenario is constrained by the both the source and load impedances, since the arc current is limited by the maximum load current [34]. The impact of the series arc on the loop is a reduction in voltage across the load and thus a decrease in loop current, where the resulting power dissipation in the arc causes temperatures in the arc column from around 5000K to 20000K [3] which can cause damage to local system components. If a series arc fault occurs in the centre of a cable bundle in a given system and it is left uninterrupted then this can cause adjacent cable insulation to melt which can lead to parallel arc faults between other conductors in the bundle.

Detecting series arc faults using basic thermal circuit breakers is not possible since the current during a series arc event is similar to that of the standard load current [34]. The circuit breaker rating is also typically derated against the load current which implies that the series arc fault is well within the typical thermal circuit breaker normal operating area as detailed in MIL-STD-1760 [35; 36]. Circuit breakers and modern Solid State Power Controllers (SSPCs) implement I^2t wire protection, where thermal circuit breakers function by means of thermal dissipation caused by the breaker current which heats a bimetallic strip and in turn trips the circuit breaker, and SSPC technology typically measures current and feeds this data into a software-based I^2t protection algorithm. Figure 1.7 illustrates a typical SSPC I^2t trip curve and highlights the series and parallel arc fault threat regions. The "never" and "always" curves

limit the variation in I^2t trip performance with ambient temperature, and a typical SSPC can provide steady state current up to 118% of rated current without tripping.

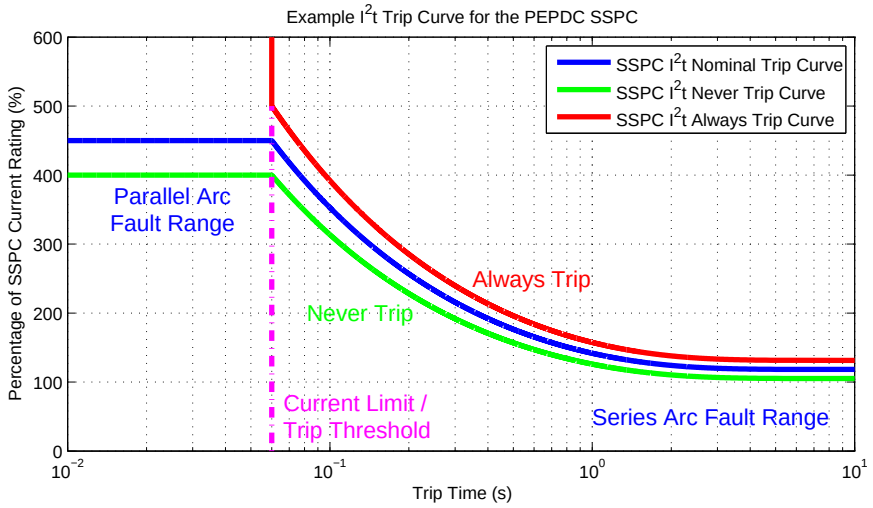


Figure 1.7: Typical SSPC I^2t Trip Curve Showing Arc Fault Threat Regions

1.5.2 Parallel Arc Fault

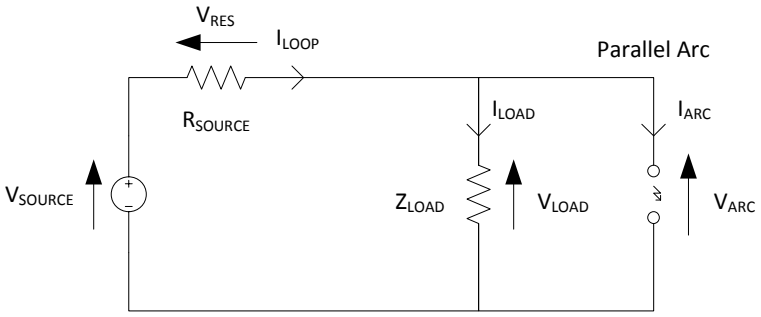


Figure 1.8: A Simple Power Supply Loop Illustrating A Parallel Arc Fault

A parallel arc fault can be defined as an arc fault which occurs in parallel with the load in a typical electrical power distribution system [32; 33; 34]; a simple example of the parallel arc is illustrated in Figure 1.8. Parallel arcs are problematic because very often parallel arcs are similar in nature to short circuits where arc currents are in the range of the short circuit current capability of the power source [34]. Electrical distribution networks fitted with fast thermal circuit breakers will offer a level of protection against parallel arc faults, but the parallel arc fault current may fall within the acceptable operating envelope for a given breaker [34].

In contrast to series arc faults the maximum arc power in a parallel arc is limited only by the source impedance of the power supply and feeder cables, with the exception of

current limits imposed by any overcurrent devices used in the electrical system. Thermal circuit breakers may be triggered in the event of the overcurrent event caused by the parallel arc fault, however with this approach the circuit breaker has to respond quickly in order to prevent the arcing conductors from vapourising and causing secondary damage. This necessitates the use of fast solid state switching devices as a means of isolating power in the event of a parallel arc fault since traditional mechanical circuit breakers may either weld shut or be too slow opening (typically 50ms) in response to a parallel arc fault scenario thus allowing severe damage to occur before a trip can be completed. It is widely assumed that parallel arc faults dissipate powers that are several orders of magnitude greater than that of series arc faults since the load impedance does not limit the arc current, and thus a typical parallel arc fault lies above the I^2t trip curve illustrated in Figure 1.7 [34].

1.5.3 Arc Fault Detection and Protection

Arc Fault Detection can be defined as the detection of an "arc fault" based upon a given physical characteristic of the electric arc phenomenon. Arc Fault Protection can be defined as the capability to protect a given electrical distribution system from the effects of an "arc fault". Arc Fault Protection firstly requires detection of an "arc fault" followed by a remedial action, where an example of remedial action is to open the circuit breaker or SSPC which is supplying power to the given arc fault.

1.6 Motivations

1.6.1 Arc Fault History in Aircraft

The motivations for the work carried out in thesis were derived firstly from the history of arc faults in aviation, while also considering the threat of increasing electrical power distribution voltages highlighted in Sections 1.1 and 1.2. The literature surrounding the history of "arc faults" in aircraft indicates that there have been a number of recorded incidents where arc faults have been the cause of / contributor to aircraft damage or loss. Faults in aircraft wiring have been implicated in a number of severe aircraft accidents including the Swiss Air-111, TWA-800, and UAL-811 flights, and have contributed to many flight delays [37].

Swiss Air-111, a McDonnell Douglas MD-11 with 215 passengers and 14 crew members on board was on a scheduled flight from New York, US to Geneva, Switzerland on 2nd September 1998. 53 minutes after take-off, the flight crew detected a mysterious odour in the cockpit; the odour was later found to be the result of a fire. It was determined that the fire most likely started from an electrical arcing event that occurred above the ceiling on the right side of the cockpit near the cockpit rear wall [26]. The executive summary of the crash investigation states that a section of arced electrical

cable from the in-flight entertainment network was found in the location where the fire originated.

Trans World Airlines Flight 800 (TWA-800), a Boeing 747-131 with 212 passengers and 18 crew members on board exploded and fragmented in mid-air near East Moriches, New York, US on 17th July 1996, 12 minutes after take-off [27]. There was evidence of arcing in a wire bundle that included the Fuel Quantity Indication System (FQIS) wiring that connected with the Centre Wing Tank [27]. Safety issues in the air crash investigation report focus on fuel tank flammability, fuel tank ignition sources, design and certification standards, and the maintenance and ageing of aircraft systems [27]. The report suggests that after prolonged exposure, water could enter the potting of the wire terminal assembly, leading to corrosion; the report goes on to state that the corrosion can lead to arcing. The arcing in this scenario causes thermal expansion and can result in the failure of the pump hardware.

United Airlines Flight 811 (UAL-811), a Boeing 747-122 with 337 passengers and 18 crew members on board suffered explosive decompression in mid-air near Honolulu, Hawaii, US on 24th February 1989, following take-off [28]. There was no visible external evidence of burning, arcing, or heat distress in any of the wires removed, however several areas of wire insulation damage were found [28].

A more recent event occurred in 2010 where a fire ignited on-board a Boeing 787 test aircraft, ZA002 [38]. Engineers have determined that the fault began as either a short circuit or an electrical arc in the P100 power distribution panel, most likely caused by the presence of foreign debris [38]. This incident demonstrates that the use of rigorous design processes and design-based arc fault prevention measures alone are not sufficient to prevent electrical arcing, and that there is value in provisioning arc fault detection and protection technology as a last line of defence against series and parallel arc faults.

As a result of the recorded aircraft incidents the FAA recently carried out the "Aircraft Wiring Degradation Study" [24] where the importance of the investigation is described as follows:

> *"The continued safe operation of aircraft beyond their expected service life depends on the safe and effective transfer of power and electrical signals between aircraft electrical components."*

During the life of an aircraft the wiring looms are subjected to heat, humidity, chemical contamination, electrical stress, mechanical stress and thermal stress, where the results of which can lead to the failure of either the conductor itself or of the insulation material [24]. Under these stress conditions the life of a given wire depends upon its location in the aircraft, for example a wire located inside the engine cowling will

experience wide temperature ranges and wide pressure variation, whereas a similar wire inside the fuselage may be at a consistent pressure at a regulated temperature. The location of a wire within a given loom also affects its behaviour over time because wires in the centre of a bundle tend to be shielded from their environment by neighbouring wires which makes the prediction of failure of a given wire difficult on an individual wire-by-wire basis. It can therefore be concluded that in electrical power systems there is a requirement that the degradation of a given feeder wire shall not lead to a catastrophic failure of the electrical power system, nor shall it cause damage to surrounding wiring or equipment, and thus the requirement for arc fault detection / protection systems is born.

1.6.2 Arc Fault History in Domestic Dwellings

As an adjacent concern there is a significant volume of literature regarding arc faults in domestic dwellings. In 2008 the United States Fire Association issued a report on domestic building electrical fires, which states [39]:

> *"Annually, an estimated 28,300 residential building electrical fires cause 360 deaths, 1,000 injuries, and $995 million in direct loss."*
>
> *"Nearly half (47%) of the residential building electrical fires where equipment was involved were caused by the building's wiring."*

Arc Fault Circuit Interrupters (AFCI), also known as Arc Fault Circuit Breakers (AFCB), were first introduced in the early 1990s in the US and the requirement for AFCIs has been included in the National Electrical Code® (NFPA 70) [40] 1999, 2002, 2005, 2008 and 2011 editions [41]. As a consequence there is much literature in this area which must be considered as background during investigations into arc fault detection and protection systems for aerospace applications.

1.6.3 Arc Fault Detection / Protection Standards

The threat of arc faults in aircraft wiring has lead to a quest for robust airworthy arc fault detection / protection systems. To ensure that the aviation systems industry develops safe and reliable algorithms the Society of Automotive Engineers (SAE) has developed and issued the first standard for arc fault detection on aircraft, SAE AS5692 "ARC Fault Circuit Breaker (AFCB), Aircraft, Trip-Free, Single Phase 115VAC, 400 Hz - Constant Frequency" [8]. This standard relates specifically to arc fault circuit breakers, however the test methodology in this standard has been applied to develop arc fault detection capability for integration into SSPCs (Solid State Power Controllers). SAE AS5692 is instrumental in defining the test requirements for arc fault detection, and attempts to replicate representative series and parallel arc faults. A new revision of the SAE AS5692 standard is in progress for 28VDC arc fault

detection systems, and recently the SAE AE-7 Committee has commenced upon a new standard SAE AS6087 which will cover 270VDC arc fault detection requirements. At the time of writing, the author is a member of the SAE AE-7 subcommittee responsible for the development of SAE AS6087.

It is not heavily documented, however it is the author's experience that a number of aircraft electrical power system designers have attempted to implement arc fault detection / protection systems using the SAE AS5692 standard, but a majority of these systems have presented "nuisance trips" in the presence of representative aircraft electrical loads. A motivation here is therefore to produce an arc fault detection system which avoids or at very least minimises nuisance trip behaviour.

The main arc fault detection standard for non-aerospace AFCI devices is the Underwriter's Laboratories ANSI/UL1699 [42] whose scope concerns 120VAC 60Hz systems with a maximum AFCI rating of 20A. The AFCI devices covered in ANSI/UL1699 are not designed to detect "glowing connections" and are limited to arc fault detection only. This part of the scope leads to the questioning of the statistic in Section 1.6.2 regarding whether arc faults are the main cause of residential building electrical fires and injuries, or whether other failure modes such as "glowing connections" are more probable and prevalent. "Glowing connections" are caused by the introduction of local series resistance in a power distribution circuit, the resistance increases power dissipation in the fault area which causes a glow to establish [43]. Ettling reports that "glowing connections" can be reproduced experimentally by creating intentionally loose connections similar to those found in faulty connectors.

A further motivation is therefore the consideration of how a given arc fault detection solution could meet requirements of the regulatory and commercial environment with regard to aircraft certification and the development of a compliant yet cost effective arc fault detection system.

1.6.4 History of Arc Fault Detection at GE Aviation Systems Ltd

GE Aviation Systems Ltd have prior experience of arc fault detection technology which was developed for 28VDC and 115VAC 400Hz applications as part of the Modular Power Tile (MPT) product family, and have contributed arc fault detection capability and electromechanical / solid state electrical power distribution expertise to multiple collaborative research projects. Arc fault detection capability was successfully demonstrated on the Air Force Research Lab (AFRL) funded "Aircraft Electrical Power Systems Prognostics and Health Management (AEPHM)" programme [44] led by Boeing, and the European Commission funded "More Open Electrical Technologies (MOET)" programme [45] led by Airbus. The MOET trials in particular highlighted that further work covering arc fault detection technology is required for the More Elec-

tric Aircraft (MEA) and All Electric Aircraft (AEA) where higher voltage 270VDC and +/-270VDC electrical power distribution systems are implemented.

1.6.5 Future Trends in Arc Fault Detection

There have been a number of attempts to produce arc fault detection systems for 28VDC and 115VAC 400Hz systems using a variety of different properties of electric arc faults from analysis of current/voltage waveforms through to observation of ultra-violet light emitted. It is the opinion of the author that to produce a robust arc fault detection system based on current/voltage waveforms the designer must first fully characterise the given fault and relate recorded data to the fundamental arc physics rather than blindly applying complex pattern recognition techniques, and second form a holistic understanding of the effect of arc faults on the electrical power distribution system at different levels, under varying load conditions and in the presence of loads which produce arcs during normal operation before considering a solution. To further understand the interaction between arc faults and the solid state electrical power distribution system, there is a desire to model and simulate arc fault behaviour without needing to set up a complex test facility each time a new arc fault scenario needs to be investigated. Furthermore the ability to accurately model arc faults accurately allows for simulation of these arc fault detection approaches before committing a solution to physical hardware and software.

The trend towards the use of SSPCs rather than electromechanical circuit breakers for load switching in aircraft electrical power distribution systems results in circuit currents which can be interrupted without producing an arc as part of the switch opening process. This implies that it is also possible to influence arcs by modulating the impedance of the solid state switch during an arcing event as a possible means of actively identifying a given arc fault, and this is a further motivation for the research in this thesis.

1.6.6 The PEPDC and PEPSC Projects

A final and major motivation for this thesis is the need to develop a series arc fault detection system for the Primary Electrical Power Distribution Centre (PEPDC) and Primary Electrical Power Solid (state power) Controller (PEPSC) projects.

The PEPDC project is a GE Aviation Systems Ltd funded civil technology demonstrator aimed at TRL-5 [46] which is designed to provide a solid state primary power distribution solution incorporating 7 x 270VDC 60A and 7 x 270VDC 120A SSPC modules. The PEPDC unit is a major component in the Solid State Electrical Distribution Unit (SSEDU) which has been demonstrated successfully at the Air Force Research Labs (AFRL) [47]. The PEPDC features a current limit function which prevents severe parallel arc faults from forming, and allows fast interruption of short

circuit and overcurrent faults. In order to provide complete protection against arc faults, each SSPC also requires a series arc fault detection function which is provided using the techniques developed by the author in this thesis.

At the time of writing the author is currently employed as Engineering Project Manager and Lead Engineer on the PEPSC project which is a part-funded Innovate UK civil technology demonstrator aimed at TRL-5 [46]. The PEPSC builds on SSPC technology developed under the PEPDC and provides a single solid state 270VDC 120A contactor replacement unit [48]. The change in form factor from the PEPDC card-and-backplane solution to a highly integrated solution in the PEPSC requires a transferable series arc fault detection solution, and the development of this series arc fault detection system is also covered by the author in this thesis.

1.7 Thesis Goal

Based on the motivations outlined in Section 1.6 the main goal of this thesis can therefore be summarised thus:

> *"The characterisation, modelling, simulation and detection of series arc faults in aircraft electrical power distribution systems featuring Solid State Power Controllers (SSPCs)"*

Although this goal is focussed on an aerospace application for series arc fault detection, the realisation of this goal requires a broad level of understanding from aircraft system level, through hardware and software down to the physical understanding of electric arc phenomenon. This goal was broken down and bounded by the scope of work in Section 1.8 to ensure a focused approach to was taken to realising this goal.

1.8 Thesis Objectives and Scope of Work

To meet the thesis goal there are a number of objectives which need to be addressed and these form the main scope of the doctoral work undertaken in this thesis. The ten discrete thesis objectives are presented thus:

1. **Literature Review**
   Identify similar arc fault detection and protection research by means of an in-depth literature review in order to gain a detailed understanding of the issues surrounding the state of the art in arc fault detection, and to highlight potential further areas for investigation.

2. **Characterisation**
   Characterise series arc faults in aircraft solid state electrical power distribution systems while considering aircraft-representative wiring configurations, power sources and loads in order to define the arc fault detection problem space.

3. **Modelling/Simulation**
   Evaluate, develop and validate a series arc fault model and corresponding simulations against the captured characterisation data, again considering aircraft-representative wiring configurations, power and loads. This allows the electrical impact of series arc faults on the solid state switching hardware and the wider electrical power distribution system to be understood, and enables the effect of series arc faults to be demonstrated to a wider audience.

4. **Sensor Evaluation**
   Evaluate different sensor technologies to detect arcs within aircraft representative wiring configurations, power and loads. The purpose here is to identify where a given sensor element needs to be deployed.

5. **Hardware Design**
   Evaluate and develop physical series arc fault detection hardware for use in the PEPDC 270VDC 120A SSPC and PEPSC 270VDC 120A SSPC modules. The purpose of the project is to provide a series arc fault detection technology demonstrator, and in order to do this a hardware solution is required.

6. **Algorithm Design**
   Investigate and develop series arc fault detection algorithms for deployment into the PEPDC and PEPSC arc fault detection hardware.

7. **Nuisance Trips**
   Investigate arc fault detection methods and algorithms which are able to detect series arc faults without causing nuisance trips when other spurious transients appear on the aircraft bus power due to Electrical Power Variation / Electrical Load Variation.

8. **Integration Testing**
   Perform integration testing on the final arc fault detection hardware and software solution used in the GE Aviation Systems Ltd PEPDC 270VDC 120A SSPC and PEPSC 270VDC 120A SSPC modules.

9. **Power Line Modulation**
   Investigate the benefits of using the solid state switching technology in the PEPDC and PEPSC modules to modulate the power line during a series arc fault event. The purpose of this objective is to determine if an active arc fault detection scheme is possible using these techniques.

10. **Further Work**
    Identify further work based on completion of the integration testing of the arc fault detection hardware and software in the PEPDC 270VDC 120A SSPC module.

1.9 Thesis Structure and Chapter Summary

In this section the thesis structure is presented along with a summary showing the significance of, and contribution provided by each chapter. The sequencing and purpose of each chapter within the wider thesis context is discussed and related to the top level thesis objectives outlined in Section 1.8, where novel aspects of the research and original contributions to knowledge are clearly identified.

1.9.1 Chapter 2 - Understanding Arc Faults, and the State of the Art in Arc Fault Detection

Following a clear definition of the series arc fault threat and the project scope, the purpose of Chapter 2 is to begin understanding arc faults and the state of the art in arc fault detection in greater detail by means of an extensive literature review.

The literature review commences by discussing existing arc fault detection literature reviews carried out with a bias towards both the automotive and aerospace sectors. Arc fault test methods and standards from different sectors are also analysed in order to outline likely arc fault failure modes, and to highlight the importance of series arc fault detection where the source of data was primarily directly from test standards themselves, and secondly from IEEE journal articles covering the use of these test standards. Understanding the regulatory position on requirements for arc fault detection technology is critical to developing a compliant and certifiable solution.

Although this thesis is primarily concerned with detection of 270VDC series arc faults, the literature review covers both AC and DC, parallel and series arc fault behaviour in order to understand the similarity between these faults and to determine how the arc physics are manifested in each type of fault, where the source of data here is primarily IEEE and SAE journal articles. When considering arc fault detection techniques it is important to understand the relationship between physical and electrical behaviour of arc faults before attempting to determine a solution.

The review of arc fault detection methods is divided broadly into passive and active methods where the relative advantages and disadvantages of each method are discussed. The literature review also explores methods of arc fault detection where different passive schemes are combined in order to realise more specific detection and better resilience to nuisance trips. Methods of discriminating and differentiating arc faults from other system transients using passive detection techniques and trip coordination have also been covered. Literature regarding arc fault detection techniques was taken from a wide variety of sources where a significant number of IEEE transactions and conference papers were studied, along with many patent documents since these provide insight into the different practical approaches to arc fault detection, protection and location.

Nuisance trips and certification considerations are explored here since the minimisation of nuisance trips is critical to the development of a robust aerospace arc fault detection system.

1.9.2 Chapter 3 - Behavioural Modelling and Simulation of Series Arc Faults in Aircraft Electrical Power Distribution Systems

Following an extensive electrical characterisation activity of series arc fault behaviour in aircraft DC solid state electrical power distribution systems featuring SSPCs presented in Appendix A, the purpose of this chapter is to present the development of a series arc fault SPICE model which can be integrated with existing GE Aviation Systems Ltd SSPC SPICE models. SPICE is typically used for SSPC hardware models since these are component-level models which allow accurate studies of SSPC switching and failure modes to be carried out. It is therefore proposed that a SPICE arc fault model would integrate with existing SSPC models and allow arc fault / SSPC interaction to be simulated.

The original contribution to knowledge and therefore the purpose of the research presented in this chapter is the provision of quantitative simulation data and qualitative analysis of the interaction between a modified Nottingham series arc fault model and the wider 28VDC and 270VDC solid state aircraft electrical distribution system model.

The arc fault model development and methodology are presented, beginning with a review of historical static V-I and energy balance arc model literature and moving on to the development of a SPICE-compatible arc equation before covering the detailed parametric and configurable arc model development.

The integrated model is used to simulate the effect on the SSPC of introducing capacitive, inductive and resistive loads, different system voltages, and Electrical Power Variation profiles from RTCA DO-160G Section 18 [49] in the form of bus ripple. The simulation results from the integrated solid state electrical power distribution system and modified series arc model are validated against the experimental results captured in Appendix A and the limitations of the proposed model are discussed. Academic and industrial study has been carried out for over a century and as yet there is no unilateral arc model solution, and thus the final part of this chapter highlights the envelope under which the developed SPICE model is valid.

The scope of this work is to qualitatively determine the behaviour of the SSPC hardware in response to series arc faults and not to invest significant effort in equation development and lengthy parameter extraction associated with arc modelling since there is already significant literature in this area. The second assumption is that the SPICE models developed shall be demonstrated in DC electrical power distribution

systems only covering 28VDC and 270VDC systems and should be scalable such that future 115VAC 400Hz, +/-270VDC and 230VAC CF 50/60/400Hz and 230VAC VF systems can be modelled without significant modification to the models developed in this work package.

1.9.3 Chapter 4 - Development and Evaluation of a Voltage Invariant Arc Fault Detection System

The motivation for the work in Chapter 4 is the need to provide a series arc fault detection system for the PEPDC and PEPSC SSPC modules. Given that the development of active arc fault detection schemes is a complex and expensive affair, the author strategised that immediately attempting to develop an active arc fault detection system is not an appropriate step until the possibility of passively detecting faults using current and voltage waveforms has been exhausted. The electrical characteristics of series arcs in 270VDC systems were explored during the characterisation activity in Appendix A, and the purpose of this chapter is to design a system to passively detect series arc faults based on these fundamental electrical arc characteristics.

The original contribution to knowledge in this chapter is simply that this is the first successful attempt at providing a passive arc fault detection solution for 270VDC electrical power systems.

The chapter begins by presenting the top level requirements for the proposed series arc fault detection system before deriving the required hardware and software requirements. The hardware development covers the implementation of voltage and current sensors for passive series arc fault detection, based on the characterisation data analysed in Appendix A. The software development covers the detection and confirmation of arc events. In order to verify the proposed series arc fault detection solution, the test scenarios used during characterisation are repeated and the results are analysed allowing the success of the proposed arc fault detection scheme to be demonstrated quantitatively. The chapter then provides a discussion exploring the significance of the results and explores the limitations of passive arc fault detection scheme against the top level requirements.

1.9.4 Chapter 5 - Development and Evaluation of an Arc Fault Perturbation / Confirmation Scheme

Following on from the electrical characterisation and modelling of series arcs in Appendix A and Chapter 3 respectively, an arc fault detection scheme was developed in Chapter 4 and a focus was subsequently placed on reducing nuisance trip behaviour based on the findings of the literature review in Section 2.9. The literature review highlighted that purely passive schemes which rely on a series arc fault classifier cannot be completely free from nuisance trips. The motivation for the work on an active

arc fault perturbation / confirmation scheme therefore stems from a need to accurately detect and isolate arc faults in aircraft electrical power distribution systems during operation without nuisance tripping.

The first original contribution to knowledge for the research presented in this chapter is a novel alternative active arc fault detection / perturbation / confirmation technique based on the concept of SSPC output modulation during a passively detected series arc fault event. The SSPC modulation is designed to induce system behaviour unique to the underlying physics of series arc faults. Series arc faults are generated using a loose terminal scenario subjected to a typical aircraft vibration profile given by SAE AS5692 [8] and RTCA DO-160G [49]. The loose terminal scenario is inserted in a representative solid-state aircraft electrical power distribution system where the system can be analysed at 270VDC for varying load characteristics.

This scheme was used to further validate the series arc fault system model developed in Chapter 3 by loading the model with the required timing parameters in line with the proposed perturbation / confirmation scheme. The resulting simulation results correlated well with the experimental data. The system model from Chapter 3 is therefore a valuable tool for trialling SSPC modulation techniques.

During the development of the arc fault perturbation scheme it is also determined that both a loose terminal and drawn series arc fault could be detected and/or confirmed when the SSPC is open, due to the interaction of the arc fault with the SSPC leakage current. Leakage currents are present due to the imperfect behaviour of the semiconductor switching devices in their off-state. The SSPC output leakage voltage phenomena is experimentally characterised for varying series arc fault conditions and a novel arc fault detection / confirmation scheme is proposed. During development of the series arc fault perturbation scheme it was further determined that when the SSPC was opened following a suspected series arc fault, the interaction of the loose terminal fault with the SSPC output leakage current and SSPC output leakage voltage yielded a signal which was indicative that a series wire fault was present in the distribution system. The second original contribution to knowledge in this chapter is therefore a novel series arc fault confirmation, and series wire fault detection system.

The third and final contribution to knowledge in this chapter is a novel Initiated Built-In Test (IBIT) scheme which further reduces the likelihood of nuisance trips due to unexpected faults in the series arc fault detection hardware developed in Chapter 4. The IBIT scheme allows for reduction of nuisance trips due to incorrect operation of series arc fault detection hardware when no series arc fault is present, and also allows the reliability and availability of the series arc fault detection system to be improved by providing aircraft maintenance crews the ability to initiate an IBIT function on demand. The IBIT scheme is furthermore implemented in the PEPDC and PEPSC and the successful results of verification testing are presented and discussed.

1.9.5 Chapter 6 - Conclusions and Further Work

The thesis conclusions are presented, the significance and implications of the research are analysed, the pre-existing arc fault detection approaches are challenged, and the original contributions to knowledge are discussed. The limitations of the concepts and data presented in the research are explored, and future research is recommended based on these limitations.

1.10 List of Publications/Patents

Given the author's involvement with industry during his doctoral studies, any Intellectual Property (IP) arising from work on this project was closely controlled. Since the majority of the work carried out on this project yielded novel IP, the company public-release approval procedure limited the opportunity to produce publications arising from this research during the course of study. In the interests of securing IP rights several patents were filed during the project where those patents published are given in Table 1.2, and those patents filed are presented in Table 1.3.

Publication Number	**Inventor(s)**	**Title**
CA 2,813,933 A1 [50] CN 103,384,446 A [51] DE 102,013,104,286 A1 [52] US 8,842,398 B2 [53]	Peter James Handy, Adrian Shipley (GE Aviation Systems Ltd)	Apparatus and method for arc fault detection

Table 1.2: Patents Published During Study

GE Disclosure / Docket Number	**Inventor(s)**	**Title**
44999 / 265352	Peter James Handy	Built-in-Test Method for Arc Fault Detection Hardware
33811 / 268868	Peter James Handy, Adrian Shipley	Perturbation Technique for Arc Fault Detection
55075 / 274954	Peter James Handy	A bifurcated method of arc fault detection and location, using arc fault perturbation technique and TDR/FDR/STDR/SSTDR
62939 / 282149	Peter James Handy	A method of detecting arc faults and open circuits in electrical switches using the switch leakage

Table 1.3: Patents Filed During Study

Chapter 2

Understanding Arc Faults, and the State of the Art in Arc Fault Detection

2.1 Introduction

2.1.1 Purpose and Scope

The purpose of this literature review is to outline the basic properties of electric arcs and arc faults and to present existing research in the field of arc fault detection. While the overall goal of the thesis is to research a high voltage series arc fault detection system for a 270VDC aerospace electrical power system application, the scope of the literature review was expanded to cover firstly arc fault test methods, secondly AC and DC arc fault behaviour, and thirdly detection and location of arc faults and wire faults in automotive, domestic, industrial and aerospace electrical power distribution systems. The techniques used in these adjacent areas are of great interest when considering the wider series arc fault detection challenge.

Arc fault detection techniques based on electrical phenomena experienced during electric arcing have driven significant research in both academic and industrial establishments over the last twenty years. The author has determined that arc fault detection, protection and location schemes can be categorised broadly into two categories where firstly passive methods observe a characteristic of the system and use a classifier in order to detect and/or locate the given arc fault prior to performing a corrective action, and secondly active methods apply a stimulus to the system under test in an attempt to provoke a response associated with an arc fault such that the fault can be detected, isolated and located. There are other novel methods which are arguably neither passive nor active schemes, where the electrical system itself is modified in order to either avoid or prevent series arc faults in the first instance, and these are captured in a separate section.

2.1.2 Literature Review Structure and Sources of Data

The first section of the literature review covers arc fault circuit breaker standards and arc fault test methods where the source of data was primarily directly from test standards themselves, and secondly from IEEE journal articles covering the use of these test standards.

The second section of the literature review covers behaviour of arc faults, and the source of data here is primary IEEE and SAE journal articles.

The subsequent eight sections of the literature review address active and passive arc fault detection / protection / location methods, combined detection methods, discrimination methods, nuisance trips and trip coordination. Literature for these sections was taken from a wide variety of sources where a significant number of IEEE transactions and conference papers were studied, along with many patent publications which provide insight into the different practical approaches to arc fault detection, protection and location.

The final section reviews literature discusses certification considerations and is covered solely by Federal Aviation Authority (FAA) publications.

2.1.3 Existing Arc Fault Literature Reviews

A number of literature reviews have been carried out in the area of arc fault detection, the most prominent of which is the "Ageing Aircraft Wiring Fault Detection Survey" which was prepared as part of the "Aircraft Ageing and Durability Project" by NASA in 2007 [54]. This report details purely active wire fault detection methods and covers Time Domain Reflectometry (TDR), Frequency Domain Reflectometry (FDR), Standing Wave Reflectometry (SWR), Multi-Carrier Reflectometry (MCR), Microradar, Micro Energy Tool (MET), Noise Domain Reflectometry (NDR), Sequence Time Domain Reflectometry (STDR), Spread Spectrum Time Domain Reflectometry (SSTDR), Pulse Arrested Spark Discharge (PASD), Partial Discharge Detection, Optical Current Sensors and Acoustics. These technologies are reviewed in the "active arc detection methods" section of this review.

Earlier in 2005, during a short period where 42VDC battery technology was under research for automotive applications, Mishrikey completed a study on broadband noise emissions of arcs and the effect on system voltage during arcing. He observed an increase in the noise floor in the range 300kHz through 30MHz from -70dBm to -38dBm under the arcing scenario [55]. This thesis presents before and after arc frequency-magnitude plots and is a good reference for studies on arc emissions.

More recently in 2013 Kumpulainen et al published two reviews of preemptive arc fault detection techniques for switchgear and control gear, and while this does not re-

late directly to the application of series arc fault detection in an aerospace application the detection requirements are comparable [56; 57]. Kumpulainen begins by outlining the arc fault mitigation principles where prior to arc ignition the active approach of "arc prediction" can be implemented using on-line monitoring systems to detect potential difference, temperature, UV and smoke. A passive approach to pre-ignition detection is defined as "arc prevention" where design, education and proper maintenance can be used to limit exposure to the potential damage caused by arc faults. Passive post-ignition schemes are not applicable to aerospace applications, however for completeness Kumpulainen et al highlight arc resistant switchgear and Personal Protective Equipment (PPE) as arc fault mitigation. Finally active post-ignition mitigation techniques include "arc detection" based on detection of light, overcurrent or pressure; "arc relays" which may included dedicated systems, integration into numerical relays or stand-alone devices; and finally "arc elimination" using circuit breakers or arc eliminators.

Kumpulainen et al give an excellent outline of possible arc fault sensor technologies in their first publication which are: RF sensor, coupling capacitor, capacitive sensor, high frequency CT, Rogowski Coil, Piezoelectric ultrasonic sensor, ultraviolet sensor, thermal sensors, thermal ionisation detector and D-dot sensors [56]. These technologies are evaluated for suitability in Chapter 4 of this thesis during development of a series arc fault detection system for use in the aerospace environment.

2.2 Arc Fault Standards and Test Methods

The review of literature revealed that there are a number of arc fault circuit breaker industry standards and associated test methods. These can be broadly categorised into firstly series arc fault and secondly parallel arc fault test methods where a summary is given below.

2.2.1 Series Arc Fault Test Methods

There are two main series arc fault test methods and firstly in 2004 the "loose terminal" test scenario was presented as part of the SAE AS5692 115VAC 400Hz single phase Arc Fault Circuit Breaker (AFCB) aerospace test standard, which involves the random vibration of a set of ring tongue tag terminals on corresponding loose threaded bolts using a predetermined vibration power spectral density profile [8]. SAE AS6019 covers the test requirements for 28VDC arc fault circuit breakers and uses the same top level arc fault detection test requirements as SAE AS5692, which only covers 115VAC 400Hz systems [8; 58]. This test method was further cited by Potter and Lavado where the purpose of the test method was outlined by demonstrating the effects of localised heating where wire insulation and a plastic circuit breaker housing was damaged as a result of series arcing [35]. Furthermore Li et al present an

implementation of the loose terminal test scenario using a shaker table mounted in an environmental chamber, where the behaviour of the arc in different environments can be determined [59]. The loose terminal scenario is thus a versatile and repeatable test worthy of further research concerning arc faults in high voltage DC systems.

The second series arc fault test method is the drawn arc where Li et al present a method of creating a repeatable drawn arc for experimental purposes using a stepper motor controlled linear actuator, which separates a pair of electrodes conducting a known current at a predetermined velocity, thus drawing an arc [59]. In 2014 Artale et al used a similar technique to Li et al to verify arc fault detection capability and the effect of "nuisance loads" in accordance with ANSI/UL1699 [60].

2.2.2 Parallel Arc Fault Test Methods

For completeness it is necessary to review parallel arc fault test methods. The ANSI/UL1699 specification was released in 2006 and describes test methods for arc fault detection equipment in DC Photovoltaic (PV) circuits under a drawn arc scenario [42]. The drawn arc method described in the series arc fault test methods above is therefore equally applicable to both series and parallel arc fault testing, where the parallel arc fault current levels are significantly higher.

In 2001 Hetzmannseder et al presented three papers illustrating the damage caused by shorting a fused output to ground by cutting through cable insulation using a "guillotine" which created severe arcing [61; 62; 63]. The focus of this research was on simulation of parallel arc faults in residential 120VAC 60Hz, aerospace 120V 400Hz and automotive 42VDC applications. Later in 2004 the guillotine test scenario was presented as part of the SAE AS5692 115VAC 400Hz single phase Arc Fault Circuit Breaker (AFCB) aerospace test standard which involves the short circuiting of a pair of power conductors using a knife blade [8]. Again SAE AS6019 covers the test requirements for 28VDC arc fault circuit breakers and uses the same top level arc fault detection test requirements as SAE AS5692 which covers 115VAC 400Hz systems [8; 58]. Major Lietch et al of the Air Force Research Laboratory (AFRL) demonstrated the effect of a guillotine test on a 115VAC system in their 2006 paper, where significant wire damage and ablation of the shorting knife blade occurs during an uninterrupted guillotine test [64].

Hetzmannseder et al also presented their findings from a dangling wire test in three papers where a live wire was allowed to dangle over a car bonnet resulting in severe and continuous parallel arcing [61; 62; 63]. The resulting arc current was found to cause negligible heating of the 70A series fusing element used in this circuit and thus arcing was allowed to continue unabated. Hetzmannseder et al further presented the results of a wet arc tracking test where a salt water drip is set to drip over two or

more conductors with damaged insulation, and when conduction through the salt water commences this causes heat dissipation which in turn can lead to fire [63]. Similar to the guillotine method, Hetzmannseder et al also presented the saw test where the wire under test is mounted close to a block of metal and a "saw" is used to cut through the wire under test, thus allowing a parallel arc to strike and causing further wire damage and heat dissipation to occur [63].

ANSI/UL1699 presents a carbonised path test method which is used to induce parallel arcing [42]. In 2004 Nemir et al presented the results of a carbonised sample test which shows that significant current can flow during this fault and that the fault can go undetected, ultimately leading to fire in similarity with other parallel arc fault test scenarios [65]. In conclusion there are many methods for inducing parallel arc faults and each of these demonstrates similarly catastrophic results.

2.2.3 Other Test Methods

Andrea presented a repeatable and calibrated arc fault generator in his 2010 paper, where a MOSFET switches a current through the primary winding of a transformer, and the secondary winding is connected across a pair of arc electrodes [66]. When current ceases in the primary winding, the back-EMF generated in the secondary winding causes an arc to form across the pair of arc electrodes, where the controlled switching of current through the primary winding gives a repeatable and calibrated arc. The arcing generated using this method is a great way to understand the physics of electrical arcing and the electrical breakdown process, but this is not a representative arc fault test method for aerospace applications.

Ettling presented a method of recreating glowing contacts in his 1982 paper where two conductors carry power from a domestic supply to a load, where the conductors are clamped to a wooden block [43]. A nail is hammered into the wooden block and the two conductors are positioned such that they each form a point contact with the nail thus encouraging the formation of a glowing contact. The glowing contact did not commence immediately, and instead time elapses before localised heating forms an oxide layer on each conductor such that the contact resistance increases further and a glowing connection forms. This method is similar to the loose terminal series arc fault scenario in the absence of any vibration stimulus, and thus it is of limited use for aerospace applications.

2.3 Behaviour of Arc Faults

2.3.1 DC Arc Fault Behaviour

A number of studies have been carried out on the behaviour of DC arc faults and it was identified during the literature review that papers which provide characterisation

of arc faults often tend to also include a report on the effectiveness of a given arc fault detection scheme. This section contains a review of dedicated DC arc fault characterisation literature only, where any detection-specific characterisation details are included in Section 2.4 covering passive arc fault detection methods.

Scientists and engineers have been carrying out experiments on electric arcs for over a century and in order to understand arc faults it is important to first understand the electrical characteristics of electric arcs. The work of Ayrton focussed on developing a simple static electric arc model and remains widely cited by modern literature. The Ayrton (1902) arc behavioural model is given in Equation (2.1) and describes the static characteristics of a given electric arc [67].

$$V_{arc} = A + B\ell + \frac{C + D\ell}{I_{arc}} \tag{2.1}$$

where V_{arc} is the arc voltage (differential voltage between anode and cathode), I_{arc} is the arc current, A is the sum of the cathode and anode drop (which remains constant with arc length), B is the column voltage gradient, C and D model the arc's non-linear characteristics, and ℓ represents the arc length. Additional work has been carried out on arc modelling and this is covered in more detail in Chapter 3.

Strobl and Meckler demonstrated that to achieve stable arcing there is a minimum arc power requirement and this was calculated from the Ayrton equation. Arc extinction was found to occur during the condition presented in Equation (2.2) [68].

$$V_{src} > A + \sqrt{A^2 + 4R_{load}C} \tag{2.2}$$

where V_{src} is the source voltage, A is the cathode and anode drop, C represents the arc's non-linear characteristics and R_{load} is the load resistance.

Strobl and Meckler also presented spectrograms of both the arc current and arc power waveforms for numerous drawn arcs in circuits with DC source voltages of 35V, 40V and 45V where it was demonstrated that high frequency content is in indication of arc instability [68]. The corresponding time domain arc current waveform showed a very fast reduction in arc current during arc strike, which corresponds to broadband noise in the frequency domain. Strobl and Meckler identified that non-linear load behaviour and 270VDC source voltage scenarios require further work.

Naidu et al make the observation that during a series arc, since the voltage seen at the load drops by the arc voltage, the corresponding reduction in current can be calculated in accordance with Equation (2.3) [69].

$$I_{arc} = \frac{V_{in} - V_{arc}}{R_{load}} < I_{load} = \frac{V_{src}}{R_{load}} \tag{2.3}$$

where I_{arc} is the current through the series arc fault, V_{src} is the source voltage, V_{arc} is the arc voltage, R_{load} is the load impedance and I_{load} is the load current in the absence of an arc fault.

Figure 2.1 shows exemplary series arc fault time-domain electrical behaviour in a 28VDC system where the series arc fault current reduces by 50% with respect to the nominal 4A resistive load current during series arcing. The arc voltage (red) indicated in Figure 2.1 is 15V for a 4A resistive load, which is approximately half of the supply voltage, and thus from Equation (2.3) the arcing current (yellow) is approximately half of the nominal load current. Conversely Figure 2.2 illustrates parallel arc fault behaviour in a 28VDC system with a high impedance load where parallel arc fault current peaks exceed 50A and arc voltage is in the order of 20V during parallel arcing.

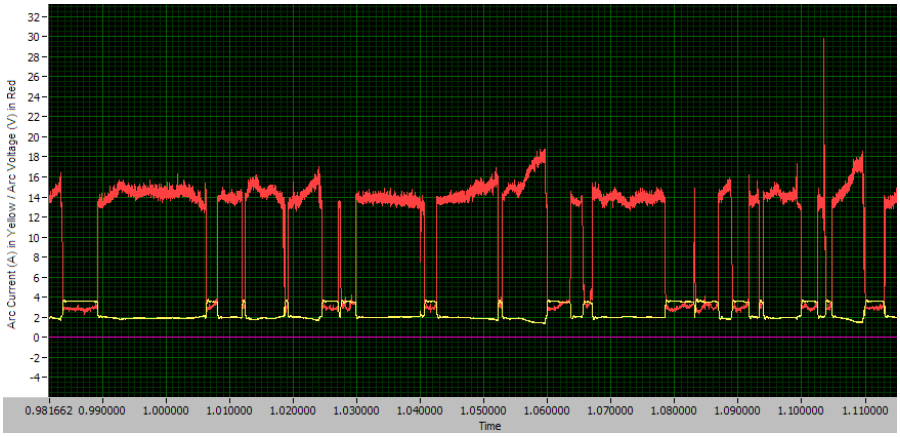


Figure 2.1: An Example of 28VDC Loose Terminal Series Arc Fault Behaviour

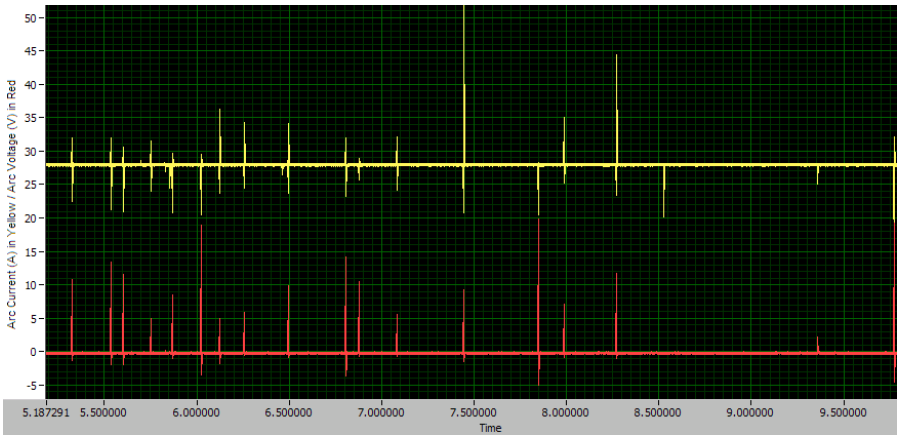


Figure 2.2: An Example of 28VDC Guillotine Parallel Arc Fault Behaviour

It is clear from the work of Allen et al in their ageing aircraft conference paper that in 28VDC circuits arcs regularly quench since the arc voltage is the same order of

magnitude as the source voltage [70]. Series arcs quench rapidly in the loose terminal scenario, but the arc is still present for a short duration, and while this may not be a threat in an inert environment these repetitive arcs can lead to ignition of hydraulic fluid or other contaminants in the airframe.

Yao et al confirmed that a rise in source voltage results in a smaller reduction in current for a given pre-arc load current [71]. It was also observed that arc voltage has a loose relationship with supply voltage and a strong correlation with load current. Yao et al determined that arcs exhibit a high impedance at high frequencies and application of wavelet packet analysis reveals high frequency content caused by random / chaotic behaviour of arc. It is proposed that current variation could be used for arc fault detection purposes and this is covered in Section 2.4.4.1 of this review.

Gattozzi et al propose that constant gap arcs can be represented by the Ayrton model, but fluctuations of ideal conditions at the arc electrodes cause premature arc extinction of the experimental arc compared with the model [72]. The movement of the arc electrodes causes complexities not covered by the Ayrton model other than for slow separation of electrodes. Gattozzi et al model this instability by considering a constant voltage source connected through an resistor-inductor circuit to a series arc, where not only static V-I arc characteristics are observed but also how the rate of change of arc current creates variation in arc voltage, thus explaining the high impedance at high frequencies observed by Yao et al [71; 72]. A plot of V_{arc} vs I_{arc} vs $\frac{dI_{arc}}{dt}$ was produced from experimental drawn arc data which validates this approach.

Spyker et al of the Air Force Research Laboratory (AFRL) highlight the importance of series arc fault protection in 270VDC systems in their 2005 paper, since this level is prevalent as the distribution voltage of choice in new aircraft including the United States Air Force F/A-22 and Joint Strike Fighter (JSF) platforms [73]. Spyker et al later design a series drawn arc generator using two arc electrodes mounted on a linear actuator arrangement allowing arcs of different lengths to be drawn. A 270VDC power supply is used to deliver power through the arc gap into a resistive load, and a current transformer and oscilloscope are used to measure the arc current during the arc. Experimentation with the common electrical conductors copper and aluminium reveals that the copper electrodes create a blue-green arc and aluminium electrodes create a white-blue arc. The power spectral density plot of the arc current waveform shows significant energy in the range 1kHz through 100kHz across the range of data sets, and while spectral peaks exist at specific frequencies, these are inconsistent between data sets. It is demonstrated that increasing arc length in circuits with a fixed resistive load results in a reduction in arc current due to the increase in arc voltage and thus a reduction in voltage supplied to the resistive load. For short arcs with currents above a given current threshold it is demonstrated that arc voltage remains constant and therefore arc power becomes proportional to arc current. The

effect of pressure on drawn arcs is investigated where arc power vs gap length is consistent at 1,000ft, 25,000ft and 40,000ft, however the voltage at which the given arc extinguishes varies significantly.

2.3.2 AC Arc Fault Behaviour

The behaviour and modelling of AC electric arcs is a research area which has been studied at length. Browne presented models for predicting AC arc behaviour near current zero where the energy balance equations of Mayr and Cassie were used [74]. This work demonstrated that the V-I characteristics of the arc during strike and extinction are not identical since the temperature and conditions of the arc change during the half-cycle leading to highly dynamic behaviour.

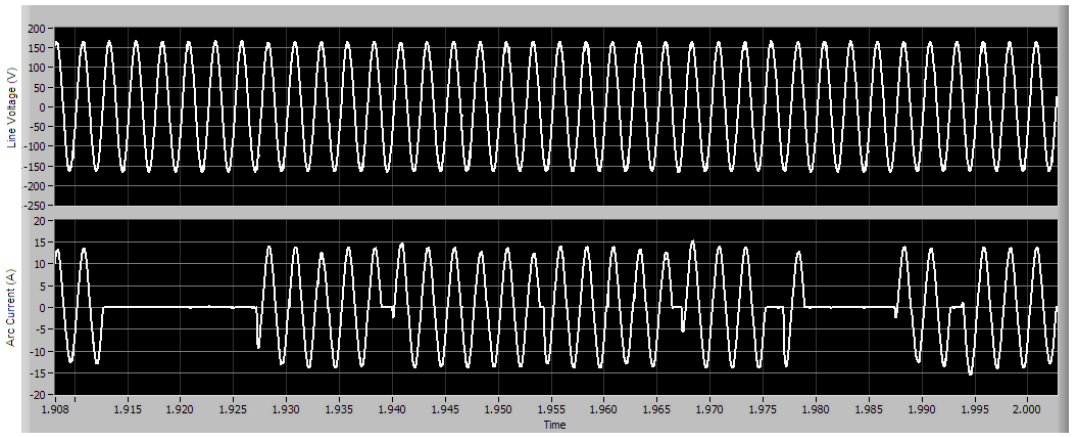


Figure 2.3: An Example of 115VAC 400Hz Loose Terminal Series Arc Fault Behaviour

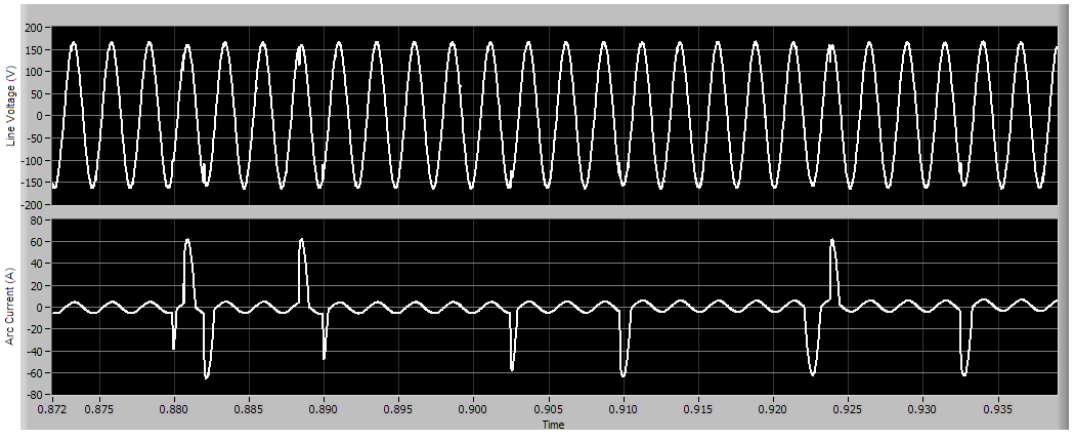


Figure 2.4: An Example of 115VAC 400Hz Guillotine Parallel Arc Fault Behaviour

Figure 2.3 shows exemplary series arc fault behaviour in a 115VAC 400Hz AC system where the series arc fault current reduces with respect to the normal 12.5A resistive

load current during arcing. The unstable nature of arcing can result in missing current half-cycles as indicated in Figure 2.3. Conversely Figure 2.4 illustrates parallel arc fault behaviour in a 115VAC 400Hz AC system with a 10A nominal resistive load, where parallel arc fault current half-cycle peaks can exceed 60A.

In 1969 Harry presented AC series arc fault behaviour which showed that at the start of a given half-cycle the arc voltage has to increase to a voltage sufficient to break down the arc gap, and when breakdown occurs current begins flowing to the load and the arc voltage falls to 15-20V for short arcs [75]. As the end of the half-cycle is approached the arc current reduces and the arc voltage increases until the arc can no longer be sustained and finally the arc becomes extinct. The process repeats and leads to the characteristic current waveform where current doesn't start flowing for the first few degrees of the half-cycle.

Later in 2009 Müller et al presented an artificial low current arc fault for pattern recognition in low voltage switchgear where a small resistor is deliberately destroyed in order to strike an arc [76]. These experiments correlate with the results presented by Harry, where it is important to note that the arcs quench at the current zero crossing when there is a low voltage across the arc. This contrasts with DC arcs where the arc continues unabated until the power source is removed. Müller et al concluded that it is difficult to generate stable arcs for currents under 1000A at 115VAC 60Hz, that breakdown voltage depends strongly on remaining charge carriers in the arc plasma channel (heating and evaporated copper), that inductive arcs are easier to maintain, and finally that arc reignition depends strongly on arc current amplitude where higher currents result in a shorter time to reignition after zero-crossing.

Müller et al further studied AC arc behaviour in their 2010 paper where their time domain analysis was complemented with a frequency domain analysis of the AC arc current and it was determined that the magnitude of the third, fifth and seventh harmonics are elevated during arcing [34]. It was later discussed that loads such as elevators created similar spectral content, and therefore nuisance trips are a potential risk. Very high harmonics in the range 250Hz through 2kHz were also seen in the arc current, but again these frequencies also appear in representative load current waveforms. Spectral density above 2kHz was also observed but there was no spot frequency identified which classifies AC arcing behaviour.

Sun and Gao presented an analysis of arc current rate during arcing in their 2011 paper and it was found that the rate of change of arc current $\frac{dI_{arc}}{dt}$ is very fast due to the electric breakdown event and is only limited by power supply source impedance and circuit inductance [77]. Sun and Gao continued on to use fractal analysis techniques to characterise the rate of change of current.

Finally in 2014 Carvou et al presented a study on drawn arcs produced using a linear actuator to separate the arc electrodes in 110VAC 60Hz and 220VAC 50Hz circuits [78]. It was demonstrated in the 220VAC system that a larger number of arcs were present compared with the 110VAC system due to the additional potential which aids breakdown following the arc quench during the current zero-crossing. In conclusion arc faults are more prevalent in both high voltage DC and AC systems and need to be detected such that remedial action can be taken.

2.3.3 Influence of Inductive and Capacitive Loads

Literature surrounding the influence of inductive and capacitive loads on the behaviour of arc faults is somewhat limited and is of particular interest, given the desire to understand how fault location and system impedances change fault behaviour.

Suhara presented a paper in 1991 covering the behaviour of break arcs in inductive circuits [79]. Suhara experimented using a DC voltage source connected through a series resistor-inductor circuit and in turn through a drawn series arc, where arc voltage and current were measured and recorded. It was demonstrated that the addition of energy storage in the form of inductance improved the stability of the series arc circuit and as such allowed arcs to strike and burn stably at lower pre-arc load currents (<1A). Series arc faults in aircraft electrical power distribution systems are therefore an issue even for lower load current levels since wiring inductance introduces significant energy storage allowing stable series arcing.

Müller et al presented a paper in 2011 where the influence of capacitive and inductive loads on the detectability of arc faults in AC electrical systems was studied [80]. The main conclusions from this study were that the introduction of inductive loads influences both the time and frequency domain characteristics of the arc current waveform during series arc faults. In the time domain the time until re-ignition is reduced or the arc doesn't extinguish at all, and in the frequency domain the amplitudes of high frequencies are considerably reduced and there is little influence on lower frequencies (<1kHz). Müller et al note that capacitive loads are expected to have an effect on arc current, however their series arc fault tests with 20μF capacitors in the test circuit showed little influence on time or frequency domain behaviour and thus further work was recommended. They finally concluded that the position of a given arc fault within a system, and therefore the effects of system capacitance and inductance, changes the time and frequency characteristics of the fault and thus influences the detectability of arc faults. The work of Müller et al only addresses AC fault behaviour under a range of inductive and capacitive scenarios, and DC faults remain unexplored. It also does not produce a satisfactory conclusion regarding the effect of capacitance on system behaviour, and given the influence of inductive loads on detectability, this is an area which requires further work.

2.3.4 Glowing Connections

An interesting discovery was made during the review of literature which is that arc faults are not always the cause of electrical fires, and in fact "glowing connections" have been of interest for some time and are primarily of concern with domestic electrical installations. A glowing connection is caused where a high impedance electrical interface appears in electrical cabling, usually where broken wires contact each other or loose connections exist which in turn cause points of high current density at the interface leading to glowing connections. In 1977 Meese and Beausoliel carried out an exploratory study of glowing connections with the most relevant conclusion being that glowing electrical connections may exist for protracted periods of time without breaking the electrical circuit and without introducing a significant series voltage drop, and therefore they have little effect on load performance and typically remain undetected [81]. In similarity with series arc faults "glowing connections" will not operate fuses or circuit breakers since current through the fault cannot exceed the nominal load current. It was also concluded that glowing electrical connections may occur over nearly the entire range of currents likely to be present in residential branch circuits, which are not dissimilar to aerospace current levels.

Literature addressing glowing contacts is somewhat sparse and thus much later in 2007 Zhou and Shea carry out a characterisation study on glowing contacts using optical emission spectroscopy in order to understand the physical mechanisms involved in the typical glowing contact scenario [82]. A micrometer was used to separate two copper wire conductors in a controlled manner where a current was fed through the conductors from an AC power source. Voltage across the contacts, current through the contacts and high speed video camera footage was recorded using a data acquisition system in order to correlate physical behaviour of the glowing contact to electrical behaviour during the test. The voltage across the glowing contact was in the order of $6V_{pk-pk}$ with a $7.5A_{rms}$ current presented in the conductors which resulted in a hazardous power dissipation of $15.8W_{rms}$. This fault is therefore fundamentally different from a series arc fault since a typical arc voltage with a small electrode separation between copper electrodes in standard conditions is 15V.

Later in 2010 Urbas made a study on low current ($<1A_{rms}$) glowing contacts within electrical connectors containing spring contacts where he determined that vibration is initially required in order to create a glowing connection or series arc scenario, however after a number of vibration cycles the sustained arcing creates an oxide layer which allows a glowing contact to form when vibration ceases [83].

Although glowing connections could be regarded as irrelevant to series arc fault detection, the author wishes to note that while the vibration within the aerospace environment would most likely cause broken wires and loose connections to form series arc

faults during flight, when the aircraft is on the ground and running on ground power in the absence of a vibration stimulus these faults could form “glowing connections” which dissipate power and can go undetected. This phenomena was observed both by Urbas and by the author during experimentation with the loose terminal scenario presented in Appendix A, where detection of “glowing connections” is difficult due to their minimal impact on normal load operation.

2.4 Passive Arc Fault Detection Methods

This section reviews passive arc fault detection methods where Figure 2.5 highlights both properties of electric arcs for arc fault detection, and additional considerations for the evaluation of arc fault detection techniques.

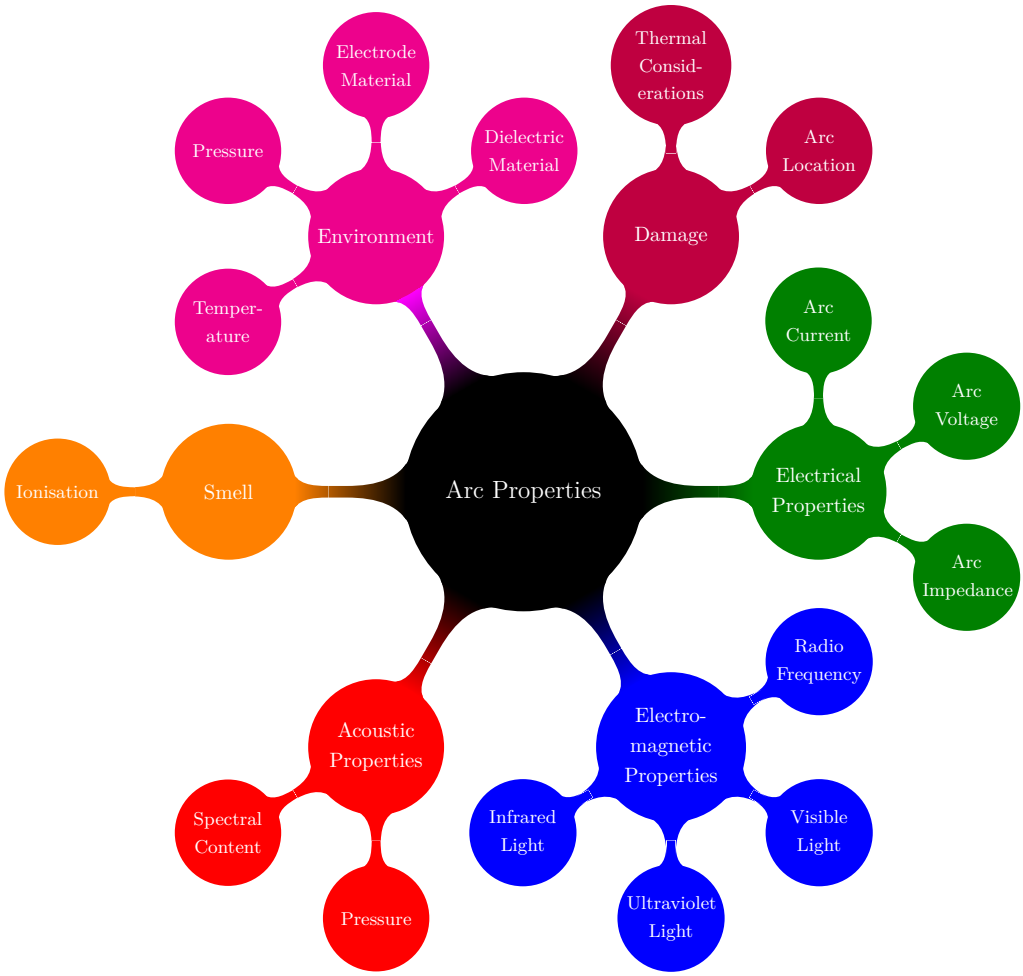


Figure 2.5: Basic Properties of the Electric Arc

2.4.1 Acoustic (Audio and Ultrasonic)

Electric arcs and arcing faults generate pressure waves and literature surrounding the acoustic radiation properties of the electric arc mainly analyse the risk of arc pressure

waves from a personal health and safety perspective. Drouet and Nadeau became motivated to study pressure waves created by electric arcs in 1979 with a particular focus on AC arcs within large substations, following the collapse of a building housing a large substation due to an arcing fault [84]. The arc currents tested were in the range 10A through 80kA with arc lengths varying from 8mm to 15m burning in air for up to one second. The results showed that the amplitude of the pressure wave generated by a given arcing fault was directly proportional to the rate of change of the electrical power in the arc. Although the range of currents and arc lengths covered in this literature is typically greater than that experienced in an aerospace electrical power scenario, this paper demonstrates the acoustic properties of arcs concisely.

A decade later there was further interest in pressures developed by arcs in the context of health and safety, with particular interest in flash burns caused by electric arcs. Lee explores the relationship between arc pressure and distance to the arc at different power levels, noting that intuitively there is greater pressure close to the arc and the pressure experienced falls proportionally to the distance to arc centre [85].

Moving forward a further decade to 1997 and the first research into acoustic-based arc fault detection is carried out by Phelps for General Atomics. Phelps' scheme uses detection of both sound and electromagnetic emissions from the arc, where sound signals 40dB to 50dB above background noise are observed, and low radio frequency (HF) electromagnetic noise levels of 20dB to 60dB above the noise floor are recorded in an electrically noisy nuclear reactor [86].

In 2000 Wactor et al investigated the acoustic properties of arcs within switchgear and although their paper is interesting for scenarios where the arc is enclosed in a box, the focus of this thesis is on arcs that occur within aircraft wiring, not within enclosed aircraft equipment specifically and therefore this paper is of limited use [87].

Shortly after in 2001 Maroni et al of Schneider Electric Industries published the first paper which explicitly focussed on series arc fault detection in switchboards [88]. The paper states that:

> *"In switchboards, a conduction fault almost always degenerates into a series arc, then into a parallel arc. A study performed in 1998 showed that series arcs naturally emit ultrasonic waves into the busbar."*

The presence of ultrasonic waves in the busbar gives a good basis for arc fault protection providing that the intended environment for the detection system does not suffer from acoustic noise at the frequencies of interest. Any interference from external sources presents the opportunity for a nuisance trip. The natural rigidity of busbars lends itself to an acoustic based detection scheme and therefore the possibility of exploiting this scheme on a flexible semi-rigid wire-based distribution systems could be investigated.

In 2003 Tallman et al were awarded Patent US 2003/0169051 A1 regarding the use of an RF and acoustic arc fault detection/location system for detection of arcing in domestic and industrial applications. The acoustic detection element provides coverage of audio and ultrasonic frequencies, although disappointingly specific frequencies have not been identified [89].

Yang et al also investigate "arc sounds" in their paper of 2008 regarding arc fault detection and protection based on chaos [90]. For their experiments a fibre optic microphone was used to capture arcing sounds, since condenser microphones suffered from electromagnetic field interference from the arc. Arcs were generated from supply voltages up to 5kV and the results showed that a steady state wave spectrum due to arcing in the range 4kHz-7kHz was present in the recorded signals. Yang et al then used a Duffing oscillator system to detect the chaotic nature of the arc faults present in their system.

Similarly to Yang et al, Beihoff et al were granted Patent US 5,185,687 A in 1993 for a chaos sensing arc detector, where this patent discusses hardware level implementation as opposed to the physics behind chaotic arc behaviour [91]. The patent discusses an "arc discrimination circuit" which produces an "arc indicative signal" in response to a "random chaotic pattern" generated in a B field sensor which is coupled to the circuit under test, although the statistical nature of the "random chaotic pattern" remains undisclosed.

Glowing contact detection by means of acoustic detection has also been attempted by Zhou et al in their paper of 2009 which used an acoustic transducer attached to one end of the cable feeder under test to detect potential series faults. Monitored acoustic signals from the glowing connection are prominent at the second harmonic of the AC supply voltage, although the paper focusses on signals in the ranges 20Hz-70kHz and 100kHz-700kHz, and the attenuation of associated cables per unit length [92]. This is a comprehensive study which also covers the behaviour of wire splice connections including stud and bus splices which lead to attenuation of the glowing contact acoustic signal.

Earlier in 2006 Zhou et al were awarded Patent US 7,148,696 B2 which presents a method where acoustic sensors can be used to detect series and parallel arc faults, by monitoring specific spectral content from acoustic sensors [93]. This reference indicates an ability to detect faults in AC distribution systems where power is delivered using sinusoidal voltage sources; in this scenario during an arc fault the acoustic detector would detect the arc fault frequency signature along with the power supply modulation frequency and harmonics. Further work is thus required to determine the acoustic signature of DC arc faults.

Of particular interest to aerospace applications is the threat of acoustic noise which can be at sound pressure levels up to 165dB across a frequency range from 150 through 2500Hz in accordance with MIL-STD-810G Test Method 515.6 [94]. Any acoustic sensor used for arc fault detection must therefore be capable of surviving operation at this sound pressure level, yet be capable of detecting the acoustic signature of the given series arc fault and therefore dynamic range becomes a dominant design requirement.

The literature shows that the acoustic properties of arcs are potentially useful for arc fault detection. However, the intended operating environment for the arc fault detector could preclude the use of acoustic sensors where high levels of acoustic noise may be present, and this could limit the practical realisation of this technology.

2.4.2 Visible and Ultraviolet Light

It is known that electric arcs emit visible and ultraviolet light radiation, and this is the very property that gave the electric arc its name. The characteristic arc shape of the electric arc can be seen when drawing an arc between horizontal electrodes and is as a result of air convection due to the heating effect of the arc. Arcs can be clearly observed from arc welders and were originally used as a means for creating light intentionally in early "arc lamps". Early literature from Steinmetz describes the suitability of the electric arc for lighting purposes, and states that the radiated spectrum of light is that same as that of the gas in which the arc exists [95].

In 2009 Caggiano was granted Patent US 7,580,232 B2 which presents an arc fault detection system and method based on optical detection of ultraviolet light which emanates during an arc flash [96]. This detection scheme is aimed at detecting phase-to-phase arc flashes in AC distribution systems. This method utilises several ultra-violet sensors in a distribution cabinet, along with several radio-frequency sensors. These sensors are fed into a processing unit which compares the current situation to a pre-determined set of characteristics and determines whether an arc is present thus providing trip indication. Optical sensors can be overloaded or desensitised with high ambient light levels and therefore these sensors are best deployed in a sealed low-light environment and not in an open electrical power distribution system.

In 2012 Das presented a method of detecting arc flash events within arc fault detection relays by using long unclad fibre optic sensors in order to gather the high light intensity associated with an electric arc [97]. Das claimed that the arc flash can generate light intensities in the range 100,000 to 1,000,000lx at a distance of 3m. This is substantially greater than that of a typical camera flash which produces typically 234,000lx at only 0.45m. Dynamic range of the visible light spectrum at the point of sensing is therefore unlikely to be an issue in an aerospace application.

It can be concluded from the literature that the limitation for use of a visible or ultraviolet based arc fault detection scheme here is that the electrical distribution cabling can run for miles within a typical civil narrow-body aircraft and thus distributed light sensors or fibre optic sensors would need to provide coverage of the complete electrical system, where this would incur additional weight and cause an additional aircraft installation and maintenance overhead.

2.4.3 Ionisation

Land et al presented a method of arc fault detection in naval switchboard applications motivated by a number of arc faults in battery driven submarines during World War II [98]. Land et al also suggest that smoke and fumes emitted from overheated connections could be used for arc fault detection purposes. However, studies with commercial gas detectors based on semiconductors and heated beads had the potential to cause nuisance trips since they reacted to paint fumes, diesel generator fumes and other gases which are likely to be encountered on a ship. Long-term stability and calibration were also found to be problematic.

Land et al later developed a radioactive ionisation chamber with an Americium-241 source for use as a Thermal Ionisation Detector (TID) thus providing continuous thermal monitoring which yielded good arc fault detection performance compared with previous thermal imaging systems. Land et al were awarded Patent US 6,292,105 B1 in 2001 covering the disclosure of their Thermal Ionisation Detector (TID) design [99], and a MIL-SPEC qualified variant of the TID was created.

Detection of ionisation within aircraft electrical power distribution systems is a possibility, but in the aerospace environment the location of the fault could be widespread over a large area of the aircraft and this arc fault detection methodology does not provide the location of the fault down to a specific circuit breaker or SSPC output and is therefore of little value during flight.

2.4.4 Electrical

2.4.4.1 Time Domain Methods

There is a significant volume of literature describing time domain methods for arc fault detection, which is the fundamental starting place to build an understanding of the state of the art in passive electrical arc fault detection methods.

In 2011 Rabla et al investigated an vibration-induced series and short circuit contact-induced parallel arc fault detection approach using an FPGA evaluation board in aerospace 28VDC, 270VDC and 115VAC 400Hz, automotive 48VDC and domestic 110VAC 60Hz and 230VAC 50Hz systems [100]. Simple Eulerian differential detection

and cumulative sum approaches were taken to detection, where both techniques are aimed as detecting fast steps in arc current and circuit breaker output voltage as an indication of arcing. This approach is very simple but is open to nuisance tripping in the presence of load step events. Rabla et al interestingly use a similar FPGA-based approach to arc fault detection using Wavelet decomposition which is covered in Section 2.4.4.2.

In 2012 Yuan et al presented a method of detecting drawn series arc faults in DC electrical power systems with source voltages from 0-300V and currents as high as 30A [101]. It was further determined that during arc initiation a small positive going voltage pulse appeared at the output of the power source. In the event that the arc quenches, a larger positive going voltage pulse appears at the output of the power source. Yuan et al do not explain the cause of this behaviour, however the author believes that this is either due to poor load regulation in the power supply or due to parasitic inductance in the output of the power supply which causes a voltage transient during any step in arc current. Yuan et al also note following FFT analysis of the arc current waveform that there is significant energy in the range 10-100kHz which could form the basis of arc fault detection, although the root cause of this spectral energy is not discussed.

Lezama et al presented a method of arc fault detection in 230VAC systems in their 2013 paper, using an FPGA prototyping board [102]. This solution uses five parameters for arc fault detection, current magnitude analysis to observe the RMS arc current variation between successive periods, low frequency (<1kHz) frequency analysis, 5^{th} harmonic current analysis (250Hz) using a bandpass filter, variation voltage analysis which measures average voltage across each half cycle to detect voltage variations due to parallel arc, and high frequency voltage analysis (1-20kHz) using a bandpass filter. Combining these techniques it is possible to detect and differentiate series and parallel arcs where experimental verification of detection capability in the presence of series arcing confirms the functionality of this algorithm. Testing in the presence of a non-linear load in the absence of series arcing shows that this scheme is robust against nuisance trips created by non-linear load behaviour, however this scheme is not transferable to a DC arc fault detection application.

Faifer et al presented a method of detecting loose terminal induced series arc faults in aerospace 28VDC systems in their 2013 paper [103]. It is noted that arc ignition can be easily identified by a sudden decrease in arc current, which in turn can be easily detected by analysing the rate of change of the arc current signal and therefore if the derivative of the arc current signal falls below a tuned negative threshold, this indicates that an arc is likely to have struck. Faifer et al also comment that numerical differentiation is strongly influenced by system noise and therefore a high pass filter is

a more sensible approach detection. For this aerospace-specific application MIL-STD-461E [104] was considered and it was determined that load currents should feature negligible energy above 1kHz and therefore this is a suitable cut-off frequency for the high pass filter. The author suggests that this assumption may be optimistic due to noise contributed by the interaction of the wider electrical system. Faifer et al also go on to calculate arc power and thus energy dissipated based on arc current and an assumption of arc voltage, where an energy threshold can be implemented as a series arc fault trip level.

Ragsdale was granted patent US 5,280,404 A in 1994 which describes a method of arc fault detection where the load current is sensed, filtered and amplified [105]. Any breaks in current trigger a latch circuit and trip a solid state relay, where the trip can be reset by pressing a button. This is a passive detection approach and will be subject to nuisance trips.

Zuercher and Tennies were granted patent US 5,561,605 in 1996 for their method of arc detection in AC electrical power distribution systems using load current and line voltage monitoring [106]. The voltage monitoring uses a harmonic notch filter to filter out the power line frequency and then produces a running sum, which is thresholded and used as one of the conditions required to trip a circuit breaker. The current monitor signal is also subject to a harmonic notch filter, and a synchronous summer where the output of the summer feeds into a complex condition checker using current average, peak to average, two quiet zones >1.56ms, a quiet zone <9.17ms and a null zone <1.24ms, where justification of these conditions is not provided.

Russell was granted patent US 5,659,453 in 1997 for his arc burst pattern analysis fault detection system [107]. This method is targeted at AC arc detection systems, where discontinuities in the load current waveform during the rising of the load voltage are used as the arc fault discriminator. This behaviour is not seen in DC systems and therefore this arc fault detection solution is limited.

Elms and Schlotterer were granted patent US 5,835,321 in 1998 for their arc fault circuit breaker implementation [108]. The patent describes an arc fault detection method for AC power systems using current and voltage signals in the frequency range 3kHz to 20kHz, so as to avoid interference from power line communications systems. This implies that power line communications systems would interfere with this passive detection approach, therefore the approach may suffer with nuisance trips due to other interference sources. The scheme also monitors the zero crossing point in the current waveform such that harmonic content can be related back to the phase of the current signal.

Schmalz was granted patent US 6,300,766 B1 in 2001 for his envelope-type AC parallel arc fault detector which is sensitive to the amplitude of the arcing current [109]. This

scheme uses a two-stage envelope detector to capture both fast and slow current increases before analysing the randomness of the signals and generating a trip signal.

Haun et al were granted patent US 6,259,996 B1 in 2001 for their arc fault detection system which functions by monitoring broadband noise components of the arc current signal within 120VAC distribution systems [110]. The arc current signal is taken and bandpass filtered at 35kHz and 70kHz where the presence of a energies over a given threshold at these frequencies triggers a digital counter to provide an indication that arcing is occurring. In addition to this, the arc current signal is integrated firstly to detect zero-crossings of arc current, which are used for timing purposes, and also to detect missing half cycles, which again are indicative of series arcing behaviour. This scheme uses the physical interaction between the cyclic nature of the AC voltage and the arc in order to provide detection capability. Scott et al were granted a similar patent US 6,625,550 B1 in 2003 for their method of detecting arc faults in aerospace electrical distribution systems by monitoring electrical current flow in a given distribution circuit, and extracting broadband noise signal components [111]. The system analyses these signals and produces a trip signal which may be used directly or indirectly to trip a circuit breaker or other interruption device. Furthermore Wong et al were also granted patent US 2003/0072113 A1 in 2003 for their arc fault detection system for AC electrical distribution systems [112]. The main body of the detector relies on the detection of broadband low frequency noise, which has been classified as energy at 20kHz, 33kHz and 58kHz. The physical rationale behind the filter value choices in each patent has not been presented and appears highly empirical in nature.

Brooks et al were granted patent US 6,195,241 B1 in 2001 for their arc fault detection system which monitors the rate of change of arc current in an AC breaker and generates a pulse each time a predetermined rate of change of current is exceeded [113]. The pulses are then filtered to eliminate a signal or pulse which falls outside a selected frequency range. A rolling window is then applied to the pulses and if the number of pulses in the given window exceeds a predetermined threshold, then the circuit breaker is tripped.

Macbeth et al were granted patent US 2001/0033469 A1 in 2001 for their arc fault detection technique which uses a current transformer to monitor load current from a circuit interrupter, and identifies the signature patterns of arc fault noise while rejecting arc mimicking noise from normal load behaviour [114]. In 2002 Macbeth and Packard were granted patent US 6,373,257 B1 for their arc fault circuit interrupter scheme which uses a current transformer to sense the derivative of arc current flowing through a circuit breaker, and two peak detectors to detect positive and negative current step transients through the arc [115]. Arcing is indicated in the event that a positive and negative step occur within a predetermined period of time. This scheme is simple however noisy load currents such as brushed AC motors, which produce

periodic arcing, are likely to trigger this scheme and cause nuisance trips. Later in 2002 Packard and Romano were granted patent US 6,421,214 B1 where the existing arc fault circuit interrupter design was combined with a ground fault detection circuit [116]. Macbeth and Packard were also granted patent US 2002/0033701 A1 in 2002 for their arc fault circuit detector device detecting pulse width modulation (PWM) of arc noise [117]. This patent begins by stating that when an arc fault occurs, there is a step in current followed by broadband arc noise caused by fluctuations in the arc column resistance. The scheme works by detecting high frequency noise on the load current waveform, and producing a PWM signal whose length is equal to that of the broadband arc noise. The PWM pulses are integrated and a trip signal is produced which cuts power on the affected circuit interrupter.

Rae was granted patent US 6,388,849 B1 in 2002 for his arc fault detector design which can be integrated into circuit breakers [118]. This patent describes a method of arc detection in AC electrical power distribution systems using current monitoring where the arc current signal is instantaneously averaged and since any deviation in the average current during a given half-cycle is indicative of an electric arc, the system also uses a step current detector which identifies fast changes in current which occur during arc strike to trigger monitoring of the current averaging circuit, and in turn to provide a trip to the circuit breaker. Active loads may feature fast current spikes and therefore this scheme is only useful in very specific circumstances. Kim et al addressed this issue and were granted patent US 2002/0085327 A1 in 2002 for their similar method of arc fault detection, where load current is detected and integrated allowing harmful arcs to be differentiated from load transients since large signals are integrated and detected and short signals generated by the start-up of electronic devices are rejected thus preventing nuisance trips [119].

Alles et al were granted patent US 6,525,918 B1 in 2003 for their adaptive arc fault detection and smart fusing system which firstly monitors arc current to determine if the current is over a predetermined value [120]. If the current is over a predetermined value this is an indication that a parallel arc is present in the system. If the current is under the predetermined value, and the current change is outside a predetermined "guard band" this is indicative of normal inductive or resistive arcs. If the current change is outside the predetermined "guard band", the arc duration is outside another predetermined guard band, and the current decay rate or current change is over a given percentage, then an arc is detected. It is clear that this process is complex and uses multiple time domain properties to classify arc behaviour, which allows the designer to reject nuisance trips due to normal load behaviour.

Zuercher et al were granted patent US 2004/0027749 A1 in 2004 for their arc fault detection solution for DC electrical systems [121]. The first concept is to measure load current and load voltage, where the presence of the series arc fault in the load

feeder cable creates a step reduction in both load current and voltage thus indicating that arcing is present in the system. A second concept is that arcing can be indicated if following the initial drop in current, arc current and voltage does not return to the pre-arc levels. The third and final concept is that following the detection of a step decrease in load current, further indication of arcing can be gained if there is a drift in load current either upward towards a short or downward toward and open circuit. Guo et al were granted a similar patent US 6,683,766 B1 in 2004 for their DC arc detection and prevention circuit and method which functions by detecting negative steps in the arc current and subsequently switching off power to the load using a solid state switch circuit in order to quench the arc and thus limit the threat imposed by the arc [122].

Macbeth and Richards were granted patent US 6,972,937 B1 in 2005 which describes a method of arc detection in AC electrical power distribution systems using current monitoring [123]. The current monitor signal is compared against a two-stage threshold and is also compared against a predetermined arc fault signature. If an arc fault is detected, there is a response mechanism to cut power to the arc.

Hale et al were granted patent US 6,943,558 B2 in 2005 which describes a method of detecting and locating damaged conductors [124]. The arc fault detector features at least one controller per solid-state switch output. Each slave node features voltage and current monitoring, and an associated software detection algorithm. The details regarding the detection algorithm suggest that this scheme is a simple overcurrent / overtemperature detector with little resistance to nuisance trip behaviour caused by electrical system noise and transient load behaviour.

Khan and Critchley were granted patent US 7,023,196 B2 in 2006 for their three phase AC arc fault detection system where the voltage on each phase is low pass filtered and full wave rectified, and compared with a set threshold [125]. If either the three signals fall outside of the specified thresholds for a predetermined time period then a fault is flagged. It is therefore a clear advantage with three phase systems that fault detection is somewhat simpler due to the availability of more information with which to discriminate systems faults.

Kilroy and Oldenburg were granted patent US 2007/0133135 A1 in 2007 which shows a method of DC arc fault detection as part of a solid state circuit breaker, based on analysis of the arc current waveform [126]. The scheme here identifies a parallel DC arc event when the difference between a maximum signal value and minimum signal value exceeds a threshold. The scheme also determines average signal values in order to detect DC series arc events in response to the difference between the average values exceeding a predetermined threshold, in similarity with the technique described by Rae [118].

Lazarovich et al were granted patent US 7,177,125 B2 in 2007 for their method of arc fault detection based on comparison of an SSPC load current to a predefined load signature [127]. If the SSPC load current deviates from this predefined signature, the arc fault detector creates an arc fault indication signal to an SSPC which in turn provides protection against arc faults.

Restrepo and Staley were granted patent US 7,492,163 B2 in 2009 aimed at arc fault detection in AC power distribution systems using both zero crossing and broadband spectral analysis of the load current to determine whether an arc is present [128]. Since the characteristic monitored here is the broadband nature of the load current waveform, the system could be used for both series and parallel arc fault detection. The system shows that the output of the system would trip a circuit breaker to cut power to the arc.

In conclusion it is somewhat simpler to detect AC arc faults compared with DC arc faults, and the majority of literature does not correlate the seemingly empirical detection classifier with physical arc parameters thus bringing into question the robustness of all the passive electrical arc fault detection schemes outlined in this section.

2.4.4.2 Frequency Domain Methods

In the course of compiling this literature review it was determined that arcs generate wide bandwidth electromagnetic radiation. RF signals are present both in the form of radiation and currents present in the arc current waveform. Whilst there is significant literature on the behaviour of RF currents flowing through the arc and a number of associated arc fault detection systems based on this behaviour, interestingly there is limited literature on small-scale RF radiation behaviour in arc faults.

In 1994 Ham and Keenan were granted patent US 5,373,241 for their broadband RF based arc fault detection scheme using an inductive current clamp to detect RF currents flowing within a given power cable [129]. The input current signal is amplified and high pass filtered before finally being frequency mixed with a wide band noise generator in order to reject narrowband interference sources. This scheme is hardware intensive and would be difficult to implement. However with the advent of fast Analogue to Digital Converter (ADC) technology, which has enabled Software Defined Radio (SDR), it is likely that this implementation could be simplified into a complex logic device.

Dollar was granted patent US 5,590,012 A in 1996 for his RF-based arc fault detection scheme [130]. This patent describes a method of arc detection in AC electrical power distribution systems using current and voltage monitoring. The current monitor here is novel since it uses a current transformer in series with a capacitor, which in turn is in parallel with an inductor element, which is in series with the line. This allows

the inductor to conduct the low frequency power line signals, and the capacitor and current transformer to conduct the higher frequency current components associated with electric arcs. The output from the sensor is processed and a trip signal is generated.

Dollar was later granted patent US 2002/0183944 A1 in 2002 for a DC arc fault detection system in a vehicular application where a superheterodyne circuit is used to detect high frequency emissions from arc fault behaviour and a simple comparator, accumulator and timing circuit is used to confirm arcing behaviour [131]. This patent lacks any specific detail regarding the frequency range monitored by this approach and is open to nuisance tripping due to interfering EMI sources.

In 2007 as part of an investigation into arcing within Naval electrical distribution systems Kim reported on VHF and UHF radiated RF emissions from electric arcs drawn between carbon electrodes [132]. Later in 2009 Kim recorded that *"Radiation from the arc is a reflection of all of the discharge dynamics of the arc process"* [133]. Arc dynamics are based around the physical configuration of the arcing electrodes and the environment in which they reside, which in itself is subject to variation between one discharge event and the next discharge event. Kim later explained that electromagnetic radiation from arcs has long been studied and is dominated by the rapid arc current changes in the arc dynamics. Kim also experimented using a blade contact in a knife switch as a means of drawing an arc and goes on to evaluate electromagnetic radiation using a stick and loop antenna. Kim concluded that *"The stick and loop antennas with frequency bands of low AM and megahertz, respectively, are effective in detecting the arc / spark of the low-voltage circuit."* [133].

The Fast Fourier Transform (FFT) is a popular method for determining the spectral content of a given sampled time domain waveform. Many arc fault detection schemes have attempted to use this technique for fault detection and these are summarised thus.

In 2003 Luis analysed arc currents during guillotine-induced parallel arc faults using FFTs in 42VDC automotive electrical systems, where it was concluded that arcing current does not exhibit a sufficiently high magnitude or distinct arcing signature, and the broadband characteristics display no significant or distinguishable features that can be used for simple detection of all arcs [134].

González and Button also presented a paper in 2003 discussing the detection of high impedance arcing faults in DC radial distribution systems [135]. Their work highlighted several important points, firstly that high levels of high frequency noise in excess of 30MHz were present on the arc voltage, where it is impossible to sense arc voltage in a complex aircraft system because the location of a given arc fault is unknown. Secondly, to locate arcs in a radial distribution system it would be necessary

to isolate each switched output with a small LC filter, which was demonstrated to be successful for cable lengths of less than 50ft, but any series impedance introduces losses into the distribution system. In contrast to the voltage signal, the current signature is at relatively low frequencies and modifications to the cable lengths do not significantly affect this information. It was demonstrated that current noise behaviour was not always consistent and it was suggested that combining current and voltage detection may be necessary to create a robust detection system. Their final conclusion was that robustness is key to a successful detection system and that further work is required to distinguish between real arc faults and transient events such as DC brushed motors and relays opening and closing.

Rivers et al were granted patent US 2005/0207083 A1 in 2005 for their FFT-based arc fault detection system for an Arc Fault Circuit Breaker (AFCB) application [136]. Arc current is monitored, a representative FFT is produced, and the output of the FFT is split into three frequency bands where the energy present in each given band must exceed a set of predefined references. In the event that the energy in each three bands exceeds each of the three references then a trip signal can be issued to the SSPC or circuit breaker. This scheme addresses drill loads, compressor loads and resistive loads and therefore robustness against nuisance trips will be superior to other FFT-based arc fault detection methods.

Ohta et al were granted patent US 2009/0284265 A1 in 2009 for their FFT-based arc fault detection scheme [137]. The scheme samples arc current and produces FFT plots over time using a rolling window, and from the current FFT spectra the Mahalanobis distance is calculated. The Mahalanobis distance is a multivariate statistical analysis tool for indicating covariance distance of new data against and existing data set [138]. If the Mahalanobis distance exceeds a given threshold then this is indicative of arcing behaviour and the SSPC or circuit breaker can be turned off. This scheme is novel however it does not address the issue of broadband current noise as part of normal load operation. Similarly Xiaochen et al presented a paper on AC arc fault detection based on the Mahalanobis distance where in this case odd and even harmonic components are extracted from an arc current signal and compared with an existing master arc fault data set [139]. This method assumes that every arc fault will feature the same characteristics as the arc created in a lab environment, therefore further work on nuisance trip robustness is required.

National Semiconductor Corporation presented their DC arc fault detection evaluation board based on their Solarmagic^{TM} technology in 2011 which detects arc faults on photovoltaic (PV) systems with voltages up to 1000V and currents up to 10A using a current transformer as the main input [140]. The detection algorithm is based on detecting an increase in current noise in the frequency range 40-100kHz. Neither the physical origin of this broadband noise emission nor the effect of interfering noise

sources including power converters and loads are considered. Healy and Roemer of Pulse Electronics observe that in high current PV systems, Rogowski coil current sensors are preferable since they do not suffer from core saturation like ferrite core current transformers and offer improved bandwidth up to 1MHz [141]. This is a key finding which later supports the development of a Rogowski coil current sensor in Section 4.3.

In 2013 Reil et al prepared a paper comparing different DC arc spectra investigating the effect of different contacts, contact materials, cable lengths, inverters and resistive loads on the arc current frequency spectrum [142]. It was found that characteristic frequencies for individual arcs do not exist and that to detect an arc from basic noises in the PV string, a broader range of frequencies in the 1/f spectrum has to be observed. It was also found that certain frequencies created by arcing are absorbed when longer feeder cables are used. The power source and inverter both need to be clearly defined within a given test standard since their spectral behaviour severely impacted test results. In an aerospace application it is not always possible for the electrical power distribution system designer to know load characteristics in any great detail beyond the limitations imposed by RTCA DO-160G [49].

Rabla et al presented a method of locating series arc faults in 270VDC automotive, aerospace and photovoltaic (PV) systems by analysing the correlation function of the RF signals detected by two Rogowski coils inserted at two points within the circuit under test [143]. Rabla et al show that for arc localisation to be achieved a Rogowski coil would be required both at the output of an SSPC and at the input to the load which it is feeding. Distributed sensing in an aerospace application is not ideal since it complicates the electrical system design and defeats the modular design of the system. In addition to this, if load-side monitoring were permitted then a simple remote voltage sensor at the input to the load would allow calculation of voltage across the cable feeder thus making arc fault detection trivial.

Most recently in 2014 Wendl et al characterised low current DC arcs motivated by a requirement from the National Electric Code (NEC) in the United States of America that photovoltaic (PV) systems with voltages in excess of 80VDC shall be protected by Arc Fault Circuit Interrupters (AFCI) [144]. Arcs were created by placing a thin copper braid between two electrodes at a defined spacing, where current and voltage data was gathered on an oscilloscope. Data was gathered covering different arc currents and electrode separations and it was determined that the power spectral density of the current signals varies with current magnitude, where higher currents provide more stable arcs with reduced spectral content, and similarly shorter electrode separations result in more stable arcs which lead to lower noise levels. It is noted that the worst case scenario for arc fault detection is an arc which strikes with weak disturbing properties such as a high current and a short electrode separation.

A variation on the FFT is the Short Time Fourier Transform (STFT) which analyses shorter duration data sets on a rolling-window basis. Strobl and Meckler published waterfall plots of arc current during series arc events in 35V, 40V and 45V DC electrical systems [68]. Strobl and Meckler state:

> *"The current signals show a noticeable broadband frequency spectrum. Only at ignition, at extinction and at some other larger steps - probably caused by arc root motions - spectral ranges up to 100kHz can be recognised. During the intervals of steady burning the spectrum shows a small width of some kHz."*

Using this spectral content as a basis for a detection algorithm could be acceptable in a lab environment, but is likely to cause nuisance trips in an aircraft environment due to radiated and conducted radio frequency interference, and power quality variations from the aircraft generation and conversion equipment.

Later in 2009 Hong et al proposed that the STFT can be utilised to detect series arc faults based on the reduction of the fundamental amplitude and the presence of even and odd order harmonics during a series arc fault event in 50Hz power distribution systems [145]. Hong et al continue:

> *"When the arc is in series with a load, it is necessary to look for changes as well as the characteristics themselves. However, some loads have the time domain characteristics that look much like characteristics of arcs, so it is also very important to test the detecting algorithm for the unwanted tripping."*

Hong et al later implement and evaluate an STFT detection scheme which detects harmonic current content in the range 100Hz-1500Hz based on a 50Hz distribution system [146]. A range of loads including an electric iron and a personal computer were tested with the series arc fault detector, and these did not cause nuisance trip events. The algorithm was tuned extensively in order to achieve this result.

The Wavelet transform is a scale-space method used for extraction of multiple scale features from a given data set. Fernández and Rojas presented a literature review in 2002 giving an overview of the application of wavelet transforms in power systems applications including power quality, partial discharge detection, load forecasting, power system measurements, power system protection and power system transients [147]. Of particular interest is the ability to detect partial discharges where unlike Fourier transforms, Wavelet transforms allow transient events to be identified with both good time and frequency resolution.

Li and Li presented Wavelet transform analysis of the current signal in 115VAC 400Hz systems featuring series and parallel arc faults [148; 149]. A top level signal

was sampled at 12.5KHz which gave a signal bandwidth of 6.25kHz. The Daubechies wavelet was used for the analysis, the signal was broken down into dyadic blocks and the digital frequency is divided by 2 per level. Level 3 was selected for analysis since this provides 1.5625kHz between each wavelet packet node. Li and Li then claim that wavelet packet coefficient node (3, 4) at level 3 is 7.8125kHz and this is close to a characteristic of the arc fault waveform. The choice of this frequency is not justified in the paper and could be a feature of the test setup used for the experiments in the paper. Li and Li continued on to extract arc fault features from the current signal under scrutiny.

In 2009 Yunmei et al applied wavelet packet analysis to the detection of low voltage 28VDC series and parallel arc faults, where the Coif wavelet packet system is used rather than the Daubechies wavelet since this wavelet is more symmetric [150]. The sampling rate used was 100kHz allowing a highest analysis frequency of 50kHz. This detection scheme was experimentally verified using the SAE AS5692 [8] loose-terminal and guillotine experiments to imitate series and parallel arc faults respectively, where the results show that series and parallel arcs can be differentiated from normal load-step behaviour. The paper does not address more complex high-frequency load behaviour which may mislead the detection algorithm.

Changali et al were granted Patent US 2009/0168277 A1 in 2009 which outlines an AC series and parallel Arc Fault Circuit Breaker (AFCB) [151]. Arc current is sampled at a rate of 50kHz before undergoing a 6^{th} level Discrete Wavelet Transform (DWT) to achieve coverage of 700-1500Hz which the authors claim is a frequency range in which energy is characteristic of arcing. Presence of energy in this range is then used to detect series arcing and to trip a given circuit breaker.

Ruixiang and Zhengxiang propose an arc fault detection method for 220VAC 50Hz electrical systems based on signal energy distribution in a given frequency band in their 2012 paper [152]. Series arc faults were induced using a drawn arc test scenario and the arc current waveform was recorded. The Daubechie3 wavelet was chosen to give three layers wavelet decomposition. Ruixiang and Zhengxiang identified that the signal of the arc has a high frequency component around 115kHz, which is ultimately thresholded in order to confirm the presence of series arcing.

In 2013 Wu et al presented a method for arc fault detection based on analysis of a signal's characteristic frequency band by means of a wavelet transform [153]. The circuit under test features a 220VAC 50Hz power source, a resistive load and a series arc fault. The sampling rate used for capturing arc current is 250kHz allowing a maximum input signal bandwidth of 125kHz, however the specific type of wavelet used for analysis of the signal is not disclosed. It was concluded that the change in energy in the frequency range 1.9-7.8kHz, corresponding to the 5^{th} and 6^{th} detail

signals, during the transition from normal operation to the introduction of a series arc fault is sufficient to indicate the presence of the fault.

Wang et al presented a paper in 2013 proposing a method of arc fault detection in DC photovoltaic arrays using wavelets, as a superior solution compared with FFT-based analysis [154]. Wang et al use a sampling rate of 1MHz and apply the Daubechies mother wavelet to decompose the arc signal, where the 4^{th} to 6^{th} levels of decomposition covering 7.8kHz to 62.5kHz clearly differentiate between series arcing and normal load behaviour. It is noted that the wavelet transform is very effective at detecting the exact instant at which a signal changes and also the type and amplitude of the change, where FFT-based techniques cannot locate events with sufficient accuracy in the time domain.

Koziy et al presented their low-cost power-quality meter with series arc fault detection capability for 115VAC 60Hz smart grid applications in 2013 which uses the Daubechies wavelet to extract local signal disturbances from the arc current signal with very high resolution [155]. Koziy and al further claim that series arc fault load disturbances lay within the 2-4kHz range which corresponds to detail level 3 of the discrete wavelet transform based on the 30.756kHz sampling rate, where Daubechies wavelets db2 were found appropriate for extracting arc fault features. The load is tripped by peak detecting the detail level 3 signal where if the peak exceeds a given threshold, an arc event is flagged and following the detection of a specified number of arc events within a moving window then a load trip is triggered.

In 2013 Cao et al investigated wavelet packet decomposition as a method of arc fault detection in DC electrical power systems with source voltages in the range 42-90V [156]. Data was gathered from drawn arc experimentation at a sampling rate of 100kHz and it was determined that at arc initiation the arc energy is in the low frequency range below 2kHz and when the arc becomes stable the current spectrum is very similar to the normal load current. For higher current loads it was determined that the presence of the series arc was undetectable. A load step was also performed to compare spectral characteristics with those of the series arc and it was determined that the current amplitude was in the range from 1.5-4kHz and from this data the arc fault could be distinguished from a simple load transient. Cao et al used a Coiflet wavelet at different levels from 3 to 7, and it was found that the 6^{th} level provided the best results during experimental verification.

Qi et al presented an adaptive real-time discrete wavelet transform based method for arc fault detection in 2014 [157]. The research focusses on detecting arcs within 230VAC 50Hz electrical systems. It is noted again that the Daubechies wavelet is mostly used for feature extraction since it is more adapted to detect the transient events in a given signal. Qi et al implement a novel FPGA-based adaptive wavelet

transform system based on a 28^{th} order low pass FIR and 28^{th} order high pass FIR allowing implementation of up to Daubechie14. The implementation can be configured to use different mother wavelets, different decomposition levels and different threshold levels. Different loads were analysed using MATLAB® in order to determine the optimal parameters for a given load, where the extracted parameters can be used to drive the FPGA configuration. This is a great way to improve robustness against nuisance trips caused by normal load behaviour, however it relies on the ability to gain access to and to characterise every conceivable load in a given system which is not always practical, especially in an aerospace application.

In 2014 Yao et al presented a method of series drawn arc fault detection in DC electrical power systems for source voltages in the range 75-300V with load currents in the range 3 through 25A [158]. Arc current was sampled at 200kHz and a wavelet packet decomposition procedure was applied up to level 2 using a Daubechies8 and Coiflet wavelet. The low level 2 decomposition used here combined with a relatively high sampling frequency leads to four coarse frequency bands 0-25, 25-50, 50-75 and 75-100kHz. The frequency range 25-50kHz formed the focus of the detection algorithm where a simple confirmation algorithm is applied to avoid nuisance trips. Experimental verification shows that the detection scheme functions correctly for genuine arcs and does not nuisance trip in the presence of a load step change.

The key observation from the Wavelet transform literature is that the basis of the wavelet feature detection in each case is not directly correlated with the arc physics. Each researcher also selected a different sampling rate and claimed that a different frequency band was indicative of arc fault behaviour, thus suggesting that there is no specific frequency band indicative of electric arcing. Furthermore other interfering sources could be detected as a false positive and thus the author is reluctant to further pursue Wavelet transform analysis for arc fault detection purposes.

Pan et al proposed a method for distinguishing a regular AC load current signal from an arc fault signal using time-ridge analysis in their 2013 paper [159]. Spectrograms of the arc current signal feeding noisy electric lighting both in the presence of and in the absence of electric arcing show that in the absence of arcing the first, third and fifth harmonics are present, however in the presence of arcing many higher harmonics are present. Ridge analysis allows arc fault detection by only looking at specific “ridges” in the spectrogram in order to differentiate noisy loads, such as the lightning load used previously, from real arc faults. Since a low-current lighting load is used for system verification, where pre-arc current is in the order of 75mA, the initiation of an arc results in a load current rise up to 10A. This dynamic range in load current of 133:1 suggests that the complex detection system in this paper is unnecessary, although the technique itself is promising.

Grassetti et al presented a novel algorithm for parallel arc fault identification in DC aircraft power systems, with particular regard to 28VDC systems where the frequencies of current spikes created by a given parallel arc fault were determined and plotted against time [160]. Parallel arc fault identification was performed by analysing current spike frequency against specific energy where it was proposed that parallel arc faults are characterised by high specific energy pulses at high frequencies. An algorithm was proposed where a 100ms time window and 6A over current threshold were used along with current and frequency thresholds for the purposes of arc fault detection. This paper addresses passive parallel arc fault detection but does not analyse any susceptibilities of the algorithm to nuisance trips caused by multiple burst lightning or varying load current demands and therefore this method is of limited usefulness.

Brechtken presented a paper on arc fault detection in three phase 400VAC systems where the harmonics of the system are monitored during the presence of a series arc fault on a single phase under a range of different load current levels up to 75A with a full range of power factors, and it was determined that the ratio between the amplitudes of the third and fifth harmonics remained constant at 1.6 across the operating range enabling an arc fault detection system to be designed [161]. Unfortunately this method is of limited usefulness since this technique is not transferable to DC systems. Similarly to Brechtken, Khan and Critchley published a paper detailing an arc fault detection system for a three phase 115VAC 400Hz application where the load currents for each three phases are monitored and in the event that the average current imbalance exceeds a given threshold over a given time, the circuit breaker can be tripped [162]. It was noted that during initial application of power to a load there could be a current imbalance as part of normal operation, and therefore the arc fault detection scheme should be inhibited for a preset time, where if the imbalance exceeds the preset duration a genuine fault is assumed and the circuit breaker can be tripped. This scheme was implemented in a 60A electromechanical circuit breaker and the additional detection circuit only presented a minimal increase to the overall volume of the device. The test data indicated that this scheme was effective at detecting parallel faults, however the paper did not discuss the types of loads used for this study. This technique could be modified for application in a bipolar DC system such as the proposed +/-270VDC aerospace standard.

2.4.4.3 Pre-recorded Signatures

Johnson and Kang presented a method of tuning arc fault detection algorithms using pre-recorded load currents, firstly during normal operation of a power inverter in a photovoltaic system under both cloudy and bridge conditions, and secondly during hundreds of series and parallel arc fault test scenarios [163]. These waveforms were all processed by Fast Fourier Transform (FFT) to produce magnitude plots over frequency, which were used to characterise normal operation compared with the var-

ious arc fault scenarios. The pre-recorded waveforms were played back via a Digital to Analogue (DAC) converter into the arc fault detection hardware under test as a method of algorithm verification. While this is a simple idea the number of combinations and permutations of power source, cable configuration and load behaviour result in the need for a large number of recordings which would be prohibitive in an aerospace scenario, since the tier one electrical system integrators do not necessarily have access to fully representative aircraft loads. Pre-recording of arc signatures is not trivial since in order to record arc signatures for the wider audience, the required bandwidth and thus sampling rate would have to be carefully selected based on a set of claimed arc fault-indicative characteristics which vary wildly from one researcher to another.

2.4.4.4 Model Based

In 2006 Beck and Nemir produced a paper on arc fault detection through model reference estimation [164]. This approach attempts to increase the robustness of existing arc fault detection algorithms to the effects of load current variation by predicting normal system behaviour using a discrete-time linear autoregressive model for AFCB output voltage and current. The argument is made that the majority of loads are a combination of resistance, capacitance and inductance, and therefore a second order model is usually sufficient for modelling aircraft loads. The issue with this approach is that every load would need to be characterised such that model coefficients could be extracted, and thus Beck and Nemir propose to estimate the model coefficients from the real time data. For the parameter estimation a stochastic approximation was adopted where the designer must ensure that the time constant is not so fast that parameter estimates vary wildly from sample to sample, yet not so slow that the model convergence is too slow. If the estimation errors (or residuals) for the linear model are high, this is used as an indication that non-linear arc behaviour is present in the system. This approach was successfully demonstrated to detect a carbonised arc fault in a 115VAC 60Hz system, yet was resistant to nuisance tripping in the presence of a noisy 800W dimmer load. Beck and Nemir were later granted patent US 7,366,622 B1 on this technology in 2008 [165].

Arunachalam and Diong continued the work of Beck and Nemir and applied the same model based reference estimation technique to both 115VAC 400Hz and 270VDC systems, where carbonised parallel and series drawn arc faults were detected successfully while providing resilience against noisy load waveforms [166]. Evidence of the functionality and robustness of this scheme within a 270VDC electrical power distribution systems featuring representative power sources and loads remains to be seen.

Later in 2010 Beck et al presented a Minimum Description Length (MDL) approach to arc detection where they acknowledge that the assumption that a load has linear

behaviour is not ideal since, for example, resistors have a temperature coefficient which can be seen under high current operation [167]. Beck highlights a dynamic range issue between a model capable of modelling load behaviour in the absence of an arc which would require a small number of coefficients in the model reference estimation scheme, and a model capable of predicting system behaviour in the presence of an arc which would require a large number of coefficients. This is a well known phenomenon referred to as Algorithmic Information Theory or Kolmogorov complexity. By implementing compression, both normal system behaviour and behaviour in the presence of arcing can be modelled, allowing an arc fault detection system to be realised.

Most recently in 2014 Strobl presented a model based approach to arc fault detection, however rather than a proposed solution this is a well partitioned list of design considerations for arc fault detection systems [168]. Strobl describes a set of modelling inputs to the design of arc fault detection sensors and control gear including network modelling (including sources, cables and loads), fault modelling (including arc models and noise models), large signal modelling (for fault examination) and small-signal analysis (for analysis of noise propagation). Standard specifications and other additional requirements including cost are covered here. The remainder of the paper is concerned with modelling faults in photovoltaic installations which are not relevant to this thesis.

2.4.4.5 Mathematical Morphology

Leprettre and Rebière coupled time-frequency analysis of AC series arc fault current waveforms with mathematical morphology in their 2001 publication [169]. The scheme begins with the arc current derivative, from which a spectrogram is computed. A first morphological structuring element is created in order to connect features spaced less than 8.3ms apart, which the authors assume to be the series arc features. A second structuring element is defined in order to erase every feature that was not connected by the closing operation and thus features spaced at 8.3ms or greater are therefore eliminated from the spectrogram. The algorithm is completed by integrating along the frequency axis thus giving a "series arc probability" plot. Leprettre and Rebière claim that their method was always successful in detecting arcs and rejecting transient load behaviour. Any periodic perturbations caused by motor harmonics are also eliminated from the spectrogram by the morphological processing.

Mathematical morphology functions well to detect series arcs, but Leprettre and Rebière cover only application to AC systems and thus further research is required into DC series arc analysis with mathematical morphology. Furthermore no justification was provided for the 8.3ms feature interval, therefore there is a concern that this is a purely empirical solution which may be limited to application on the specific arc fault test apparatus used during these experiments.

2.4.4.6 Genetic Algorithms and Neural Networks

Yaramasu studied arc fault detection and location for aircraft power distribution systems as part of his masters thesis where a genetic algorithm was used as a computationally efficient method of estimating the distance to an intermittent fault [170]. This arc fault location scheme first uses a network of lumped ABCD transmission lines to model the aircraft distribution system and from this a system matrix is obtained which is solved by a genetic algorithm. Although the simulation and test work carried out demonstrates that faults can be located and shows that the system is robust to loads turning on and off, further work is needed to determine whether this scheme can function when subjected to electrical power variation and electromagnetic susceptibility testing in accordance with RTCA DO-160G [49].

Yaramasu also remarks that intermittent fault phenomena, such as series arc faults manifested as loose terminals excited by vibration, may not be repeatable when an aircraft is on the ground since no vibration is present and therefore such a fault is very difficult to detection [170]. Further to an additional review of glowing connections presented in Section 2.3.4 it is possible that "loose terminals" may manifest themselves as "glowing connections" in the absence of the aircraft vibration stimulus.

Zadeh published a paper in 2005 proposing a method of detecting a High Impedance Fault (HIF) in an AC power distribution system where the distribution bus voltage and current signals are preprocessed and second and third harmonic content is filtered and fed into an Artificial Neural Network (ANN) [171]. The ANN is a subset of machine learning systems where the network is trained by Zadeh to function as a pattern recognition tool to detect HIFs. The ANN system was demonstrated successfully detecting faults as far away as 40km.

In 2011 Maguan and Guan presented an arc fault recognition approach firstly using a wavelet transformation to extract frequency and time characteristics of arc current, and secondly a Back Propagation Neural Network (BPNN) was trained to recognise valid arc faults [172]. The scheme detected Mean Square Error (MSE) and continued the training process until the MSE fell to 1 given 100,000 iterations.

Yuanhang et al built on the work of Maguan and Guan in their 2013 paper where in place of the BPNN, a Weights Direct Determination (WDD) method was used to accelerate learning speed and reduce the training time of the neural network [173]. Yuanhang et al concluded their paper with the remark *"WDD neural network not only has a simple structure, but also has the ability of identifying aviation fault arc with nearly 100% of accuracy"*.

Nuisance trips are of great interest to those skilled in the art of arc fault detection, and each researcher is on the quest for a zero nuisance trip rate. However the neural

network schemes presented here all use an optimisation technique where success of the learning process is determined when the nuisance trip rate falls below a given threshold, so by definition these systems will always have a nuisance trip rate greater than zero.

The ability of the neural network to correctly classify a given arc fault depends heavily on the data set with which it is provided and therefore a robust detection solution must consider the full range of possible source, wiring and load combinations and permutations under the full range of EMC and EPV test scenarios in order to achieve a high detection rate. Conversely since the aerospace electrical environment is unfriendly, teaching the neural network what is not a genuine arc fault is also of value and it would be interesting to trial this technique on brushed electric motor loads and during contactor switching events which create arcs during normal operation.

2.4.4.7 Network Analysis (for Arc Fault Location)

Alamuti et al published papers in 2010 and 2012 discussing their intermittent parallel arc fault location technique for three phase AC power distribution systems where an equivalent RL circuit is produced for each of the three phases and circuit analysis is used to derive location to the given fault based on the level of inductance between the source and the arc fault as a percentage of the total cable inductance between the power source and load for the other two phases, thus enabling the distance to the fault to be determined [174; 175]. This technology is similar to that proposed by Yaramasu and has benefits when compared to other arc location schemes since no significant additional hardware is required beyond the existing voltage and current monitoring hardware for the line under test, unlike schemes such as TDR, FDR or SSTDR which require significant additional hardware.

Cao et al proposed a novel series arc fault location approach based on a two conductor RLC transmission line model with current and voltage monitoring at both the power supply and load of a power distribution circuit [176]. An expression is derived which allows calculation of the currents and voltages seen at the series arc fault based on the equivalent circuit and the recorded currents and voltages at the power supply and load. Assumptions are made regarding the line impedance Z, the currents and voltages at the source and load are sampled and from these an FFT is applied to the sampled data. For a given assumed fault position, the arc currents are calculated and a current error signal is generated. Frequency F_k is then found at the point where in the frequency range 5kHz-30kHz the current error is at the minimum condition.

The approach of Cao et al is a simple way to locate series arc faults without the addition of complex hardware. However the author is very critical of this approach since it relies on the ability to monitor current and voltage at both the source and

load, which may not be possible in an aerospace application. If it is possible to measure the load voltage then providing arc fault detection capability is trivial since the voltage across the cable can be monitored, and if a voltage in excess of 15V is encountered, an arc fault or very high impedance is present in series with the feeder cable. This approach also provides the ability to accurately measure the voltage drop across a given cable for voltages less than 15V, thus allowing the indication of glowing connections and other faults.

2.4.4.8 Noise Domain Reflectometry (NDR)

Lo and Furse are typically more associated with their research on active wiring fault detection methods, as detailed in Section 2.5. However their 2006 paper discussing Noise Domain Reflectometry (NDR) offers an arguably passive approach to wire fault location using the autocorrelation function [177]. An uncorrelated random source generates a signal which is either connected through a directional coupler to the wire under test (NDR I), or directly connected to the wire under test (NDR II). Reflected signals seen either at the output of the directional coupler for NDR I, or directly on the input to the wire under test for NDR II are fed into a multiplier along with the random source delayed by time λ, the output of which is fed into the autocorrelation estimator in order to determine the fault location. Lo and Furse demonstrate functionality of this scheme on controlled impedance cables, and although they have proven detection of momentary open circuit and short circuits, it is questionable whether this scheme can be applied to loose terminal arc faults since the impedance discontinuity presented by the fault may be too small to detect.

2.5 Active Arc Fault Detection Methods

Active arc fault detection and location methods apply a stimulus to the given wire under test in order to detect and locate faults. Active arc fault detection techniques must be considered since they promise to reduce nuisance trips significantly. The majority of active schemes focus on reflectometry which is an area where Furse et al at the University of Utah have been particularly active in the research of wire fault location over the last ten years. The author is concerned by active arc fault detection methods due to the significantly increased technical complexity of the given solution, which drives both increased non-recurring engineering cost to implement, and a corresponding increased recurring hardware cost.

2.5.1 Time Domain Reflectometry (TDR)

Time Domain Reflectometry (TDR) is arguably the simplest method of wire fault detection whereby a step function with a very fast rise time is applied as an incident signal to the wire under test, and reflected signals are monitored and analysed to

determine the location of the given fault. Furse et al evaluated TDR as a method of detecting wire faults and suggested that TDR would be an excellent method of locating small anomalies such as frays and chafes if a very accurate initial baseline is available, although they noted that it is not practical to baseline every wire within a fleet of aircraft [178]. It is also noted that given the sensitivity of the TDR method, any movement of the wiring due to maintenance and operation can cause a change in wire impedance which dominates any change caused by "soft" faults. It is proposed that TDR is limited in live wire test applications since the magnitude of the TDR signal would need to be below the acceptable EMC emissions chart, and any noise on the wire under test would corrupt the TDR profile. Interestingly Furse et al note that TDR is capable of testing branched networks, subject to the availability of a network topology extraction algorithm.

2.5.2 Low Energy High Voltage (LEHV)

High Potential (HiPot) wire testers have been used for many years in both manufacturing test and as part of regular maintenance in order to detect defects in electrical systems prior to them becoming shorts. In aerospace applications these tests are carried out while the aircraft is on the ground thus limiting test coverage. While defects and faults can be easily detected, HiPot testing is not capable of locating them.

Building on HiPot testing, Eisenhart and Ballas presented a paper on the practical application of Low-Energy High-Voltage (LEHV) wire diagnostic techniques to detection of faults in the aircraft Electrical Wiring Interconnect System (EWIS) [179]. Eisenhart and Ballas break LEHV down into two techniques where firstly the "fast pulse technique" utilises a high voltage, narrow width pulse which is transmitted down the wire under test and a comparison of the reflected signature with and without an arc is monitored allowing analysis of the presence of and distance to a given wire fault. The "fast pulse technique" is also referred to as Pulse Arrested Spark Discharge (PASD) which is a technique patented by Sandia National Laboratories [180; 181; 182].

The second scheme presented by Eisenhart and Ballas is the "slow charge breakdown technique" which begins by slowly charging the distributed capacitance in the EWIS to a fixed voltage. If an arc or breakdown occurs the distributed capacitance discharges and analysis of the reflected signature allows the distance to wire fault to be determined [179]. In reality these techniques work well when combined, whereby a DC scan using the "slow charge technique" is used to locate potential defects, and the "fast pulse technique" is used to improve the distance to wire fault solution, although this is highly dependent on knowledge of the Velocity of Propagation (VOP) within the wire under test.

LEHV schemes have been implemented as a piece of test equipment such as the Astronics LEHV test set which can be used by maintenance staff without specialist skills. At the time of writing this technique has not been employed to detect or locate faults on live wires, and therefore a similar scheme could be integrated into an aerospace SSPC for further investigation.

2.5.3 Frequency Domain Reflectometry (FDR)

Furse et al critically compare reflectometry schemes and note that Frequency Domain Reflectometry (FDR) is a method where a stepped set of sine waves are transmitted down the wire under test, and each sine wave is subsequently measured for frequency, magnitude and phase in order to determine distance to a given discontinuity [178]. From this basic concept Frequency Modulated Continuous Wave (FMCW) systems measure frequency shift, Phase Detection Frequency Domain Reflectometry (PDFDR) systems measure phase shift and Standing Wave Reflectometry (SWR) systems measure amplitude variations in a given standing wave.

The Frequency Modulated Continuous Wave (FMCW) approach varies the frequency of the applied sine wave quickly generally in a ramp function, and measures the frequency shift between incident and reflected signals. Distance to a given fault is determined by converting frequency shift into time delay based on the frequency ramp rate. It is important to note that FMCW has not been implemented for wire testing due to limitations on the maximum speed of the ramp [178].

Furse et al applied Phase Detection Frequency Domain Reflectometry (PDFDR) to wire fault location in aircraft wiring in their 2003 paper where the scheme proposed operates in the frequency range 0.8GHz through 1.2GHz providing a range of 4.5m, and a resolution of 3cm, although the range and accuracy can be adjusted by changing the frequency bandwidth and number of steps used in the frequency sweep [183]. It is noted that the PDFDR scheme requires a large impedance discontinuity in the form of a near open or short circuit along the wire under test in order to detect a given fault, and smaller impedance changes due to damaged insulation and non-opening series arc faults are virtually undetectable. The PDFDR scheme is therefore less attractive for series arc fault detection applications, whereas parallel arc faults create near-short circuits which are more easily detectable using this method.

Standing wave ratio (SWR) systems apply a sine wave to the wire under test and measure the magnitude of the standing wave created by the superposition of the incident and reflected waves on the wire under test, and in the scenario where a null in the standing wave is detected, the distance to the fault can be determined [178]. Again the signal magnitude required to provide reliable detection is likely to exceed the acceptable EMC emissions outlined in RTCA DO-160G [49].

2.5.4 Joint Time-Frequency Domain Reflectometry (JTFDR)

Shin et al propose a scheme in their 2005 paper where Time Domain Reflectometry (TDR) and Frequency Domain Reflectometry (FDR) techniques are operated simultaneously in order to create a new high performance Joint Time-Frequency Domain Reflectometry (JTFDR) scheme [184]. Shin et al use a Gaussian Time Envelope to gain time localisation and multiply this by a chirp signal which allows excitation of the system over the frequency band of interest. Detection and accuracy of the reflected signal are enabled by use of a cross correlation function. This scheme was demonstrated on RG-142 controlled impedance cable where the JTFDR waveforms more clearly show impedance discontinuities in the test cable with higher resolution in contrast to the TDR scheme, however it is later mentioned that a degree of tuning is required for operation on different cable types with particular regard to the range of the chirp signal used.

In 2006 Sadok et al demonstrated a novel Time-Frequency Domain Reflectometry (TFDR) scheme based on the application of a standard TDR incident wave to the wire under test, where the reflected signals are analysed using a Continuous Wavelet Transform (CWT) to extract defect-related signatures, and the popular "Mexican hat" wavelet was found to provide the most effective extraction [185]. Bechoefer and Sadok were granted patent US 7,120,563 B2 in 2006 for the CWT-based TFDR scheme [186]. In this scheme a CWT is applied using a single scale value to first determine the presence and location of any "hard" faults present on the wire under test, and secondly a CWT-based Time-Frequency map is computed in order to detect "soft" defects. A stationarity index can be determined from the Time-Frequency map which allows location of the "soft" defects. The scheme was demonstrated on the Goodrich Wire Integrity Tool (GWIT), which is a hand held TDR with a 200ps rise time and 2.5GHz bandwidth. The proposed scheme correctly detected all "hard faults" tested and detected approximately 50% of "soft" wire defects. The testing of "healthy" wires resulted in 14% mischaracterisation as damaged wires, and this is directly equivalent to nuisance trips in arc fault detection systems.

The work of Sadok et al was based on lab testing and is aimed at wire fault detection on aircraft during regular maintenance. Testing of live wires was not considered during this testing and therefore the TFDR scheme is arguably unsuitable for an arc fault detection solution. The CWT approach to analysis of TDR signals is a novel method of "soft" wire fault feature extraction and could be transferable to a live wire application if nuisance trips could be eliminated.

2.5.5 Sequence Time Domain Reflectometry (STDR) and Spread Spectrum Time Domain Reflectometry (SSTDR)

Sharma et al presented an exciting paper in 2007 covering the Silicon implementation of Sequence Time Domain Reflectometry (STDR) for detection of faults on live wires in aerospace power system applications, where STDR uses a pseudo-noise (PN) code for the incident signal [187]. The STDR scheme is coupled with the Time Domain Vernier (TDV) method which uses a deterministic PN sequence to transmit on to the wire under test at a level not exceeding the conducted emissions limit. The PN sequence is reflected back from any impedance discontinuity, which is manifested as a scaled and delayed representation of the original PN signal, and from this reflected data the location of the fault can be determined.

Furse et al note that the PN signal can be very small with respect to the aircraft signal on the wire and in the order of -20dB down [178]. This is an attractive feature since EMC emissions regulations in aerospace applications are strict and can be difficult to meet, especially in cases where high frequency RF signals are present on the non-shielded power cables found in the electrical power distribution systems.

In contrast to STDR, Spread Spectrum Time Domain Reflectometry (SSTDR) uses a sine wave modulated PN code. When the transmitted and received PN codes are synchronised a high value is obtained from the correlation stage, and conversely when the PN codes are unsynchronised a low value is obtained, thus allowing the location of a given fault to be determined [178]. The advantage of SSTDR is that it provides a sharper correlation peak compared with STDR when operated on live data transmission wires since the operation frequency is typically higher than that of data signals present on the wire under test, but this is unlikely to be beneficial on power feeder cables. For both STDR and SSTDR the estimated maximum cable length supported is limited by cable attenuation and hence by the physical wire type, and is in the order of 70+ ft, where a typical accuracy of one inch is achievable.

Smith's work has demonstrated that STDR and SSTDR can be effective tools for locating defects on live cables and this was demonstrated on both controlled and uncontrolled impedance cables carrying 60Hz AC signals [188]. Aircraft power feeders represent an uncontrolled impedance since the the power feeders are typically in a wire-over-ground plane configuration where the separation between cable feeder and ground plane varies depending on the routing of that particular feeder within the aircraft structure.

Wei and Li analyse the behaviour of SSTDR in their 2011 paper where they conclude three important features of scheme are firstly that the magnitude of the reflected cross correlation wave head decreases when the cable length increases, secondly that when the frequency of the incident signal increases the total cable length which can be tested

reduces, and finally when the cable length and incident signal frequency are constant then the amplitude of the reflected cross correlation wave head is determined by the fault point impedance [189]. Furse et al classify wire faults based on identification of peaks in the reflected cross correlation wave head [178].

"Hard" faults such as open and short circuits are easily detectable by means of reflectometry, however Griffiths et al provide a critical analysis of the use of TDR, FDR and SSTDR schemes for fray location and other "soft" faults where they conclude that frays on wires have a reflectometry signature that is smaller than ordinary impedance changes on the wire such as wire movement and the presence of water droplets on the wire insulation [190].

The literature therefore indicates that both STDR and SSTDR are promising technologies for accurately detecting and locating open and short circuit wire faults on non-controlled impedance live wires without introducing prohibitively high levels of EMC emissions. There is concern that a "soft" fault, such as a series arc fault in a 270VDC system, may not provide a sufficient impedance discontinuity to be detectable using this method, given that frays are invisible to TDR, FDR and SSTDR schemes and that specific literature concerning location of series arc faults is sparse. In conclusion the cross correlation scheme performs well at preventing nuisance fault reports, but the classification of the type of wire fault by the magnitude of the reflected wave head may be inaccurate.

2.5.6 Carrier Signal Technology

In 2009 Kim presented a novel approach to arc fault detection in a naval application using "carrier signal technology" whereby a modem is used to generate a 2400bps Frequency Shift Keying (FSK) modulated data stream with a carrier frequency of 132.45kHz, which in turn is coupled onto the power cable under test, and a receiver at the opposite end of the power cable detects the transmitted signal and can verify that no arc fault is present [191]. In the event that an arc fault occurs it is proposed that the fault will interrupt communications momentarily which will indicate that an arc fault is present. Kim supports this approach with practical test data gathered in a lab environment.

While Kim's solution is acceptable for a naval application, the additional weight and complexity introduced for each cable run is likely to make this prohibitive for an aerospace application. In addition to this each circuit breaker / SSPC output and each load would require a transmitter / receiver, which in turn would need to communicate with a centralised computing resource, thus defeating the modular approach to electrical power distribution system design.

2.6 Other Methods

2.6.1 Bifurcated Arc Fault Detection

Brooks presented a bifurcated arc fault detection method for an Unmanned Combat Air Vehicle (UCAV) platform where rather than a single feeder, two parallel feeders are connected from an Arc Fault Circuit Breaker (AFCB) through to the given load [192]. During normal operation the load current is divided equally between the two feeders, and in the event of an arc fault on either feeder the current through the two feeders will no longer match and the AFCB can be tripped. This scheme is simple to implement, but in this scenario cables are being added to the system in order to test cables. This adds an installation and maintenance overhead, and reduces the numerical reliability of the system under test. In addition to this the two feeders can be chosen such that the sum of their conductor cross-sectional areas is equal, but having two cable insulation sleeves will contribute additional weight and will cause cable bundles to grow, and therefore this is not an elegant solution.

Yu et al of Honeywell International were granted patent US 7,489,138 B2 in 2009 for a somewhat inelegant solution whereby current and voltage are monitored not only at the output of a given circuit breaker at the AFD master node, but also at the load by means of the addition of an AFD slave node [193]. This allows the voltage across a given feeder cable to be monitored for signs indicative of a series arc fault, and in addition to this, current monitoring at the output of the AFD master node and input of the AFD slave node enables a differential current value to be computed, which in turn indicates the presence of a short circuit or parallel arc fault in the feeder cable. The requirement for an AFD slave node results in additional cost and complexity since the electrical power system provider would need to provide AFD slave nodes for every load fitted to the aircraft and in turn would need robust communication to each of the slave nodes, and therefore this scheme is impractical.

2.7 Sensor Fusion and Combined Detection Methods

2.7.1 Sensor Fusion

One widely accepted method of improving resistance to nuisance trips is to use multiple arc fault classifiers, described by Dong et al in their 2011 paper as the “fusion” method [194]. By utilising multiple sensors to determine whether an arc fault is present, the nuisance trip rate can be greatly reduced. Dong et al claim that it is unlikely that the presence of ultraviolet light, acoustic pressure waves and fluctuations in load current would occur simultaneously for any scenario other than an arc fault. It is envisioned that while a two-classifier approach could be suitable in an aerospace application, any more classifiers would lead to increased cost and a less elegant solution to the wider arc fault detection problem.

2.7.2 Combining Passive Arc Fault Detection Methods

In 2002 Kim presented his work on arc/spark detection within the domestic environment. The tested detection system used multiple methods of arc fault detection featuring three aspects of current analysis (peak current, odd harmonics and broadband noise above 10kHz), and two aspects of voltage analysis (peak voltage and broadband noise above 1kHz), where each of the five measurements are fed into a decision logic block which presents a master arc fault detected signal [195]. Kim follows this one step further and presents a decision rule table that classifies faults into five states "Normal", "Spark", "Arc", "Load-In" and "Load-Out" thus providing fault discrimination. This method is a hardware-intensive solution to the arc fault detection problem, and it is proposed that flight certification of such a complex algorithm would be non-trivial due to the required verification testing.

In 2010 Aihua et al investigated the use of multiple sensors in a low voltage distribution box application where visible light inside the switchboard was monitored with a photo diode, and bus voltage was monitored for arcing using an isolation amplifier [196]. The resultant signals were fed into a PIC microcontroller and a confirmation algorithm was used such that ten concurrent events had to occur within a 2 second period in order to confirm an arc fault. This is an interesting approach for a distribution box application, but the focus of this thesis is on arc fault detection in aircraft electrical wiring, and therefore visible light and bus voltage sensors would be required throughout the aircraft thus leading to an expensive and complex solution.

Andreas et al carried out a review of available arc fault detection techniques in 2012 and found many options including analysis of the temporal and spectral characteristics of the arc current, but since no one of the existing detection methods gives perfect reliability, a generic multi-algorithm detector was created [197]. Discrimination logic is used to decide whether an arc fault is present based on the n detection algorithms in operation.

It is important to note that irrespective of how many different passive arc fault detection schemes are combined, the nuisance trip rate must always be greater than zero due to uncertainty in the arc fault classification process.

2.7.3 Combining Active Arc Fault Detection Methods

Until 2012 researchers focussed on combining unreliable passive detection techniques in order to minimise nuisance trips until Parkey et al investigated the combination of two active schemes, Low Energy High Voltage (LEHV) to provide arc fault detection and Spread Spectrum Time Domain Reflectometry (SSTDR) to provide fault location [198]. The Low Energy High Voltage (LEHV) system applies a high voltage signal to a given wire under test in order to induce a parallel arc between adjacent conductors.

The energy content of the LEHV pulse is similar to that of an Electrostatic Discharge (ESD) event and therefore the LEHV pulse does not provide a threat to hardware connected to the wire under test since aerospace equipment is designed to survive ESD events [198; 199]. In the case of an intermittent series arc in an aerospace application, when the aircraft is on the ground, the intermittent connection may be in place therefore an LEHV pulse will not identify this type of fault and therefore more research is required in this area.

This active method of arc fault and wire fault detection is a promising technology since applying a stimulus to the electrical system and monitoring for a correlated transient response allows for greater certainty that a fault is present. To simplify this technique further, it is proposed to use modulation of the SSPC state in order to provide a stimulus similar to LEHV to the wire under test, and the results of this study are given in Chapter 5.

2.8 Discrimination and Differentiation Methods

Restrepo discusses arc fault detection and discrimination methods in his 2007 paper where the primary concern was hardening arc fault detection algorithms in domestic AC systems against non-hazardous arcing which occurs as part of normal operation loads such as: dimmer circuits, air compressors, vacuum cleaners, electric drills, Broadband over the Power Line (BPL) and RF carriers in the line [33]. Although the load scenarios are identical to those found in aerospace there are a number of synergies which should be considered. Restrepo analyses interfering loads and provides waveforms which look similar to genuine arc fault waveforms. This suggests that monitoring of the current waveform alone is not sufficient to provide robust arc fault detection with no nuisance trip events.

Arc fault detection in photovoltaic (PV) systems has undergone significant research recently as the world is adopting more green power solutions. The favoured detection technique in this sector appears to be FFT based analysis as Johnson et al demonstrate in their 2011 paper [200]. The focus of their work is in the area of series / parallel arc fault differentiation, where the FFT of the output current waveform from a 3kW power converter shows that the levels generated for both series and parallel arcs are comparable making them difficult to differentiate, where the baseline system noise is significantly lower than both the series and parallel arc fault levels. Johnson et al propose three novel methods to differentiate series and parallel faults, the first being combination of high frequency noise analysis with time domain analysis (dI/dt or dV/dt detection techniques as per the work of Strobl and Meckler) [201]. The second method is that of pushing the arcing string off its maximum power point, thus reducing the arc current until a series arc is quenched, or alternatively until a parallel arc fault is confirmed. The third and final method proposed is to permanently

connect parallel PV strings to establish a noise path to the frequency-based arc fault detection hardware thus allowing a trip. These three novel methods require further study such that they can be expanded for use in aerospace applications.

2.9 Nuisance Trips

Arc fault detection devices often suffer from "nuisance trips", or Type I classification errors, where the four states of an arc fault detector are given in Table 2.1. Nuisance trips occur, not in response to a real arc fault, but in response to another event encountered during the operational life of the detector. For example, in domestic dwellings a nuisance trip may be experienced on outlets where a vacuum cleaner is used due to arcing experienced during normal operation of a brushed AC motor.

Arc Fault	**Not Present**	**Present**
Undetected	Normal operation.	Type II error present. (Missed arc)
Detected	Type I error present. ("Nuisance trip")	Successful detection.

Table 2.1: Arc Fault Detection Event Classification

Avoiding nuisance trips is critical to the provision of series arc fault detection systems for aircraft electrical power distribution systems. Based on the author's experience, arc fault detection systems which nuisance trip when installed on an aircraft platform are usually disabled quickly in favour of a robust and available system.

2.9.1 Causes of Nuisance Trips - Acceptable Arcs

A possible cause of nuisance trips is the presence of arcs in a system being monitored by arc fault detection, where the arcing behaviour is part of normal system operation. Arcs are exhibited when a contactor / circuit breaker is opened, and also when the contactor / circuit breaker is closed where "switch bounce" is encountered. Gengenbach et al investigated how different materials and different insulative gases can be used to minimise the effect of arcing in contactors [202]. However, a degree of arcing will always be present when a contactor is switched, so these arcs must be considered.

Since contactor arcs are predictable in aerospace electrical power distribution systems, given that the electrical system controller provides commands to open and close contactors / circuit breakers, and the arcing within contactors is minimised by design, then it is possible to design an arc fault detection system which does not nuisance trip during contactor switching. A possible solution here is to momentarily disable or mask the arc fault detection system output during a switching event, thus preventing nuisance trips.

Brushed motors are an example of a load which exhibits arcing behaviour during normal operation. Naidu et al investigate a series arc fault on a 42VDC brushed engine cooling fan [69]. The brushed motor in this example is well filtered and this is reflected in the smooth current waveform presented. The series arc fault which follows can thus be easily differentiated from the normal motor waveform.

In aerospace systems the rate of change of impedance for a given load on the electrical power distribution system is strictly controlled to prevent the creation of Electromagnetic Interference (EMI) in accordance with RTCA DO-160G [49]. Consequently the fast rate of change of impedance caused by arcs in the motor are masked from the arc fault detection system by an input filter, and thus it is possible to design an arc fault detection system which does not nuisance trip during operation of brushed motors.

Brushless motors are now extensively used on the More Electric Aircraft (MEA) and do not exhibit arcing behaviour as part of normal operation, therefore nuisance trips associated with electric motors are no longer a major consideration [11; 203].

2.9.2 Causes of Nuisance Trips - The Electrical Environmental

EMI is an interfering source for electromagnetic radiation based arc fault detectors, and similarly Electrical Power Variation (EPV) is an interfering source for arc fault detectors based on current and voltage measurement. Two commonly used EPV standards are the US military MIL-STD-704F [204] and the commercial RTCA DO-160G [49]. These standards define power quality in the aircraft electrical power system, where systems are tested in over / undervoltage scenarios and with high levels of harmonic content on the aircraft buses. These tests can induce nuisance trips, especially where tests induce fast changes in output current on a given load, and therefore a given arc fault detection scheme needs to reject these external sources of interference.

Aircraft equipment must withstand lightning induced transients which are tested in detail within RTCA DO-160G Section 22 [49]. This standard covers both direct pin injection and cable bundle tests for multiple transient waveform shapes such as linear attack / exponential decay (Waveform 1, 2, 4 and 5) and damped sinusoids (Waveform 3). The voltage and current threats for each waveform vary depending on the top level requirements of the aircraft, and can extend in order of magnitude from 10A through 1000A and from 10V through 1000V depending on the type of aircraft construction and location of the Unit Under Test (UUT). The transients are also broken down into “single stroke” and multiple stroke” threats. “Single stroke” lightning transients are one-shot events which can easily be ignored by candidate arc fault detection systems. “Multiple stroke” threats contain many lightning transients repeated at typically 1ms intervals. The lightning threats pose two types of threat to arc fault detection systems, firstly overloading of the current and voltage sensors, and secondly the stimulation of an algorithmic susceptibility to the repetitive transient.

Crosstalk between conductors in the electrical power distribution system is an important consideration, where an arc fault on one feeder causes a nuisance trip of the arc fault detection system on an adjacent feeder [35; 205]. Crosstalk can potentially affect all passive electrical arc fault detection schemes. There is no evidence to suggest that it is possible to design an arc fault detection system which doesn't nuisance trip due to crosstalk from arc fault signals on adjacent conductors, and since crosstalk is dependent upon the physical configuration of feeders and loads it would be necessary to understand this configuration when testing the resistance of a given detection system to nuisance trips. Aircraft cable bundles are tightly restrained to prevent vibration damage, and since the position of individual cables in a given bundle cannot practically be tightly controlled to avoid crosstalk, there is a probability that an arc fault on one load feeder could induce nuisance trips on adjacent load feeders. This implies that a nuisance trip free passive detection system cannot be realised without a greater analysis of the interaction between arc faults and cable bundles.

2.9.3 Causes of Nuisance Trips - Passive Electromagnetic Methods

Passive arc fault detection schemes are susceptible to nuisance tripping because they continuously monitor the distribution system for faults, where normal system transients can be mistaken for arc faults. The merits of different passive schemes must therefore be considered.

Detection of electromagnetic radiation can be used as a passive detection method. Kim attempts to characterise the electromagnetic radiation behaviour of low voltage arcing faults with the intention of creating a passive arc fault detection system [133]. Kim demonstrates how electromagnetic radiation is created by arc faults in a lab environment. The aircraft environment suffers from electromagnetic interference (EMI), with noise levels varying depending on where aircraft equipment is installed. An arc fault detection system which relies on detecting electromagnetic radiation from an arc fault is therefore open to detecting electromagnetic interference from external sources which could lead to a nuisance trips.

Electromagnetic Compatibility (EMC) testing is mandated for aerospace electrical systems where a typical military standard for EMC testing is MIL-STD-461E [104]. The author is concerned about radiated susceptibility testing carried out in the range $30\text{MHz} \geq f \geq 1\text{GHz}$ at an electric field strength of $E = 200$ V m^{-1}. In addition to basic Continuous Wave (CW) testing, a 1kHz Amplitude Modulation (AM) tone is used to stimulate parasitic rectification effects within the Unit Under Test (UUT), where any magnetic current sensors will be susceptible to such signals.

The arc fault classifier for a detection system based on electromagnetic radiation behaviour would have to be highly filtered to detect arc faults, and be able to reject high

levels of amplitude modulated EMI while maintaining arc fault detection capability. Based on the author's own experience of radiated susceptibility testing it is concluded that it would be very difficult to design a robust arc fault detection system which is free from nuisance trips by sensing electromagnetic radiation from electric arcs.

2.9.4 Causes of Nuisance Trips - Passive Current / Voltage Methods

Many passive electrical series arc fault detection systems have been implemented and these are discussed in Section 2.4.4. Strobl and Meckler are among the large community of arc fault detection researchers investigating the behaviour of current and voltage waveforms on circuit breaker outputs during arc faults [68]. This approach is passive and therefore requires a very specific classifier to detect arc faults reliably. Strobl and Meckler state that knowledge of the connected load is required to avoid nuisance tripping since the load waveform could exhibit some similarities to that of arc fault waveforms. The author's experience is that electrical load behaviour is poorly controlled during aircraft-level electrical power distribution system design, since historically the reactive load capabilities of electromechanical switches are typically higher than modern solid state power switches, and arc fault detection systems, although under development, are not currently in service at the time of writing.

Many pattern recognition and feature extraction techniques have been employed in an attempt to find a unique characteristic of arc faults that can distinguish them from other system events and these methods are discussed in Section 2.4.4.2 [54]. Examples of feature extraction techniques include wavelet decomposition [149; 150; 148] and Short Time Fourier Transform (STFT) [145; 146]. These schemes have been successfully demonstrated in a laboratory environment in the absence of an EMC threat. The aforementioned pattern recognition techniques do not consider the full range of reactive and active aircraft loads, and therefore could be susceptible to nuisance trips or missed arcs. Fault masking by reactive loads is demonstrated during validation of a passive electrical series arc fault detection system in Section 4.8.

Arunachalam and Diong developed a parametric model approach to arc fault detection for AC and DC systems [166]. However, the detection system may still nuisance trip if the arc fault model correlates with an aircraft load signature. Again this implies that it is not possible to design an arc fault detection algorithm which is free from nuisance trips by sensing current / voltage patterns alone since there is always a risk of incorrect classification.

Ma and Guan have attempted to optimise recognition of arc faults by using a detection algorithm based on neural networks [172]. This would be an ideal way to prevent nuisance trips if it was possible not only to teach the algorithm arc fault characteristics, but also characteristics which are specifically not arc faults. Nuisance

trips remain an issue here unless the detection algorithm is "taught" all possible configurations for electrical loads and all possible combinations and permutations of the aircraft EPV and EMC environment.

2.9.5 The Impact of Nuisance Trips

The impact of nuisance trips in a domestic setting is annoyance to the end user since they will be required to reset the system. However, in an aerospace electrical power distribution system, the impact of a nuisance trip could result in the disabling of a flight-critical system which could ultimately lead to the loss of an aircraft. In reality this risk is mitigated during the electrical power system architecture design since safety is of paramount importance, where the system is designed with redundancy or failure tolerance such that the failure of a single channel will not result in the loss of a flight-critical load. In this scenario the nuisance trip is just a nuisance and would not lead to a major or catastrophic failure condition.

When considering the safety implications of an arc fault detection system it is also important to consider Common Cause Failures (CCF) since these failure types defeat failure tolerant systems [206]. An example of this is a nuisance trip caused by common cause such as common generator transient behaviour, which is seen by both aircraft lanes and could cause the circuit breakers or Solid State Power Controllers (SSPCs) in both lanes of a dual-lane architecture to trip simultaneously. A more likely CCF is a nuisance trip due to a flight critical load with a noisy load current waveform.

This CCF could be addressed by monitoring the health of the adjacent lane and disabling series arc fault detection capability in the event that the first given lane fails. In the absence of this approach it is critical that any circuit breakers in the backup systems protecting the output feeders are simple electromechanical types which do not feature common electronic arc fault protection mechanisms.

In addition to the direct impact of nuisance trips there are also a number of indirect impacts. When an arc fault detector unit trips the ground crew are required to identify the fault before the aircraft can safely fly again. Whether the arc fault detector is fitted to a civil or military platform there is a significant cost associated with this fault-finding process [191]. Every arc fault trip should be investigated until a route cause is found, therefore nuisance trips could have a profound financial and operational implications.

If arc fault detector trips are repetitively traced to nuisance trips then it is possible that this functionality will be disabled due to the cost of tracing the source of the nuisance trip, and the lack of aircraft load availability that nuisance trips cause. This has been the case with previous candidate arc fault detection systems from major aircraft electrical system vendors.

The initial Type II error or nuisance trip can then lead to a further error when the fault is being diagnosed. In the event of a genuine arc fault in the future, this will go undetected and could result in catastrophic damage. A summary of the possible arc fault detection fault finding classifications are given in Table 2.2 for completeness.

Event	**Nuisance Trip**	**Genuine Trip**
No Fault Found	Genuine nuisance trip.	Type II error present. (Missed arc)
Fault Found	Type I error present. (Conincidence)	Successful detection.

Table 2.2: Arc Fault Detection Event Fault Finding Classification

2.9.6 Minimising Nuisance Trips

One widely accepted method of improving resistance to nuisance trips is to use multiple arc fault classifiers, described by Dong et al as the "fusion" method [194]. For example, it is unlikely that the presence of ultraviolet light, acoustic pressure waves and fluctuations in load current would occur simultaneously for any other scenario other than an arc fault.

Detecting arc faults and rejecting nuisance trips is a binary classification problem. When using pattern recognition techniques to classify arc faults and nuisance trips, there is a compromise to be made between sensitivity and specificity. The more sensitive the arc fault detection algorithm is, the higher the nuisance trip rate and the less specific the algorithm is. Conversely, the less sensitive the arc fault detection algorithm is, the lower the nuisance trip rate and the more specific the algorithm is. To design an arc fault detection system for aircraft where nuisance trips are not acceptable it can be deduced that sensitivity must be compromised.

It is important to consider nuisance trips which are caused by improper function of the detection hardware. These events can be reduced by using Built-In Test (BIT) techniques to verify correct operation of the detection hardware prior to activation [207]. Although BIT cannot always provide complete test coverage, it has the ability to detect faulty hardware which could cause both nuisance trips and missed arcs. Furthermore minimising arc fault detection hardware and software complexity will increase the reliability and thus decrease the nuisance trip rate.

Nuisance trips can be minimised further by using multiple levels of AFCB devices with collaborative communications. Kim et al demonstrate a functional multi-level detection system using multiple AFCB devices throughout a power distribution network with successful results [208]. This approach is powerful since interfering nuisance

trip sources would need to affect each level of the distribution system in the same way as an arc fault to produce a nuisance trip event.

For completeness it should be noted that multi-level arc fault detection requires a centralised computing resource which may not be available when retrofitting AFCB devices into legacy aircraft. It also requires each different aircraft architecture to be programmed into the centralised computing resource. This would have to be completed for every aircraft platform onto which the arc fault detection capability is deployed, thus increasing non-recurring engineering design and verification spend significantly.

Nemir et al present an arc fault circuit breaker device which tolerates nuisance trips by using a closed loop control system within a Solid State Power Controller (SSPC) which restores power to tripped loads if the output current falls below a given threshold [65]. This approach is used to extinguish parallel arc faults and to attempt to maintain operation of the load. While this approach can potentially maintain load functionality depending on the severity of the arc fault, there is a risk that this cycling of power will continue indefinitely and cause further damage. This approach is more suited to secondary electrical power distribution where current levels are low, as opposed to primary electrical power distribution where hundreds of Amps are available to cause damage. This scheme also generates poorly controlled switching transients which could impact generator and aircraft network stability and radiate / conduct high RF currents which may interfere with other arc fault detection systems and other critical aircraft systems.

2.10 Trip Coordination

Trip coordination is an area of interest for the author given his experience with I^2t wiring protection and overcurrent trip coordination in SSPC applications where the goal is that a single load fault should only trip the SSPC immediately feeding the load thus allowing the SSPCs in the distribution layers above to remain closed.

In 2010 Kim et al presented a multi-level Arc Fault Circuit Interrupter (AFCI) for a smart grid application based on the implementation of collaborative communication between different AFCIs within the given distribution hierarchy [208]. Kim identified that an arc in a secondary electrical load could cause not only the secondary AFCI to trip, but also the primary AFCI since the change in load current through both the primary and second AFCIs would change and could therefore be detected as arcing behaviour. Kim's solution was to provide collaborative communication between the primary and secondary AFCIs such that if an arc is detected in both the primary and the secondary system simultaneously then only the secondary AFCI needs to trip.

While Kim's solution is elegant, additional wiring in the form of a communication link needs to be in place between the primary and secondary distribution panels in order to communicate the arc fault detection status. A generic modular standalone AFCI would be a more suitable solution since when additional AFCIs are required in a system or when a system needs to be reconfigured, this would require a costly software change to the electrical network controller handling the arc fault trip coordination.

2.11 Certification Considerations

Arc Fault Circuit Breakers and other arc fault detection equipment require certification prior to operation on aircraft platforms. Certification can be granted by the CAA (Civil Aviation Authority) of a given country; the FAA (Federal Aviation Administration) in the United States of America and EASA (European Aviation Safety Agency) in Europe being two examples.

In 2002 Slotte presented on behalf of the FAA at the Enhanced Airworthiness Program for Airplane Systems (EAPAS) conference on certification and implementation of Airborne Arc Fault Circuit Breakers (AFCBs) where he commented that current wire fault inspection and surveillance methods are limited in effectiveness and frequency compared with the continuous protection that AFCBs provide [209]. Slotte also voiced three major installation issues, firstly "common causes of nuisance trips" are a concern where these can be a product of load characteristics, crosstalk (including EMI, lightning and adjacent wiring) and feedback. Secondly "fault masking" is a concern since this is algorithm dependent, and each electrical subsystem supplier will develop their own algorithm which will require certification. Finally "post trip maintenance" is a concern since Slotte proposed that additional non-destructive testing would be required in addition to visual inspection following an AFCB trip.

The proposed FAA certification philosophy was to firstly provide a path for AFCB manufacturers to install AFCBs with their trips disabled, for the purpose of characterising operational electrical system behaviour [209]. Secondly limiting AFCB installation to non-essential systems allows in-service data to be collected to ensure that functionality and reliability goals are achieved. Finally AFCB installation on critical circuits should be limited such that an assumed common-mode nuisance trip does not threaten the safe flight and landing of the given aircraft, which now drives the need for a nuisance trip robust safety architecture design.

In a typical civil aircraft the primary power system loads are safety critical, as these can include flight control systems and flight surface actuators, where in contrast secondary power system loads are non-safety critical loads such as galley ovens and non-essential lighting [11]. This limits the proposed FAA certification philosophy for introduction of series arc fault detection into primary power systems.

The design target for AFCB failure rate depends on where the circuit breaker is located in the electrical system. Moir and Seabridge explain how Functional Hazard Assessment and Fault Tree Analysis are used to determine the required failure rates of given aircraft subsystems [11]. Arc Fault Circuit Breakers on primary electrical loads require a lower failure rate or higher MTBF (Mean Time Between Failure) than Arc Fault Circuit Breakers on secondary electrical loads due to the inherent criticality of primary loads. FAR/JAR25.1309, the airworthiness standard used for certification of the Boeing 737 and Airbus A300 series, dictates that any subsystem fault which leads to catastrophic failure of the aircraft must occur with a probability of no greater than 1×10^{-9} h^{-1} [210]. This is further reinforced by the aerospace recommended practice for civil aircraft development SAE ARP4754 [211]. It is therefore not possible to specify a generic minimum failure rate for an AFCB because it is dependent on the configuration of the electrical system on the given aircraft platform.

2.12 Chapter Summary

Arc fault test methods have been explored and the SAE AS5692 [8] and SAE AS6019 [58] "loose terminal" and ANSI/UL1699 [42] "drawn arc" series arc fault test methods have been identified where this thesis focusses on the realistic loose terminal scenario.

Series arc faults in series with resistive loads cause a reduction in load current since the presence of the arc voltage causes a reduction in the load voltage. Short arcs feature an arc voltage of 15-20V and low voltage DC arcs quench easily because the reduction in load current causes reduced arc power resulting in instability. In high voltage 270VDC systems with short series arc faults it is likely that most arcs with currents above 1A will burn in a stable manner. Increased circuit loop inductance results in more stable arc faults, but the effect of capacitive loads on DC systems has not been fully characterised. The interaction of arc faults with complex SSPC electronics is also not fully understood, and this forms the basis for the characterisation and modelling work in Appendix A and Chapter 3 respectively.

Passive acoustic, visible/ultraviolet light, ionisation and time/frequency domain electrical based arc fault detection methods have been reviewed, demonstrated to be susceptible to nuisance trips, and are often based on empirical data rather than well defined physical arc characteristics. Sensor fusion of multiple passive detection schemes was found to reduce nuisance trip susceptibility. Comparison of electrical system behaviour to prerecorded signals and model reference estimations has delivered improvements in nuisance trip performance, but these schemes are impractical to implement in complex electrical systems. Other passive schemes advocated the use of load voltage sense wires or dual redundant feeder cables to enable arc fault detection, but this is an example of adding wiring to test wiring which reduces system reliability.

ANN and GA learning schemes have been proposed and were found not to provide deterministic classification based on physical arc behaviour.

Active TDR, FDR, NDR, STDR and SSTDR arc fault detection schemes have been used to demonstrate open and short wire fault detection on live wires. However, detection of "soft faults" such as series arc faults has been unsuccessful. Active LEHV and PASD techniques have been demonstrated for offline fault finding. Passive arc fault detection schemes have been demonstrated to be unreliable and active schemes are more promising, but active schemes are limited since they need to operate on live wires and hence a more cost-effective active detection scheme is required. This prompted the concept of SSPC modulation for arc fault detection presented in Chapter 5.

Nuisance trips cost aircraft operators dearly due to time wasted by maintenance crew trying to finding non-existent faults. Nuisance trips have been experienced due to the presence of acceptable arcs such as brushless motor arcing and those found during contactor switching. Nuisance trips have also been found to occur in the presence of EMI / EPV and crosstalk from adjacent load wiring. Active schemes have been found to be more robust against nuisance tripping than passive schemes, although no numerical data was found to support quantitatively. Nuisance trips can be minimised using sensor fusion, BIT (explored in Chapter 5), and/or multi-level detection.

Aircraft certification concerns stem firstly from common causes of failure (CCF) in the AFD system and secondly from nuisance trips. The FAA have proposed a method of introducing series arc fault detection systems onto aircraft using a phased approach where the systems are initially installed for data gathering purposes.

Chapter 3

Behavioural Modelling and Simulation of Series Arc Faults in Aircraft Electrical Power Distribution Systems

3.1 Introduction

3.1.1 Background

When considering the modelling of series arc faults it is important to note firstly that many scientists and engineers have studied the electric arc over the course of the last century with Ayrton and Steinmetz publishing static models of electric arcs in 1902 and 1906 respectively [67; 95]. This work was focussed on the static modelling of electric arcs for both the study of physics and the goal of efficient conversion of electrical energy into light. Cassie and Mayr are recognised for introducing dynamic "energy balance" arc models which are widely used, but are less tangible [212; 213]. The development of electrical arc models continued based on this early work and this is summarised in Section 3.2.

Literature covering DC series arc fault models is sparse and the most relevant literature covers the work of Andrea et al who presented a DC and AC arc fault electrical model based on the Mayr "energy balance" model using a MATLAB® implementation in 2010 [32]. While this model considers both series and parallel arc modelling along with the effect of an Arc Fault Circuit Breaker (AFCB) on the circuit under test, this approach does not consider the impact of modern SSPC electronics on the behaviour of arc faults. Since a typical DC SSPC contains snubber components, leakage components, protection diodes and transient voltage suppressors (TVS) as well as the solid state switching devices themselves, these devices can influence the arc

fault behaviour within the system and therefore a more accurate model is required.

The work carried out in Appendix A has characterised the behaviour of series arc faults in 28VDC and 270VDC electrical systems with a range of resistive, capacitive and inductive loads. A simple equivalent circuit was constructed to support the validation of experimental results gathered during this experiment. In order to better understand the interaction of the series arc fault behaviour and the detailed SSPC hardware configuration it is desirable to model and simulate the representative test scenario developed in Appendix A. Since the thesis is focussed on series arc fault detection this chapter will primarily consider series arc fault behavioural modelling and simulation.

3.1.2 Hypothesis

The hypothesis underpinning this modelling activity is that the electrical characteristics of a series arc introduced into a representative aircraft electrical power system can be modelled using the SPICE simulation system, where parameters such as the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ respond in accordance with the experimental results generated in the series arc fault characterisation study given in Appendix A.

3.1.3 Aims and Objectives

The aim of this chapter is to model and simulate the behaviour of a series arc fault within a DC aircraft electrical power distribution system. In order to achieve this the first objective is to develop a SPICE arc fault system model which allows integration of a parametric, configurable arc model for simulation of series and / or parallel arc faults within existing SSPC and electrical power distribution models. SPICE is typically used for SSPC hardware models since these are component-level models which allow accurate studies of SSPC switching and failure modes to be carried out. It is therefore proposed that a SPICE arc fault model would integrate with existing SSPC models and allow arc fault / SSPC interaction to be simulated. With a candidate arc fault model in place the second objective of the modelling activity is to qualitatively characterise the effect of introducing capacitive, inductive and resistive loads on the SSPC model. The third objective is to simulate the effect of different supply voltages on the SSPC model, and the effect of Electrical Power Variation profiles from RTCA DO-160G Section 18 [49] in the form of bus ripple.

The scope of this work is to qualitatively determine the behaviour of the SSPC hardware in response to series arc faults and not to invest significant effort in equation development and lengthy parameter extraction associated with arc modelling since there is already significant literature in this area. The SPICE models developed shall be demonstrated in DC electrical power distribution systems only covering 28VDC and

270VDC systems and should be scalable such that future 115VAC 400Hz, +/-270V and 230VAC CF 50/60/400Hz and 230VAC VF systems can be modelled without significant modification to the models developed in this work package.

3.2 Literature Review of Arc Models

3.2.1 Static V-I Arc Models

When reviewing electric arc model literature it becomes apparent that scientists and engineers have been carrying out experiments on electric arcs for over a century. Ayrton focussed on developing a simple static electric arc model which is widely cited by modern literature. The Ayrton (1902) arc model describes the static characteristics of the electric arc and is given in Equation (3.1) [67].

$$V_{arc} = A + B\ell + \frac{C + D\ell}{I_{arc}} \tag{3.1}$$

where V_{arc} is the arc voltage, the differential voltage between anode and cathode. I_{arc} is the arc current, A is the sum of the cathode and anode drop, which remains constant with arc length, B is the column voltage gradient, C and D model the arc's non-linear characteristics, and ℓ represents the arc length.

Steinmetz (1906) derived semi-empirical V-I Equation (3.2) based on carbon and magnetite arc experiments, which were focussed on arc lighting applications [95].

$$V_{arc} = A + \frac{C\,(\ell + D)}{I_{arc}^{0.5}} \tag{3.2}$$

The researcher Nottingham (1923) conducted atmospheric arc research on copper-carbon arcs later to produce a generic arc equation similar to that of Steinmetz and Ayrton. The Nottingham model can be derived by setting Ayrton terms B and C to zero, assuming that arc length is constant [9]. Nottingham also postulated that the exponent n is directly proportional to the absolute boiling point of the arc electrode material and the gas in which the arc burns. Tseng observes the literature and makes a bold statement that n cannot be determined with any degree of accuracy due to the variable nature of the phenomenon being studied [214], and electric arcs in aircraft electrical power distribution systems are no exception.

$$V_{arc} = A + \frac{C}{I_{arc}^{n}} \tag{3.3}$$

For longer arcs >15mm, Nottingham proposed that Equation (3.4) is more appropriate.

$$V_{arc} = A + B\ell + \frac{C + D\ell}{I_{arc}^{n}} \tag{3.4}$$

In the years that followed a number of other researchers derived similar variations of the basic equations given by Ayrton, Steinmetz and Nottingham with different values

for parameters A, B, C, D and n. Peelo summarises the future work by Ackerman (1928) [215], Eaton et al (1931) [216], Tretjak et al (1931) [217], Warrington (1931) [218], Abetti (1948) [219], Gerngross (1949) [220], Browne (1955) [221], Maikopar (1960) [222] and Rieder (1967) [223] in his thesis concerning current interruption using high voltage air-break disconnectors [224]. In addition to these researchers, Ammerman et al discuss the later work of Miller and Hildenbrand (1973) [225], Hall, Myers, and Vilicheck (1978) [226], Stokes and Oppenlander (1991) [227] in their IEEE paper regarding DC arc models and incident energy calculations [6]. Similarly, these researchers derived variations of the basic equations given by Ayrton, Steinmetz and Nottingham, with different values for arc parameters A, B, C, D and n to fit the many and varied applications of arc fault modelling, including arc light characterisation and modelling of fault scenarios in electrical power distribution systems, from terrestrial power transmission to trolley lines in coal mines. Static arc models provide a simple method of characterising electric arcs, but this is only one method of arc fault modelling.

3.2.2 Heat-Transfer Arc Models

In addition to static V-I arc models, Cassie and Mayr developed differential equations in order to describe arc resistance R behaviour based on simplified power loss behaviours and energy storage in the arc column. Tseng et al suggest that the heat transfer arc equations are more suitable for simulation of arcs during the strike and extinction / quench phases [214]. Cassie proposes an arc model based on a constant current density, where if the arc length is fixed, then arc current is directly proportional to the cross-sectional area of the arc [212]. Cassie also suggested an arc model with constant resistivity and stored energy density per unit volume [214]. It is assumed that the air flow around the arc penetrated the whole cross section of the arc, carrying the heat away, and thus making the dissipation per unit volume constant. The Cassie equation is given in Equation (3.5).

$$\frac{1}{R}\frac{dR}{dt} = \frac{1}{\Theta}\left(1 - \frac{v^2}{E_0^2}\right) \tag{3.5}$$

where E_0 is the constant steady-state arc voltage, Θ is the arc time constant, the energy stored per unit volume/energy loss rate per unit volume, R is the arc resistance, $\frac{dR}{dt}$ is the derivative of arc resistance R with respect to time, and v is the instantaneous arc voltage.

Tseng et al explain that the Cassie arc model cannot be interrupted and only describes valid behaviour of the arc for large currents. Conversely, for the Mayr model of an electric arc, it is assumed that heat loss only occurs from the periphery of the arc and that the arc conductance varies with the energy stored in it [213]. The Mayr equation

is given in Equation (3.6).

$$\frac{1}{R}\frac{dR}{dt} = \frac{1}{\Theta}\left(1 - \frac{vi}{P_0}\right) \tag{3.6}$$

where P_0 is the constant power loss from the arc, Θ is the arc time constant, the energy stored per unit volume/energy loss rate per unit volume, R is the arc resistance, $\frac{dR}{dt}$ is the derivative of arc resistance R with respect to time, v is the instantaneous arc voltage, and i is the instantaneous arc current.

From Equation (3.6) it can be determined that when instantaneous arc power matches the power loss from the arc $vi = P_0$, the arc resistance remains constant. The steady state characteristics of this differential equation are hyperbolic in similarity with the static V-I models for low current arcs given in Section 3.2.1. In contrast to the Cassie equation, the Mayr equation allows the modelled arc to quench, since when R is large the $\frac{vi}{P_0}$ term can exist below unity allowing a positive $\frac{dR}{dt}$, thus allowing R to climb until the arc is quenched.

It should be noted that Tseng et al suffered from poor convergence during transient simulations using an iterative Newton-Raphson algorithm whenever the arc resistance R is very small during any of the iterations. This was solved by using arc conductance G instead of resistance in their Saber models.

3.3 Initial Investigation - Drawn Arc Study

The author spent considerable time designing a drawn arc simulator illustrated in Figure 3.1 in order to study electric arcs in a controlled test environment prior to attempting to model the "loose terminal" series arc fault scenario.

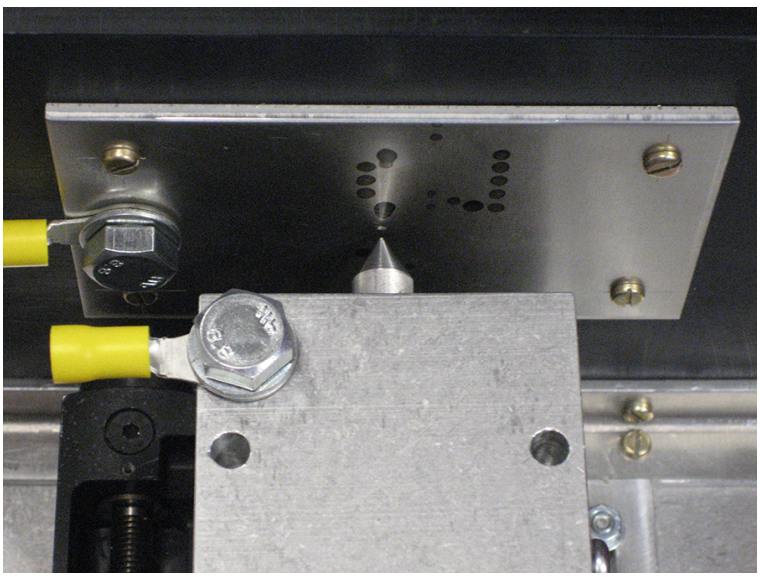


Figure 3.1: Drawn Arc Generator Photograph Showing the Two Arc Electrodes

Figure 3.2 illustrates a side projection of the drawn arc generator, and shows how a stepper motor is coupled to a linear slide actuator which carries a pointed mobile arc electrode 2. Arc electrode 1 is fixed to an insulated right-angle bracket on the left hand side. Full assembly diagrams for the drawn arc generator can be found in Appendix B.4. Both electrodes can be easily replaced and can be constructed from aluminium or copper as required.

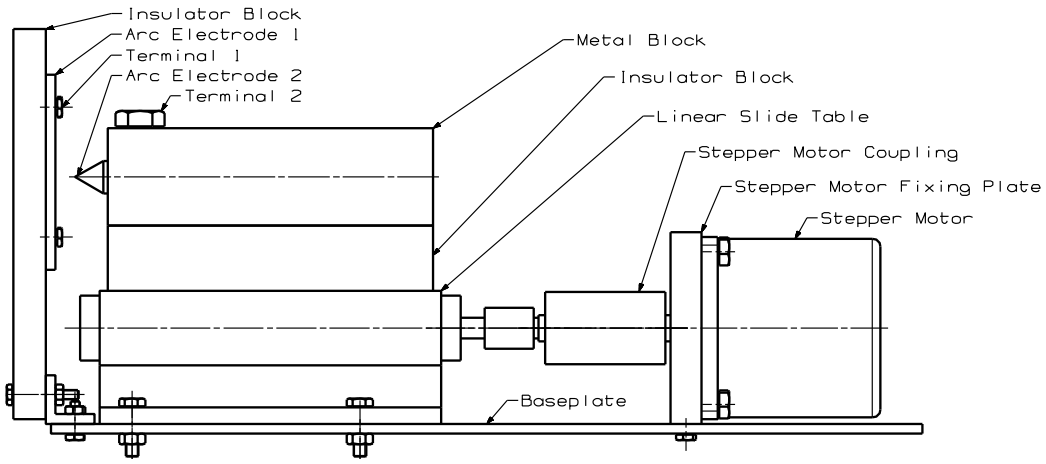


Figure 3.2: Drawn Arc Generator Side Projection Drawing

Figure 3.3: Drawn Arc Generator Software Interface

Figure 3.3 shows the C# software application, designed to control the drawn arc generator hardware, with automated functions to separate the contacts at a known electrode separation velocity v, and to step to a specified arc length ℓ. The software also features manual control based on scroll wheel input from the operator's mouse. Figure 3.4 shows a drawn arc between both copper electrodes and aluminium electrodes, where aluminium arcs generate a white-blue light and copper arcs generate a green light.

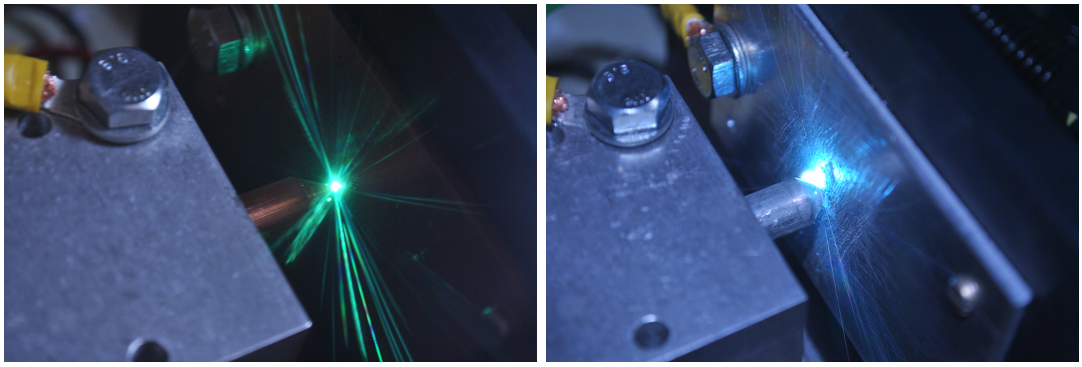


Figure 3.4: Drawn Arcs with Copper Electrodes (Left) and Aluminium Electrodes (Right)

Figure 3.5 shows the schematic configuration of the power supply V_{src}, simplified SSPC model, electrical load, and data acquisition system which monitors arc voltage V_{arc}, arc current I_{loop}, SSPC output voltage $V_{sspcout}$ and load voltage V_{load}.

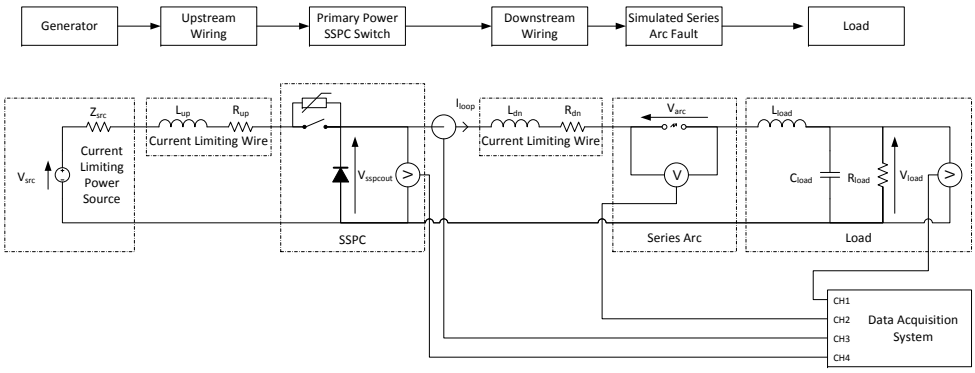


Figure 3.5: Schematic Configuration of the "Drawn Arc" Scenario

Figure 3.6 shows the results for a 270VDC 2A series drawn arc, where the arc separation is plotted alongside arc voltage V_{arc} and arc current I_{arc}, and the arc separation velocity was chosen at 0.75mm/s. In correlation with the static V-I arc models, as arc length is increased, the arc current decreases as arc voltage increases. It was determined from this initial experimentation that faster arc separation velocities lead to higher levels of instability.

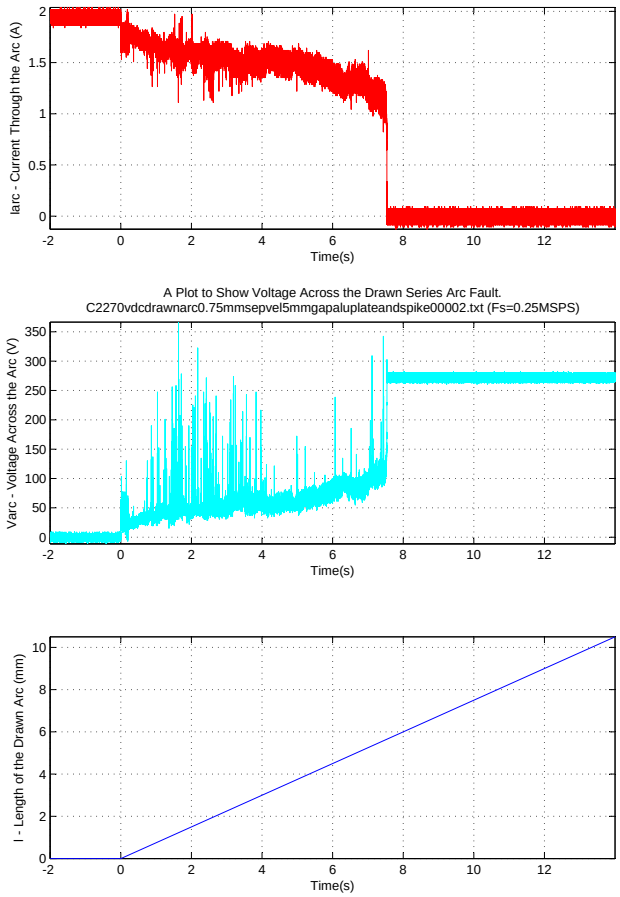


Figure 3.6: Drawn Arc Voltage and Current Over Time for v = 0.75 mm/s

During drawn arc testing with fixed longer arc lengths (>4mm) it was visible to the naked eye that the cathode / anode spots began to move quickly around the surface of the arc electrodes as the path of least resistance between electrodes was found. It was also observed with aluminium electrodes in particular that longer arc lengths caused the aluminium to oxidise, and over time the arc self-quenches causing a reduction in arc current as the arc has to gain length to find low resistance non-oxidised electrode material.

3.4 Arc Fault Model Development and Methodology

3.4.1 SPICE-Compatible Arc Equation Development

From the literature it can be determined that modelling arc faults in electrical power distribution systems is a complex affair. The requirement to use SPICE models for SSPC model integration leads to the consideration of traditional static V-I characteristics for the SPICE arc fault model, since heat loss models require parameter extraction based on physical properties of the arc which would take considerable analysis of experimental arc fault waveforms. Since each arc from the loose terminal scenario

is different, it seems that there is little value in carrying out heat loss modelling. It should also be noted that during the arc model literature review exercise no reference was found with regard to implementation of Cassie or Mayr arc models in SPICE, and furthermore the SPICE documentation shows that there is no built-in support for handling the differential resistance equations given in Equations (3.5) and (3.6) respectively [228].

From the literature review it was determined that, following the early work of Ayrton and Steinmetz, Nottingham developed a general arc equation into which five parameters can be inserted to describe the static V-I characteristic of a given arc. Now consider the implementation of the Nottingham expression in Equation (3.4) in SPICE, assuming that parameters A, B, C, D and n are known. In the first case where arc current I_{arc} is greater than or less than zero, the arc voltage V_{arc} can be determined by computing the solution to Equation (3.4). For the second case where arc current I_{arc} tends to zero, an asymptote is encountered which suggests that arc voltage tends to infinity.

Arc voltages measured during all experimental work in this thesis were carried out using a differential voltage probe with a high input resistance and low input capacitance. Although the effect of the differential voltage probe used for arc voltage monitoring in Appendix A was minimised by design it still affected the behaviour of arc voltage V_{arc}, and thus during experimental arc extinction the arc voltage did not tend to infinity. It is proposed that this is due firstly to probe capacitance which bypasses the arc current path thus allowing the arc to quench more readily, secondly due to the finite sampling period of the signal recording equipment which limits the recorded peak arc extinction voltage, and thirdly due to bandwidth limiting in the differential voltage probe amplifier which limits the measurement of fast transient voltages. The probe characteristics should therefore be modelled in an integrated SPICE system model to further quantify the influence of the probe.

For the proposed arc fault model the arc current levels of interest are $I_{arc} \geq 0.1\text{A}$, and therefore a minimum modelled arc current $I_{min} = 1\text{mA}$ can be assumed which limits the maximum arc voltage to a finite value far in excess of the proposed line voltages modelled in this work. For the purposes of a unipolar arc fault SPICE model where arc current only flows in the positive direction, Equation (3.8) can be achieved by substituting Equation (3.7) into Equation (3.4). While this is not the most elegant solution, Equation (3.8) can be easily implemented in SPICE.

$$I_{arc} = I_{arc} + I_{min} \tag{3.7}$$

$$V_{arc} = A + B\ell + \frac{(C + D\ell)}{(I_{arc} + I_{min})^n} \tag{3.8}$$

Whilst at first it may seem that a unipolar model is appropriate for a DC electrical power distribution system, in Appendix A it was demonstrated that the introduction

of reactive loads can lead to resonance in the loop current during arcing and switching events, and therefore a bipolar arc model is required to ensure qualitatively accurate behaviour during transient simulation. To realise a bipolar model further complexity is required to ensure that firstly the arc voltage V_{arc} is calculated for an absolute value of arc current $|I_{arc}|$, taking into account the minimum arc current I_{min} and this is illustrated in Equation (3.9). To determine the polarity p of the arc voltage V_{arc} the arc current I_{arc} can be divided by the absolute arc current $|I_{arc}|$. However, the SPICE engine cannot evaluate the division for $I_{arc} = 0$A, and therefore a small but insignificant offset $I_{os} = 1\mu$A also needs to be introduced to allow computation of Equation (3.10).

$$V_{arc} = A + B\ell + \frac{(C + D\ell)}{|I_{arc} + I_{min}|^n} \tag{3.9}$$

$$p = \frac{I_{min}}{|I_{min}| + I_{os}} \tag{3.10}$$

Combining Equation (3.9) and (3.10) in Equation (3.11) yields Equation (3.12), which defines the bipolar arc fault model, where the limited arc voltage can be defined by careful selection of the I_{min} parameter.

$$V_{arc} = p\left[A + B\ell + \frac{(C + D\ell)}{|I_{arc} + I_{min}|^n}\right] \tag{3.11}$$

$$\therefore V_{arc} = \frac{I_{arc}}{|I_{arc}| + I_{min}}\left[A + B\ell + \frac{(C + D\ell)}{|I_{arc} + I_{min}|^n}\right] \tag{3.12}$$

Care must be taken when utilising this model under different test scenarios since the accuracy of the arc voltage V_{arc} will be limited for very small values of I_{arc}. The author does not consider this to be problematic for the purposes of the SPICE model since at low arc current levels the arc voltage is highly dependent on the physical environment (atmospheric pressure, temperature, electrode position, velocity, material, level of oxidation etc) at the electrodes, which is yet another factor which complicates prediction of the arc extinction voltage.

3.4.2 Model Interface Definition

The first step in creating a non-linear continuous SPICE arc model implementation is to create an interface definition of the model. Figure 3.7 shows the interface definition for the proposed non-linear continuous SPICE arc model. It is proposed that the arc model has two power terminals “power terminal 1” and “power terminal 2” which allow current to flow bidirectionally through the arc model. The arc model determines arc voltage for a given current flowing through the arc model. Standard anode and cathode notation is not appropriate here since during AC arc faults, the arc polarity (anode and cathode) can invert for each half cycle.

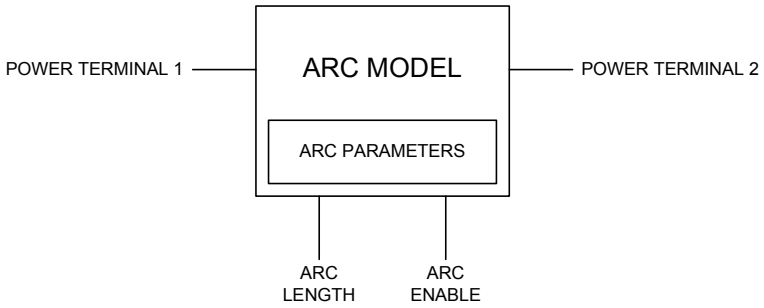


Figure 3.7: Arc Linear SPICE Model Interface

The arc model also features two additional inputs, the "arc enable" and "arc length". The "arc enable" input is a 5V logic level input which allows the arc to strike and reconnect as required. The "arc length" input defines the length of the arc in metres, and this can be modulated arbitrarily during transient simulation. Finally the arc model contains a set of arc parameters which allow the model to be preconfigured for a specific test case at the point of model-compilation, these are the values of A, B, C, D and n in accordance with the hybrid arc model outline in Section 3.4.1. It is envisioned that these parameters could be added to the arc model interface in the future to enable parameter changes during simulation run-time.

3.4.3 Model Implementation Options

Due to the asymptote which occurs as I_{arc} tends to zero, the implementation of the SPICE arc model is not trivial. The author considered two approaches to implementing the model where firstly a Look-Up Table (LUT) approach allows explicit definition of arc V-I characteristics over the desired range of arc current I_{arc} and arc voltage V_{arc}. In the author's experience LUT models run quickly in comparison with computation of linear equations containing many multiplication stages since they only require processing time to address the data table and to read back the output value. The main issue with the LUT model is that SPICE caters only for a one-dimensional LUT, which allows arc voltage V_{arc} to be determined from the single arc current I_{arc} input. This is acceptable for the scenario where arc length ℓ is small and/or fixed, and indeed for the loose terminal scenario arc length ℓ can be assumed to be small. Substituting $\ell = 0$ into Equation (3.12) gives Equation (3.13).

$$\therefore V_{arc} = \frac{I_{arc}}{|I_{arc}| + I_{min}} \left[A + \frac{C}{|I_{arc} + I_{min}|^n} \right] \tag{3.13}$$

If longer arcs are to be considered then arc voltage V_{arc} must be modelled as a function of both arc current I_{arc} and arc length ℓ, and in this case a two-dimensional LUT is required. This feature is unavailable in SPICE, but MATLAB® does offer multidimensional LUT capability should this approach be desired for future research [229].

3.4.4 LUT-Based Model Implementation

Figure 3.8 shows a proposed diagram of a SPICE subcircuit which complements the interface diagram given in Section 3.4.2.

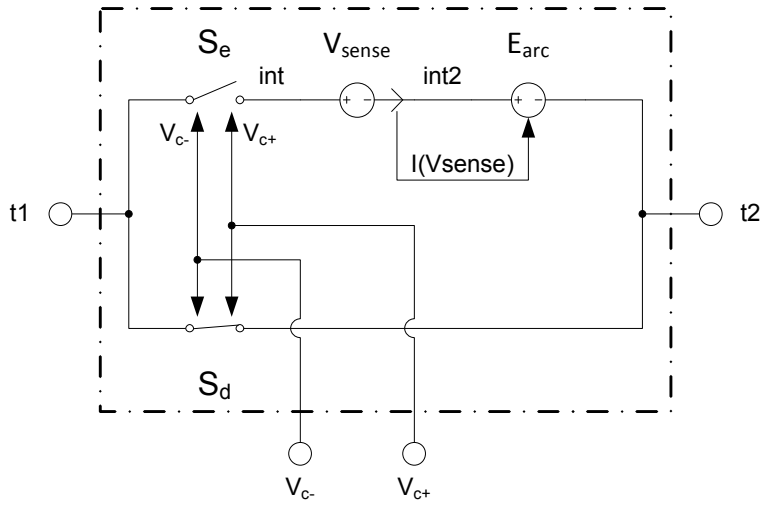


Figure 3.8: LUT-Based SPICE Arc Model Schematic

First of all t1 and t2 show the input / output terminals for the arc model. Application of 0V to the active-high enable signal (between V_{c+} and V_{c-}) results in the closing of switch S_d and the opening of switch S_e. The switch primitive model provided by the SPICE language requires an open and a closed resistance, so assume that $R_{open} = 1\text{G}\Omega$ and $R_{closed} = 1\text{n}\Omega$ respectively, where these resistance values are chosen to ensure that the switches have minimal impact on model accuracy. The threshold of these switches are set at 2.5V with $\pm 100\mu$V hysteresis to prevent oscillation of the simulation during switch transitions. The switches provide a changeover function which allows the arc model to be switched in and out of circuit, thus simulating an arc gap or a short circuit. Modulating the arc enable signal allows simulation of a loose terminal series arc fault scenario.

When the arc enable signal is set to 5V the arc model is switched in. This consists of a zero-voltage voltage source V_{sense} which is used for current monitoring purposes. There is also a Voltage Controlled Voltage Source (VCVS) E_{arc} which implements the hybrid arc model presented in Section 3.4.1. The parameters A, B, C, D and n are hard-coded into the SPICE model and this model simply determines arc voltage V_{arc} through a LUT function based on the arc current I_{arc}.

3.4.5 Non-Linear Continuous Transfer Function Implementation

Figure 3.9 shows a proposed diagram of a SPICE subcircuit which complements the interface diagram given in Section 3.4.2.

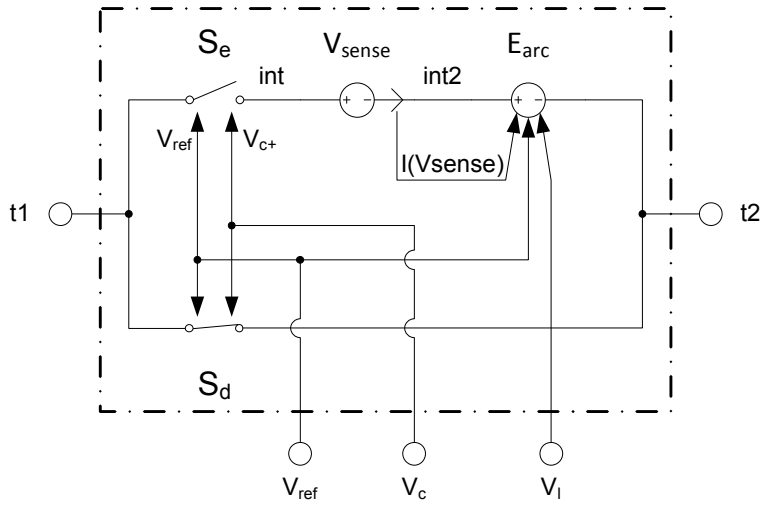


Figure 3.9: Non-Linear Continuous SPICE Arc Model Schematic

Similarly to the LUT model in Section 3.4.4, t1 and t2 form the input / output terminals for the arc model and the changeover switching function of this arc model is common with that in the LUT model. Unlike the LUT implementation this model is capable of modelling varying arc length during simulation time. The differential voltage between V_l and V_{ref} determines the arc length, which is fed into E_{arc} along with the current monitor signal from V_{sense}, and voltage is produced across the VCVS terminals which is calculated by implementation of the non-linear continuous transfer function in Equation (3.12) representing the modelled arc voltage.

3.4.6 Curve Tracer / Model Testbench Implementation

To promote the ease of use of the SPICE arc model a "curve tracer" was implemented in order to both visualise and verify that the arc V-I curve for a given set of arc parameters is consistent with that expected. The simple SPICE schematic illustrated in Figure 3.10 verifies that the arc model subcircuit is configured correctly, and is behaving as expected by performing a "DC sweep" of source I1, with the arc length set by V2 and the arc permanently enabled using V3. Data is captured by differential voltage probe V_ARC and current probe I_ARC and the two signals are plotted against each other in XY mode.

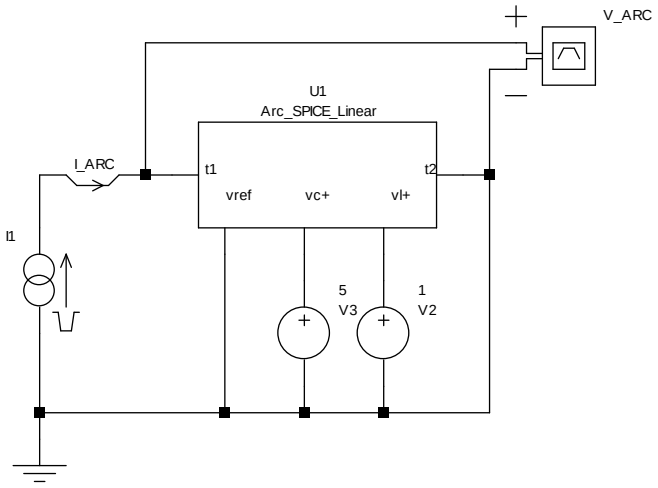
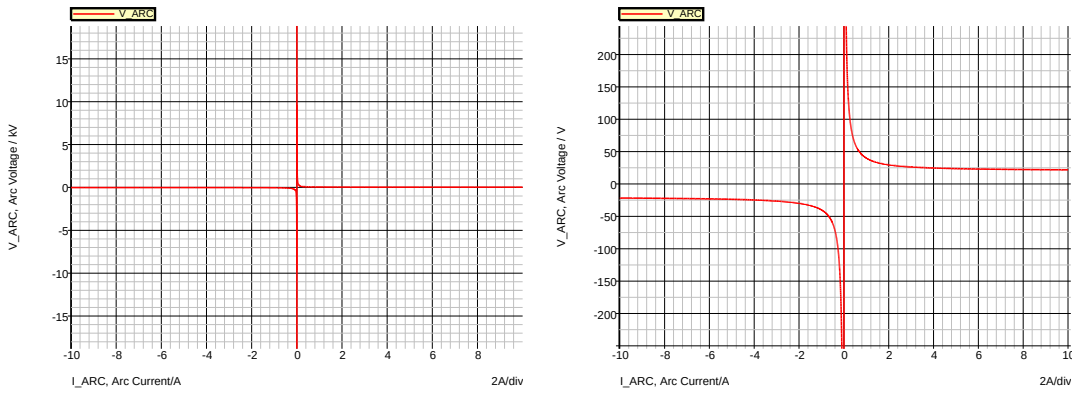


Figure 3.10: SPICE Arc Model Curve Tracer / Testbench

Figure 3.11 shows both a full scale V-I plot for a typical arc with current in the range -10A through 10A given the arbitrary parameters $A = C = 10$, $n = 0.5$ and $B = D = L = 0$. A further detailed plot showing arc voltage in the range -250V to +250V is provided for clarification. The plot shows how arc voltage V_{arc} decreases for increasing values of arc current I_{arc}, and this is the archetypal negative differential impedance arc characteristic. When modelling a specific arc scenario, arc parameters A, B, C, D and n need to be extracted from experimental test data, and this can be performed by visual inspection and successive approximation of a given set of test waveforms. The results of such parameter extraction are described in the results and discussion sections of this document in Sections 3.5 and 3.6 respectively.



(a) Full Scale Arc Voltage V_{arc} Range

(b) +/-250V Arc Voltage V_{arc} Range

Figure 3.11: SPICE Arc Model Curve Tracer / Testbench Sample Plot for the Case $A = C = 10$, $n = 0.5$, $B = D = L = 0$

3.4.7 Extracting and Modelling the Chaos Element

The model developed so far covers modelling of single arc events which may be relevant for a "drawn arc" or "wire break" scenario, but for the loose terminal scenario a random element is required to model the period and duration of arcs. It was discovered during the loose terminal experimental work carried out in Appendix A that there is an interaction between the electrical and mechanical behaviour of any arc fault. Qualitatively it was observed that at lower arc currents (<5A) this interaction was minimal, and as arc current rises, the interaction becomes greater and this skews the arc duration / period distribution. It was noted after a short time testing experimentally that this interaction is incredibly complex and the interaction is exacerbated by the random vibration profile used for loose terminal testing. In reality there are a vast number of different possible cable configurations on aircraft when considering varying wire gauge, wire material, sheath material, fixing arrangements and the actual vibration profile seen by the wire fault. Developing a model which covers all of these scenarios is out of scope for this project, and it was proposed that a simple robust scheme would be better than a sophisticated method which is hard to validate.

For the purposes of understanding arc fault electrical behaviour the decision was made to generate an "arc enable" signal from experimental data and create a SPICE digital signal source based directly upon this, thus enabling the electrical impact of a realistic arc profile on a typical SSPC to be investigated. The process in Figure 3.12 can be used to generate arc period and arc duration data from arc voltage V_{arc} data recordings. The arc period and arc duration data can written to a ".dig" file which is read during simulation run-time by a SPICE "Digital Signal Source" designated "A" by the SPICE language [228].

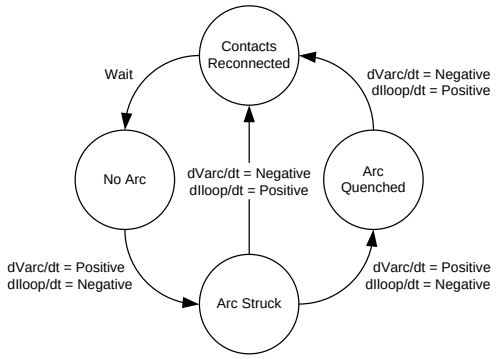
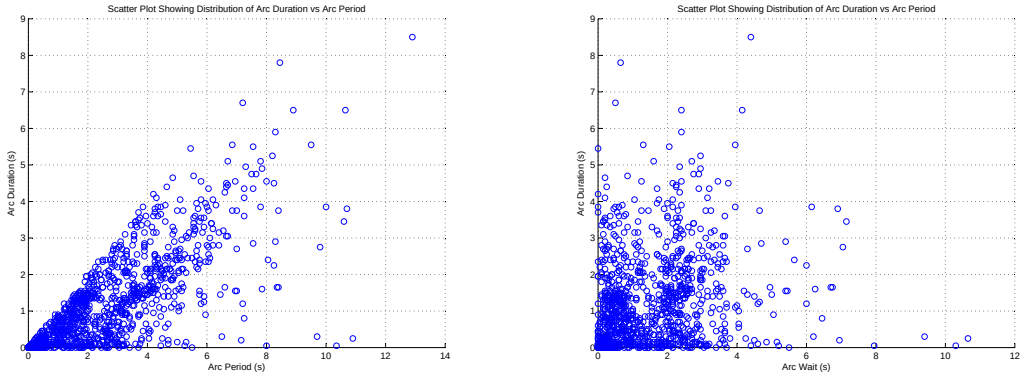


Figure 3.12: State Diagram for Arc Waveform Analysis

Using a typical loose terminal series arc fault arc voltage V_{arc} recording it is possible to generate a scatter plot demonstrating the distribution of arc period against arc duration and arc duration against arc wait respectively. The author defines arc period

as the time between consecutive arc events, arc duration as the time between arc strike and arc quench / extinction and arc wait as the time between arc quench / extinction and the following arc strike.



(a) Arc Duration vs Arc Period

(b) Arc Duration vs Arc Wait

Figure 3.13: Example Scatter Plot Showing Experimental Arc Data for a 270VDC 2.5A Loose Terminal Series Arc Fault

MATLAB® was used to perform feature extraction on the arc voltage recordings and then to plot Figure 3.13, which illustrates how the distributions vary with the mechanical and electrical configuration of the test environment. The distribution presented is arbitrary for demonstration purposes and in the three second recording 1054 arc events were captured. The extracted arc periods and durations can be used to build a SPICE "Digital Signal Source" input file using MATLAB® and the SPICE simulator output from this can be observed in Figure 3.14. The MATLAB® script illustrated in Appendix B.7 also auto-codes a corresponding SPICE subcircuit model referencing the ".dig" input file, thus bridging the MATLAB® feature extraction data and the SPICE simulator.

Figure 3.14: SPICE Representation of an "Arc Enable" Signal for a 270VDC 2.5A Load Loose Terminal Scenario

Figure 3.15 shows the MATLAB® feature extraction script output where strike / quench events have been identified. Viewing the two figures together allows a visual comparison of the arc voltage V_{arc} waveform and the proposed SPICE "Digital Signal Source" output and it is apparent that the two signals are well aligned.

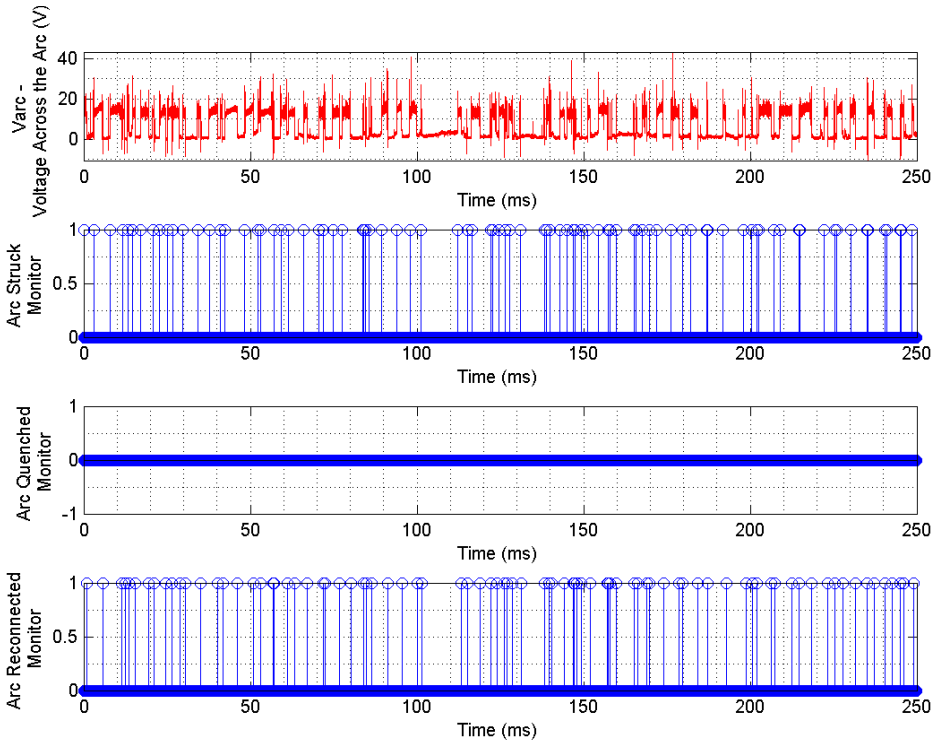


Figure 3.15: Sampled Arc Voltage Waveform Showing Feature Extraction Signals for a 270VDC 2.5A Load Loose Terminal Scenario

3.4.8 Transmission Line Model for DC Aircraft Power Distribution

Where circuit analysis of series arc faults is required, it is important to consider the sources of stored energy in the system, and this includes the electrical wiring used to connect the system under test. To permit the system behaviour during a series arc fault event to be understood a transmission line model is required to model the system wiring. The traditional generic lumped transmission line model is given in Figure 3.16 as illustrated by Paul [7].

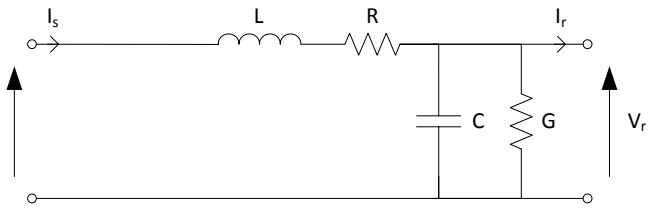


Figure 3.16: Typical Transmission Line Model

The generic model presented by Paul characterises a length of two-conductor transmission line. A lumped model rather than a distributed transmission line model can

be used because the wavelengths of interest here are long in comparison to the transmission line length. The model has four per-unit-length parameters designated the "primary line constants":

- L - Inductance per unit length due to the magnetic field created around the wires, and self-inductance.
- R - Resistance per unit length created by the finite resistivity of the two conductors.
- C - Capacitance per unit length between the two conductors.
- G - Conductance per unit length of the dielectric material(s) separating the two conductors.

It is common practice in DC aircraft electrical power system design to use a simplified configuration of the traditional transmission line model since power feeder lengths are minimised in order to avoid power losses due to cable resistance. Chakrabarti and Halder present the simplified model titled "short transmission line model", where an assumption has been made that per-unit-length capacitance C and per-unit-length conductance G may been ignored due to the short cable lengths involved [2]. The per-unit-length capacitance can further be ignored because the per-unit-length inductance dominates where the separation between wire and return is large, and therefore the simplified "short transmission line model" is more applicable to turn on/off events where the focus is on the transient response of the wiring system. This "Short Transmission Line Model" is illustrated in Figure 3.17 and in industry is also commonly referred to as the "current limiting wire model".

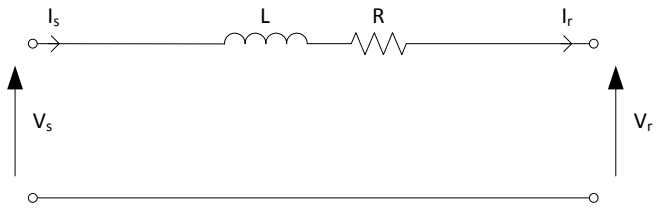


Figure 3.17: Simplified "Short Transmission Line Model" [2]

The values of R and L used for this model are dependent upon the gauge of wire used, the length of the cable and the material from which the cable is made. In aluminium aircraft with DC electrical power systems, the return current from these DC loads typically returns through the chassis, and therefore the transmission line model of the feeder wiring can be approximated as a wire running parallel to a ground plane. Derivations for aircraft wiring resistance R and inductance L are provided in Appendixes B.1 and B.2 respectively.

Example Transmission Line Parameters

Taking a realistic example transmission line to demonstrate the order of magnitude of upstream and downstream inductances, first consider the dimensions of a commercial airliner such as a Boeing 747 which has a wingspan of 59.6m and an overall length of 70.6m [230]. Assuming that the aircraft features 270VDC generators rather than the current 115VAC 400Hz three-phase configuration, that the electrical power distribution panel containing 120A PEPDC/PEPSC SSPC modules is in the centre of the fuselage, and that a load is mounted in the nose of the aircraft, this gives a load cable length of approximately 30m, with a typical wire gauge of 4AWG. Similarly the length of the upstream cable between the generators on outer engines 1 and 4 respectively and the electrical power distribution panel can be estimated as 20m, with a typical wire gauge of 0AWG. The resistance R and inductance L parameters for both a 30m 4AWG and 20m 0AWG section of copper wire mounted at an estimated 0.02m above the aircraft chassis (ground plane) can be computed.

First compute the cross-sectional areas, A_{4AWG} and A_{0AWG}, of the 4AWG and 0AWG wires from Equations (3.14) and (3.15) respectively.

$$A_{4AWG} = \left(1.2668 \times 10^{-8}\right) \times 92^{\frac{36-4}{19.5}} = 2.115 \times 10^{-5} m^3 \tag{3.14}$$

$$A_{0AWG} = \left(1.2668 \times 10^{-8}\right) \times 92^{\frac{36-0}{19.5}} = 5.348 \times 10^{-5} m^3 \tag{3.15}$$

Next compute the radius r_n of the 4AWG and 0AWG wires, r_{4AWG} and r_{0AWG}, from Equations (3.17) and (3.18) respectively.

$$r_n = \frac{d_n}{2} = \frac{\left(1.27 \times 10^{-4}\right)}{2} \times 92^{\frac{36-n}{39}} \tag{3.16}$$

$$r_{4AWG} = \frac{\left(1.27 \times 10^{-4}\right)}{2} \times 92^{\frac{36-4}{39}} = 2.59 \times 10^{-3} m \tag{3.17}$$

$$r_{0AWG} = \frac{\left(1.27 \times 10^{-4}\right)}{2} \times 92^{\frac{36-0}{39}} = 4.13 \times 10^{-3} m \tag{3.18}$$

Now compute the resistance R per-unit-length of the 4AWG and 0AWG wires, R_{4AWG} and R_{0AWG}, from Equations (3.19) and (3.20) respectively.

$$R_{4AWG} = \frac{\rho}{A} = \frac{\rho_{copper}}{A_{4AWG}} = \frac{1.7248 \times 10^{-8}}{2.115 \times 10^{-5}} = 0.82 m\Omega/m \tag{3.19}$$

$$R_{0AWG} = \frac{\rho}{A} = \frac{\rho_{copper}}{A_{0AWG}} = \frac{1.7248 \times 10^{-8}}{5.348 \times 10^{-5}} = 0.33 m\Omega/m \tag{3.20}$$

Next compute the total line resistance R of the 30m 4AWG and 20m 0AWG wires, $R_{4AWG,30m}$ and $R_{0AWG,20m}$, from Equations (3.21) and (3.22) respectively.

$$R_{4AWG,30m} = R\ell = 0.82 \times 30 = 24.6 m\Omega \tag{3.21}$$

$$R_{0AWG,20m} = R\ell = 0.33 \times 20 = 6.6 m\Omega \tag{3.22}$$

With the 120A load applied to the PEPDC/PEPSC SSPC modules then the voltage drops along the two resistive cable options with a 120A current flowing are in the order of 1V, and therefore wire resistance is not critical to the integrated SSPC series arc fault model based on the realistic resistance values calculated in Equations 3.21 and 3.22 for the Boeing 747 example.

Now compute the inductance L per-unit-length of the 4AWG and 0AWG wires, L_{4AWG} and L_{0AWG}, from Equations (3.23) and (3.24) respectively.

$$L_{4AWG} \backsimeq \frac{\mu}{\pi} \ln\left(\frac{2h}{r_w}\right) \backsimeq \frac{4\pi \times 10^{-7}}{\pi} \ln\left(\frac{2 \times 0.02}{r_{4AWG}}\right) \backsimeq 1.095 \times 10^{-6} H/m \tag{3.23}$$

$$L_{0AWG} \backsimeq \frac{\mu}{\pi} \ln\left(\frac{2h}{r_w}\right) \backsimeq \frac{4\pi \times 10^{-7}}{\pi} \ln\left(\frac{2 \times 0.02}{r_{0AWG}}\right) \backsimeq 0.908 \times 10^{-6} H/m \tag{3.24}$$

Finally compute the total line inductance L of the 30m 4AWG and 20m 0AWG wires, $L_{4AWG,30m}$ and $L_{0AWG,20m}$, from Equations (3.25) and (3.26) respectively.

$$L_{4AWG,30m} = L\ell = \left(1.095 \times 10^{-6}\right) \times 30 = 32.85 \times 10^{-6} H \tag{3.25}$$

$$L_{0AWG,20m} = L\ell = \left(0.908 \times 10^{-6}\right) \times 20 = 18.16 \times 10^{-6} H \tag{3.26}$$

To account for a "worst case" scenario the maximum upstream L_{up} and downstream L_{dn} wiring inductances from the SSPC under test have been assumed to be 50μH, thus providing some margin over the realistic inductance values calculated in Equations 3.25 and 3.26 for the Boeing 747 example.

3.4.9 SSPC Model Integration

Figure 3.18 illustrates a typical SSPC configuration along with one possible implementation of transient voltage protection. Note that the semiconductor switching element is assumed to be a perfect switch $S1$, modelled by a very low impedance whose exact value depends upon the number of semiconductor devices used and their respective on-resistances. It is not necessary to model the dynamic characteristics of the MOSFET devices used in the SSPC because the series arc fault is assumed to be present when the switch is fully closed. If a simulation was required where the SSPC is switched in the presence of a series arc fault then further SSPC model detail would be required.

Line Power / Upstream Cable Inductance

Line power is provided by voltage source V1 through an inductor L1 which models the SSPC input feeder impedance into switch S1. It is assumed cable resistance is negligible compared with other resistances in the schematic and it is therefore omitted. Voltage source V5 is provisioned for simulation of arbitrary source ripple voltages.

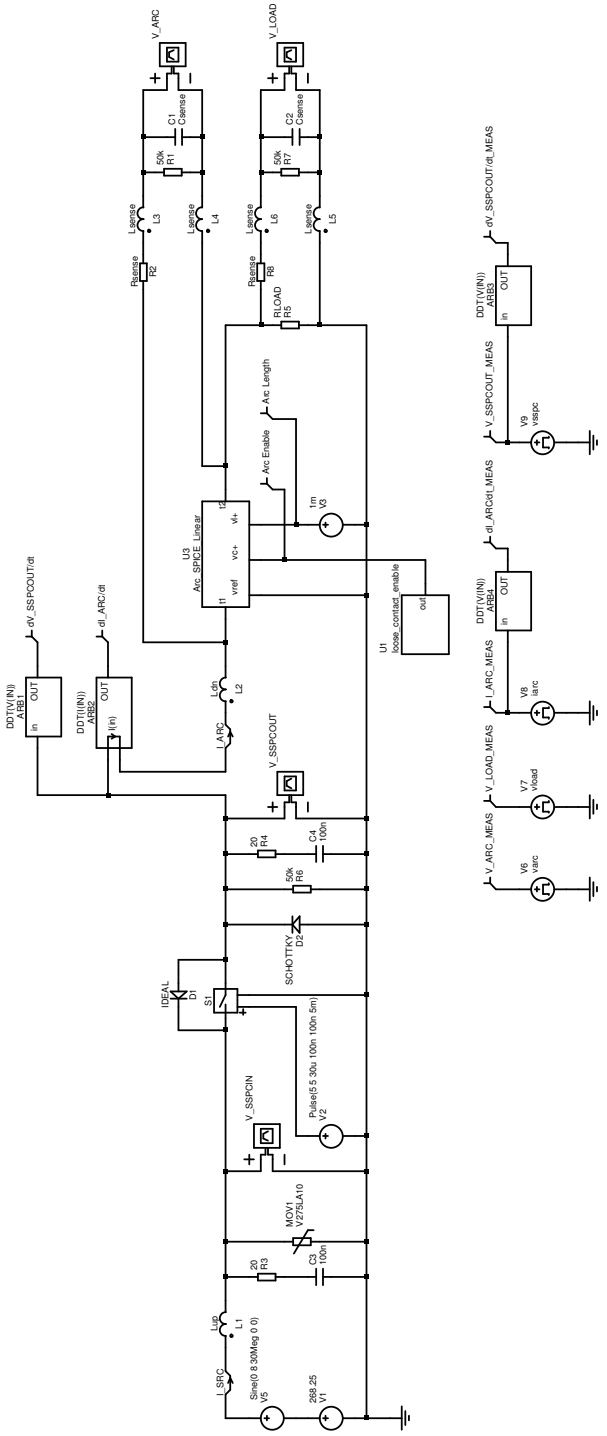


Figure 3.18: SPICE Arc Model Integrated Into SSPC Model (Series Arc)

Input Snubber

Resistor R3 and Capacitor C3 form a snubber function and values chosen are typical for SSPCs with current switching capability up to 120A. The snubber stabilises the line impedance dominated by L1 during switching transients generated by SSPC switch S1. Snubber components are not typically used in electromechanical systems.

Transient Voltage Suppression (TVS)
The Transient Voltage Suppressor (TVS) / Metal Oxide Varistor (MOV) device MOV1 limits the voltage across S1 during switching events created by the change in current through L1 to protect the semiconductor switch S1 from breakdown.

SSPC Output Current / Voltage Differentiator
ARB2 is a Current Controlled Voltage Source (CCVS) which enables a $\frac{dI}{dt}$ signal to be created for monitoring purposes. Similarly ARB1 is a Voltage Controlled Voltage Source (VCVS) which enables a $\frac{dV}{dt}$ signal to be produced again for monitoring purposes.

Current Monitor / Downstream Cable Inductance
After current has passed through switch S1 it flows through the non-intrusive element ARB2 to the load feeder cable modelled by L2 where again the cable resistance has been assumed to be negligible and can easily be inserted if required.

Arc Model
Current then flows through the arc model U3 as described in Section 3.4.5 to the load which is represented in this example case as a purely resistive load R5.

Output Snubber
Resistor R4 and Capacitor C4 form a snubber function where values chosen are typical for SSPCs with current switching capability up to 120A. This snubber stabilises the load feeder cable impedance dominated by L2 during switching transients from S1.

Leakage Current Management
Resistor R6 is provisioned in order to dissipate the DC leakage current of semiconductor switch S1.

Anti-parallel Diode
Diode D1 provides a low impedance reverse path across main SSPC switch S1 in order to steer any unwanted transients at the switch S1 output of magnitude greater than V1 back to voltage source V1 without passing through the semiconductor S1.

Flywheel Diode
Diode D2 commutates current through L2 during a switch S1 turn-off event.

Current and Voltage Probes
Fixed circuit probes are provided in the model in order to monitor behaviour of the model under different test scenarios, where...

- **I_ARC** is the current flowing through the arc.
- **I_SRC** is the current flowing out of the voltage source V1.

- **V_SSPCIN** is the voltage between the SSPC input and chassis.
- **V_SSPCOUT** is the voltage between the SSPC output and chassis.
- **dV_SSPCOUT/dt** is the rate of change of SSPC output voltage V_SSPCOUT with respect to time.
- **dI_ARC/dt** is the rate of change of arc current I_ARC with respect to time.
- **V_LOAD** is the voltage across the load where R8, L5, L6, R7 and C2 model the typical experimental probe characteristics for results comparison purposes.
- **V_ARC** is the voltage across the arc where R2, L3, L4, R1 and C1 model the typical experimental probe characteristics for results comparison purposes.
- **ArcLength** is a voltage representing the length of the arc gap.
- **ArcEnable** is a 5V logic signal which enables and disables the arc.

3.5 Series Arc Fault / SSPC Simulation Results

Tables 3.1 and 3.2 show the parametric configuration of the experimental and simulation results presented in this section, covering both the drawn series arc and loose terminal series arc fault scenarios respectively. Results for scenarios 1 through 3 are given in this section, and results for scenarios 4 through 11 are available in Appendix B.9.

Scenario Number	V_{src} (V)	R_{load} $(A(\Omega))$	L_{load} (μH)	C_{load} (μF)	L_{up} (μH)	L_{down} (μH)	**Results Figure**
1	270	2.5 (108)	12	0	4.25	12	3.19

Table 3.1: Summary of Drawn Arc Series Arc Fault Test Scenarios

Scenario Number	V_{src} (V)	R_{load} $(A(\Omega))$	L_{load} (μH)	C_{load} (μF)	L_{up} (μH)	L_{down} (μH)	**Results Figure**
2	28	2.5 (11.2)	12	0	4.25	12	3.20
3	270	2.5 (108)	12	0	4.25	12	3.21 / 3.22
4	28	2.5 (11.2)	12	100	4.25	12	B.5
5	28	2.5 (11.2)	62	0	4.25	12	B.6
6	270	2.5 (108)	62	0	4.25	12	B.7
7	28	2.5 (11.2)	12	0	54.25	12	B.8
8	270	2.5 (108)	12	0	54.25	12	B.9 / B.10
9	270	10 (27)	12	0	54.25	12	B.11 / B.12
10	28 + $4V_{pk-pk}$ 15kHz	2.5 (11.2)	12	0	4.25	12	B.13
11	270 + $16V_{pk-pk}$ 15kHz	2.5 (108)	12	0	4.25	12	B.14

Table 3.2: Summary of Loose Terminal Series Arc Fault Test Scenarios

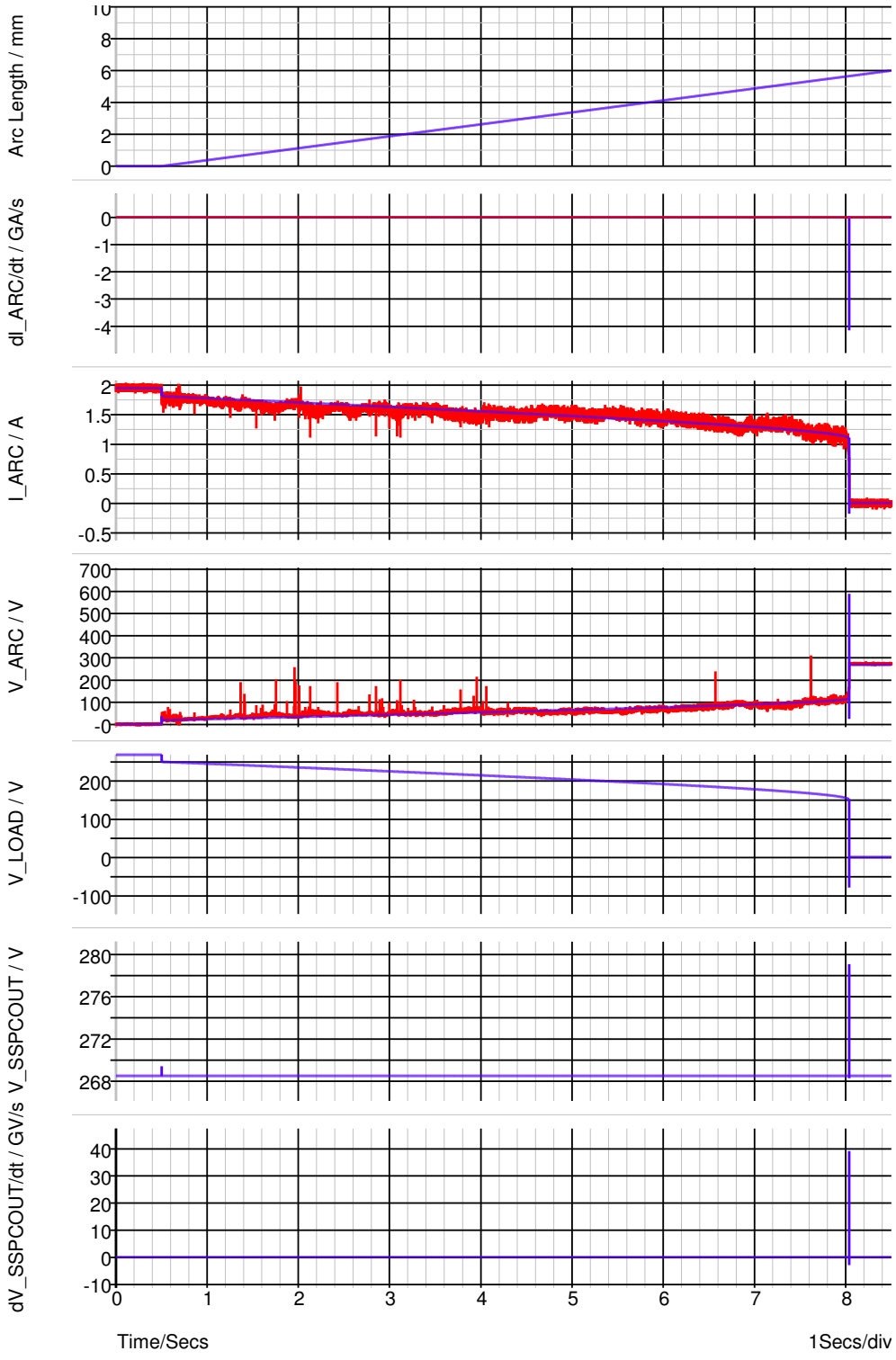


Figure 3.19: Scenario 1 - Comparison of Simulation and Experimental Results of a Drawn Arc Series Arc Fault Showing Arc Strike, Burn and Extinction - 270VDC Line, 2A Resistive Load (Blue - Simulated, Red - Experimental)

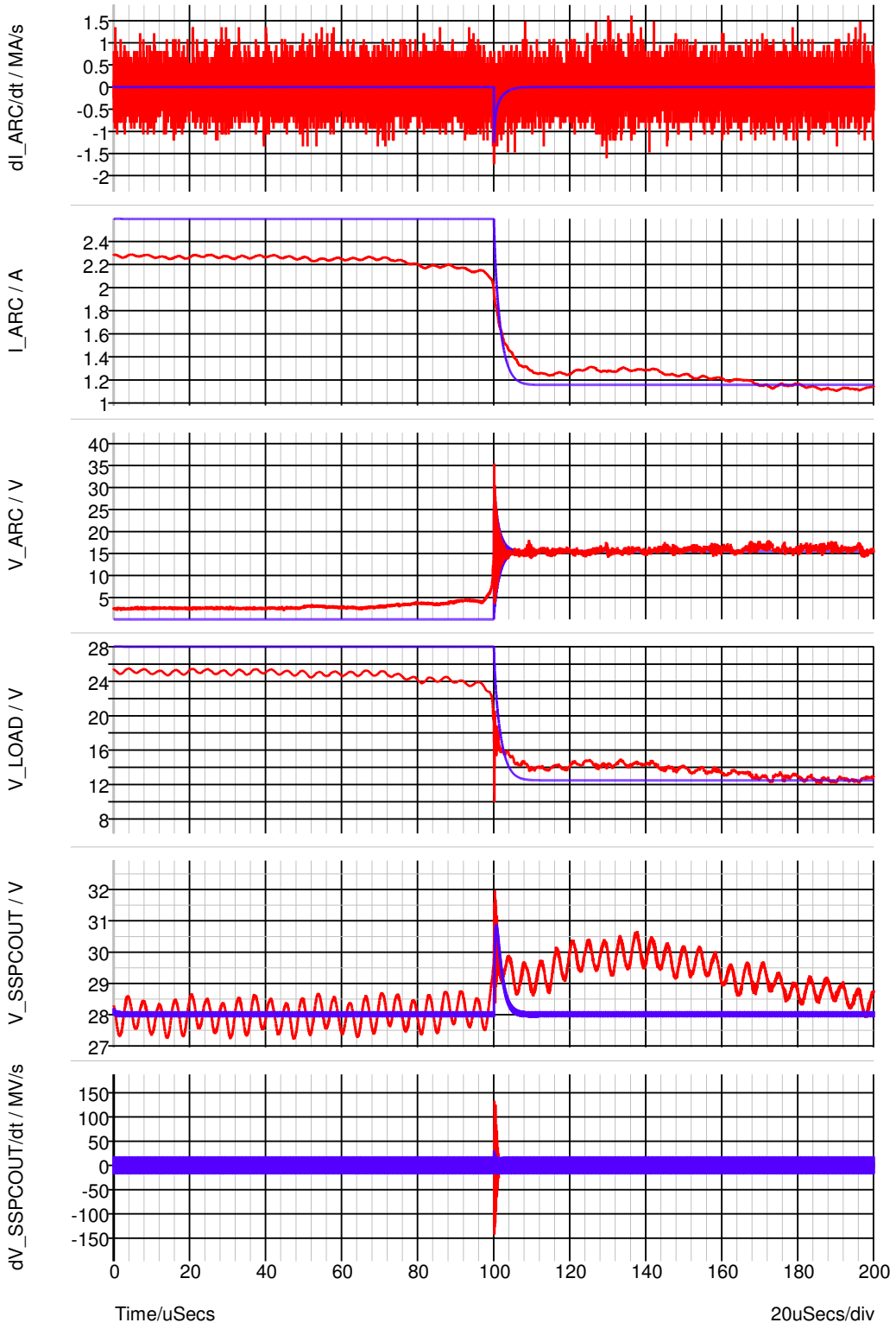


Figure 3.20: Scenario 2 - Comparison of Simulation and Experimental Results for Series Arc Fault - 28VDC Line, 2.5A Resistive Load (Blue - Simulated, Red - Experimental)

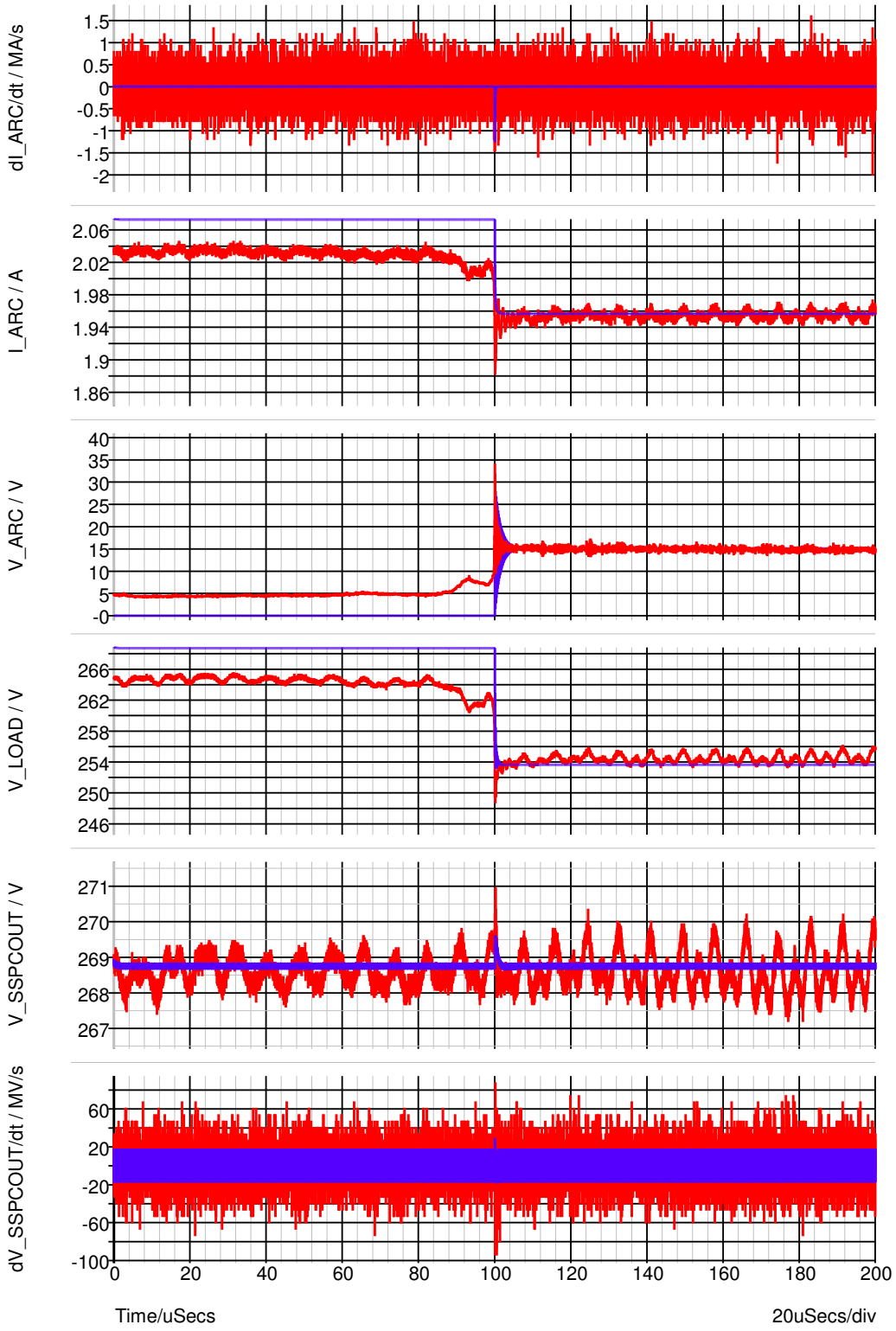


Figure 3.21: Scenario 3 - Comparison of Simulation and Experimental Results for Series Arc Fault - 270VDC Line, 2.1A Resistive Load (Blue - Simulated, Red - Experimental)

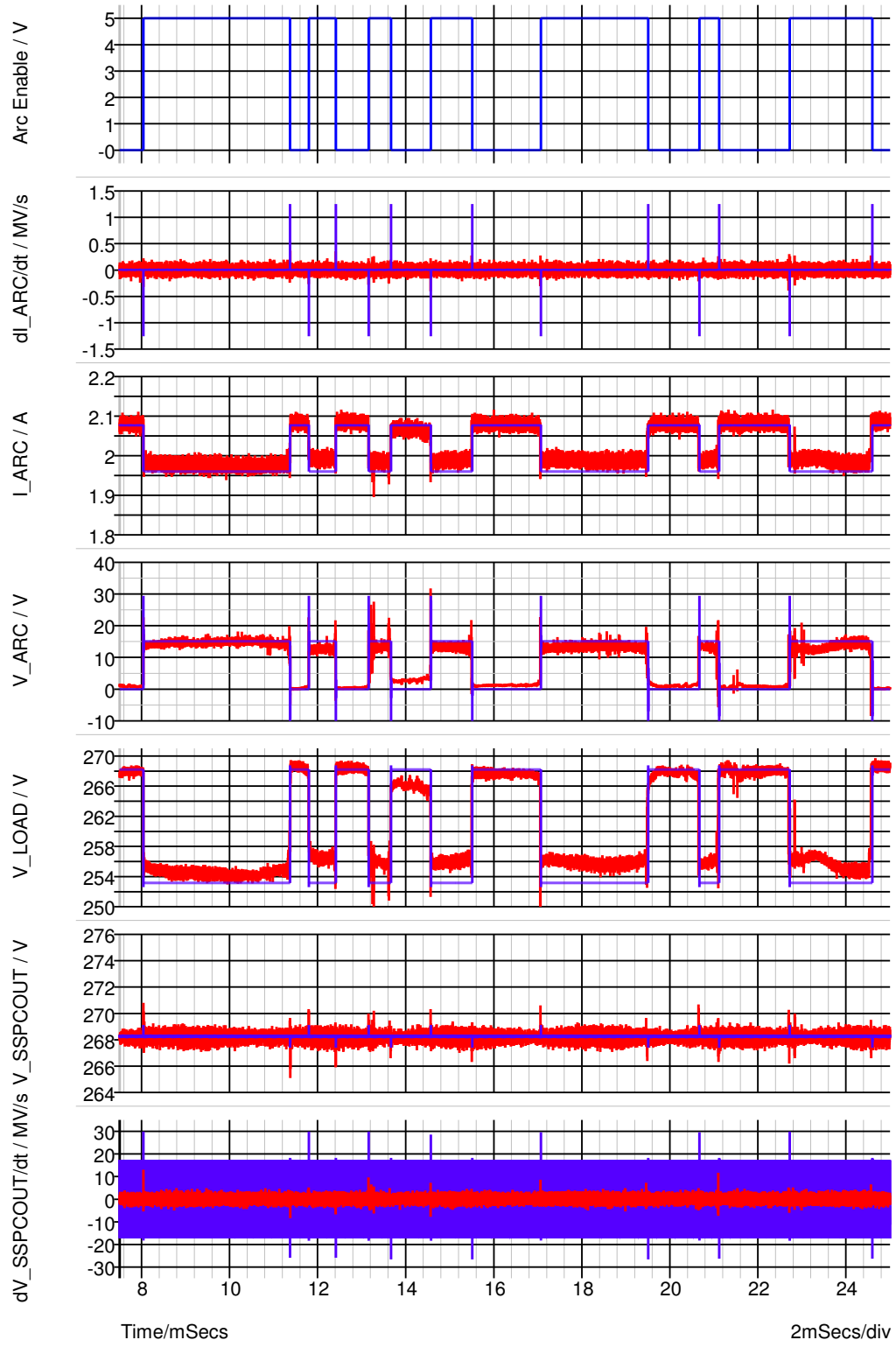


Figure 3.22: Scenario 3 - Comparison of Simulation and Experimental Results of Series Arc Fault Showing Effects of Loose Terminal - 270VDC Line, 2.1A Resistive Load (Blue - Simulated, Red - Experimental)

3.6 Discussion

3.6.1 Simulation of Drawn Arc Series Arc Fault Behaviour

Observing the basic drawn arc experiment outlined in Section 3.3 provided a great baseline for arc model parameter estimation. The integrated SSPC series arc fault model was configured with source voltage V_{src}, upstream L_{up}, downstream L_{dn} and load inductance L_{load} and load resistance R_{load} in accordance with Table 3.1. The arc strike voltage can be determined by observation of the experimental data given in Figure 3.19 and therefore model parameter A could be set to $A = 15V$. The voltage gradient B with respect to arc length ℓ was determined by observation of the gradient of arc voltage V_{arc} from the experimental data and was set to $B = 12715V/m$. Experimental data was exported from MATLAB® as a SPICE piece wise linear (PWL) source such that simulation results and experimental data could be easily compared. Finally parameter D was assumed to be zero for model simplification purposes since the arc lengths ℓ used here are small, and after selection of parameters A and B the selection of parameter C was trivial and successive approximations were made until the arc quench current from the simulation matched that of the experimental data where the final value was $C = 50$.

Comparing the final simulation result with the experimental data presented in Figure 3.19 it can be observed how arc voltage V_{arc} increases with arc length ℓ, and similarly how arc current I_{arc} reduces with arc length ℓ in the presence of a resistive load R_{load}. The extracted arc parameters produce simulation results which correlate with the experimental results. The major difference between the experimental and simulated results is that high frequency noise is present on the arc voltage V_{arc} experimental data due to instability of the arc caused by the ever increasing arc length ℓ, where the cathode and anode spots move to find the path of least resistance between the arc electrodes. The noise also appears on the arc current I_{arc} signal due to the arc voltage acting on the load resistance resulting in a current deviation dictated by Ohm's law.

Both the simulation results and experimental results illustrate why drawn series arcs are difficult to detect from the arc current I_{arc} signal because other than high frequency noise during arc burn, only the fast falling edge during arc strike and quench are indicative that a series arc is present. High frequency noise can be used for arc fault detection but it was shown in the literature review that the noise characteristics vary significantly between arcs in different circuit configurations. Furthermore high frequency noise behaviour is not modelled in this chapter because the effect of high frequency noise on the SSPC and load is negligible. Finally the experimental and simulation results show that during arc quench, the values of $\frac{dI_{arc}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ far exceed those encountered during arc strike, and this makes arc quench easier to detect. However, in 270VDC systems series arc faults rarely quench.

3.6.2 Simulation of Loose Terminal Series Arc Fault Behaviour

Following estimation of the arc model parameters A, B, C, D and n for the drawn arc scenario detailed in Section 3.6.1, these parameters were used as an approximation of the arc model parameters in the loose terminal scenario detailed in Section 3.4.9 since the arc electrode materials and arc lengths are similar. The proposed integrated loose terminal series arc fault and SSPC model illustrated in Figure 3.18 was then validated by configuring the model in accordance with a selection of experimental test cases detailed in Table 3.2. These test cases were also executed experimentally as part of the arc fault characterisation activity outlined in Appendix A, thus allowing a comparison of experimental and simulation results to be made.

The results of scenarios 2 through 9 are illustrated in Figures 3.20 through B.12 where arc length ℓ is assumed to be constant at ℓ =1mm after arc strike. The results show that the arc strike events are simulated well by the developed model during and following arc strike, however, the experimental data shows that the increase in current density between the loose arc electrodes prior to the arc strike introduces series resistance between the arc electrodes, thus causing a voltage drop in the range $2.5 \leq V_{arc} \leq 5V$, which can be seen by the arc voltage monitor V_{arc}. The top level SPICE arc models illustrated in Figures 3.8 and 3.9 could be modified to include this behaviour by introducing a variable resistor in series with the S_d switch within the arc model itself. To implement this solution more detail would be required regarding the electrical and mechanical behaviour of the loose terminal. This is an important consideration because if the voltage across the arc electrodes is already at a level of $V_{arc} \approx$ 5V prior to arc strike then the instantaneous voltage step at arc strike is now reduced, thus minimising the effect of the series arc fault on the circuit under observation. In scenario 4 where a 100μF load is connected to a 28VDC distribution circuit, the arc voltage behaviour in the simulation differs from the experimental data since an arc reconnection occurs immediately after arc quench as a result of mechanical interactions, and thus further knowledge of the mechanical system dynamics would be required to model this behaviour.

A general observation from the experimental characterisation activity in Appendix A was that arc voltage V_{arc} exhibits an exponentially decaying high frequency resonance in the order of ∼6MHz during arc strike, where the arc voltage transitions to 30V before settling down to a nominal steady state voltage of 15V. It was hypothesised that this resonance was generated by the interaction of the arc voltage step with the RLC isolated differential voltage probe characteristics modelled in the loose terminal system model in Figure 3.18 from Section 3.4.9. The resonant frequency was dependent on the probe capacitance and the probe lead inductance, therefore with a fixed probe capacitance longer probe leads gave a lower resonant frequency, and furthermore the exponential decay characteristic of the resonance was highly dependent on

the probe load resistance. The interaction of the isolated differential voltage probe and the series arc near current zero is of particular interest since the rate of change of arc voltage is limited by the probe, and therefore the true behaviour of the arc voltage in a series arc without a probe installed is hard to predict. The parasitic probe resistance, capacitance and inductance were therefore incorporated into the loose terminal system model in Figure 3.18 to allow a direct comparison between experimental and simulated data, and the results show that the simulated arc voltage resonance correlates well with the experimental data. The differential voltage probes also affect the load voltage V_{load} and SSPC output voltage $V_{sspcout}$ measurements, but the influence of these probes is less significant since the probe impedance is typically higher than the impedance presented by the test circuit.

The results of scenarios 2 through 9 illustrated in Figures 3.20 through B.12 show that the arc current I_{arc} is also simulated accurately during and after arc strike. Prior to arc strike the resistance introduced by the poor electrical contact at the loose terminal causes a voltage drop across the arc electrodes, which results in a reduction in load voltage, and this in turn leads to a reduction in arc current. This phenomena is similar to that of the glowing connection discussed in Section 2.3.4 of the literature review. Following arc strike the experimental arc current reduces to a level which matches the simulation results. Since the voltage across the arc electrodes is already 5V prior to arc strike and the steady state arc voltage after arc strike is 15V, the step in arc current is less than the predicted level if a 15V arc voltage step was assumed. This effect clearly makes arc strike events more difficult to detect and the ratio of measured arc current reduction $\Delta I_{arc(with\,drop)}$ to predicted arc current reduction $\Delta I_{arc(no\,drop)}$ can be calculated in accordance with Equation (3.27), which shows that for a typical pre-arc voltage drop of 5V the measured arc current is only two thirds of the simulated arc current, thus providing a significant detection challenge.

$$\frac{\Delta I_{arc(with\,drop)}}{\Delta I_{arc(no\,drop)}} = \frac{V_{arc} - 5}{V_{arc}} = \frac{15 - 5}{15} = \frac{2}{3} \tag{3.27}$$

The simulated rates of change of arc current with respect to time $\frac{dI_{arc}}{dt}$ for scenarios 2 through 9 are reasonably accurate in terms of order of magnitude, however, the noise levels present in the experimental arc current recordings, such as those presented in Figure B.8 for scenario 7, make it impossible to extract the real arc signal from the noise with any degree of confidence. This aspect of the simulation is therefore inconclusive due to the high levels of noise present in the experimental data, which limits the validation of this aspect of the simulation. In order to further validate the experimental data $\frac{dI_{arc}}{dt}$ would need to be computed over a longer time period to reduce the effects of high frequency noise, where this could be achieved by using MATLAB® to implement the technique for arc feature extraction presented in Section A.3.3.

The experimental SSPC output voltage $V_{sspcout}$ differs from the simulated output voltage, firstly because the power supply used for experimentation features a small AC ripple voltage which is inversely proportional to load current, and this ripple could easily be modelled and simulated. During each test scenario the experimental SSPC output voltage $V_{sspcout}$ also features a low frequency positive pulse immediately following arc strike, and this is believed to be due to the effect of sub-optimal regulation in the lab power supply following a reduction in arc current, since the power supply unit is capable of providing current far in excess of that used for this experiment, and therefore regulation at lower test currents is poor. These low frequency pulses lead to an increase of both the arc current and load voltage following arc strike, since the load voltage tracks the SSPC output voltage, and with a resistive load the arc current tracks the corresponding load voltage increase. Since the ripple and regulation behaviour is specific to the lab power supply and is not representative of an aircraft generator, this result is of no consequence to the development of a series arc fault detector, and thus the behaviour has not been added to the series arc fault system model.

The simulated rates of change of SSPC output voltage with respect to time $\frac{dV_{sspcout}}{dt}$ are in the same order of magnitude as the experimental data, although taking scenario 3 represented in Figure 3.21 as an example, the deviation in SSPC output voltage is 2V during arc strike in a range of approximately 270V, and therefore noise will affect $\frac{dV_{sspcout}}{dt}$ measurements.

For completeness a simulation of low frequency loose terminal behaviour is carried out as part of scenario 3 and is presented in Figure 3.22. As with the arc strike simulations, the arc voltage V_{arc} is accurately modelled, although due to the interaction of the probe impedance with the arc during contact reconnection, for example at time 13.6s, prior to reconnection there is a positive increase in arc voltage before arc voltage reduces to 0V. Arc current I_{arc} is modelled accurately and both arc voltage and arc current match the arc enable profile extracted from the experimental data by the MATLAB® feature extraction script.

Load voltage V_{load}, illustrated in scenario 3 and presented in Figure 3.22, is also modelled accurately along with SSPC output voltage $V_{sspcout}$, where the true significance of the voltage ripple from the supply voltage can be observed. Load voltage is not constant throughout a given arc due to variations in the arc length ℓ which are not modelled. Rates of change of both SSPC output voltage and arc current with respect to time are again in the same order of magnitude and are of the correct polarity, although high levels of noise levels are present in the experimental data.

3.6.3 Effect of the SSPC on the Series Arc Fault Electrical Behaviour

The series arc fault system model developed in this chapter allowed effects of the series arc fault on the SSPC and aircraft system to be analysed. These effects can be broken down against each functional block within the series arc fault system model given in Figure 3.18 thus.

Line Power / Upstream Cable Inductance
A higher source voltage V1 leads to a less detectable series arc since the effect of the reduction in load voltage by the 15V arc voltage is small with respect to the nominal load voltage. In contrast, the greater the upstream wiring inductance L_{up} to total system loop inductance L_{total} ratio, the more detectable a series arc fault is since this increased the magnitude of the voltage spike present at the SSPC output voltage as a result of an arc strike or quench event.

Section 18 of the environmental standard RTCA DO-160G specifies audio frequency conducted susceptibility sinusoidal ripple at a frequency of 1kHz through 15kHz at a level of $16V_{pk-pk}$ for a 270VDC aircraft bus, and $4V_{pk-pk}$ for a 28VDC aircraft bus [49]. The integrated SSPC SPICE model is valid for audio frequencies but is not valid for interfering RF signals since not all of the parasitic capacitances and distributed impedances have been considered in the integrated SSPC SPICE model. The results for scenarios 10 and 11, presented in Figures B.13 and B.14 respectively, illustrate the effect of a 15kHz sinusoidal ripple voltage source V5 of magnitude $4V_{pk-pk}$ for the 28VDC system, and $16V_{pk-pk}$ for the 270VDC system, in series with the main line voltage source V1. Note that experimental data was not available for scenarios 10 and 11 since these experiments were not part of the scope of Appendix A and an EPV tester was not available for lab testing at the time of writing.

The simulated induced ripple voltage caused a reduction in arc current in the 28VDC system, which in turn caused the series arc to quench 10μs after arc strike, whereas it has been demonstrated in a 28VDC system with a stable source voltage that arcs continue to burn indefinitely. Conversely in the 270VDC system the induced ripple voltage did not quench the arc since the influence on arc current was minimal.

The author was concerned that the induced ripple voltage and corresponding ripple current would prevent the identification of arc strike and arc quench events from the rate of change of arc current with respect to time $\frac{dI_{arc}}{dt}$ and rate of change of SSPC output voltage with respect to time $\frac{dV_{sspcout}}{dt}$ signals, thus preventing $\frac{dI_{arc}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ from being used for series arc fault detection. It was found that the induced ripple voltage did not have a significant effect on the rate of change of arc current with respect to time $\frac{dI_{arc}}{dt}$. The rate of change of SSPC output voltage with

respect to time $\frac{dV_{sspcout}}{dt}$ also did not show a significant signal in response to the ripple, and the arc strike was still clearly an order of magnitude above the ripple signal. The ripple seen in the 270VDC system therefore had little effect on both the behaviour and detectability of the series arc fault.

Input/Output Snubber

Observing both the experimental and simulation results for scenario 3 in Figure 3.22, during arc strike and arc quench corresponding exponentially decaying positive voltage spikes appear on the SSPC output voltage $V_{sspcout}$. Given that the SSPC switch S1 is closed during normal load operation, both the input and output snubbers comprised of R3+C3 and R4+C4 respectively are configured in parallel. These snubbers limit the rise in SSPC output voltage during arc strike and arc quench as current flows through R3 and R4 to charge capacitors C3 and C4 respectively. This is the inherent functional purpose of the snubber components, however, during an arc fault these snubber components limit the voltage spike seen at the SSPC output voltage, which is not ideal for passive electrical series arc fault detection purposes. The repetitive nature of series arcing could conceptually overheat the snubber resistors under high upstream inductance scenarios.

The results for scenarios 8 and 9, presented in Figures B.10 and B.12 respectively, show the effect of series arc faults at current levels of 2.5A and 10A respectively. It is demonstrated here that the SSPC output voltage $V_{sspcout}$ pulse for the simulations without snubbers (indicated in magenta) is far greater than the simulations with snubbers (indicated in cyan) since the snubber resistors R3 and R4 absorb the energy in this pulse. For scenario 8 at 2.5A the peak power in each snubber resistor R3 and R4 is 50mW and the total energy dissipated in each resistor over the pulse duration is 139nJ, and for scenario 9 at 10A the peak power in each snubber resistor is 550mW and the energy dissipated in each resistor over the pulse duration is 1.69μJ. Assuming a realistic worst case arc repetition rate of 100k arcs per second, multiplying the snubber energy per arc 1.69μJ by the arc repetition rate gives an average snubber resistor power dissipation of 0.169W. This figure is manageable with surface mount resistor technology, however, as SSPC current levels rise this number will increase and further simulations should be carried out to ensure that a series arc fault downstream from a given SSPC will not cause overheating or failure of the snubber components.

Transient Suppression

When the SSPC switch is closed the transient suppressor MOV1 presents a small parasitic capacitance across the snubber networks R3+C3 and R4+C4 in the order of tens of picofarads. Since the combined snubber network capacitances are four orders of magnitude greater than this parasitic capacitance, the snubber network dominates the SSPC output voltage transient response. If a given series arc quenches then MOV1 prevents an overvoltage across the SSPC switch S1 input.

Downstream Cable Inductance

The greater the downstream wiring inductance to total system loop inductance L_{total} ratio, the less detectable a series arc fault is since this decreased the magnitude of the voltage spike present at the SSPC output voltage as a result of an arc strike or quench event.

Leakage Current Management

The series arc fault has a minimal effect on the leakage current management component R6 and similarly the leakage management resistor has negligible impact on series arc fault behaviour, therefore this component could be neglected from future simulations for computational simplification purposes. A more detailed study of the interaction between SSPC leakage and series arc faults is carried out in Section 5.3 of this thesis.

Main SSPC Switch / Anti-parallel Diode

Since the main SSPC switch S1 is closed during normal load operation this has little effect on the series arc fault behaviour. Similarly the anti-parallel diode D1 has little effect when the SSPC is closed since no current flows through it.

Flywheel Diode

The flywheel diode D2 is not important when the SSPC main switch S1 is closed since the main current flow is through S1, however the flywheel diode component becomes more important when considering interruption of a series arc, and more detail can be found regarding deliberate interruption of series arcs in Chapter 5 of this thesis. In similarity with the transient voltage suppressor MOV1 the flywheel diode presents a small parasitic capacitance to the SSPC output, however, this capacitance is again four orders of magnitude less than those in the parallel snubber networks.

Electrical Load

Finally the effect of series arcing on the electrical load R_{load}, C_{load} and L_{load} is detailed in the experimental characterisation carried out in Appendix A.

3.6.4 Interaction of the Electrical and Mechanical Domains

During the capture of experimental data it was noted that the electrical configuration of the system affects the mechanical behaviour of the system. The most prominent example of this is that of the loose terminal scenario where the duration and period of arcs is based heavily on the mass-spring system which is the aircraft wiring harness and associated connectors and bracing, and the sinusoidal or random vibration profile to which it is subjected. It is also dependent upon the magnitude of current flowing through the cable under test since this increases current density during the arc / reconnect cycle. The increased current density results in the formation of a “spot

weld" during the reconnect cycle which changes the distribution of the arc period and arc durations under the loose terminal scenario.

To accurately model the interaction between electrical and mechanical systems would involve a huge multivariate analysis which was out of scope for this project. The author chose to use a simple model since the electrical power distribution system designer would never have sufficient project time to model every possible series arc fault position on a new aircraft platform. In addition to this, the use of random vibration drives a statistical approach to analysis of "loose terminals", since the behaviour is unlikely to be consistent between consecutive test runs.

3.7 Chapter Summary

The aim of this chapter was to model and simulate the behaviour of a series arc fault within a DC aircraft electrical distribution system. To achieve this a SPICE arc fault system model was developed including a parametric, configurable arc model for simulation of series and/or parallel arc faults within existing SSPC models. Both the Ayrton, Steinmetz and Nottingham static V-I models, and the Cassie and Mayr energy conservation models were considered for series arc fault modelling. Static V-I models proved easier to implement in the SPICE environment and more accurately modelled arc quench behaviour. A modified Nottingham model was created to realise a bidirectional arc model which addressed the issue of the asymptote in the V-I characteristics near arc current zero. A simple series arc fault model interface containing the modified Nottingham equation with configurable parameters A, B, C, D and n was developed with two arc terminals, a variable arc length ℓ input and a variable arc enable input. The modified Nottingham equation was implemented as a non-linear continuous transfer function in the SPICE environment. A curve tracer utility was developed to plot the static V-I arc characteristics and to validate the model behaviour with a given set of parameters, .

A drawn arc simulator was designed and implemented to allow study of the series arc behaviour in a controlled environment where the sample data was used to extract example parameters for the modified Nottingham model thus providing a starting point for the parameters used in the integrated SPICE SSPC system model.

The second element to fulfilling a loose terminal series arc fault model was the modelling of the chaotic contact behaviour, and to achieve this a MATLAB® script implementing a Finite State Machine (FSM) was used to extract the arc strike, arc quench and arc reconnection timing data from the experimental loose terminal series arc fault waveforms captured during the characterisation activity in Appendix A. The extracted data was then used successfully to drive arc fault enable signal in the integrated SSPC SPICE system model.

A simple transmission line model was developed based on a wire-over-ground plane scenario, common to 270VDC distribution in aircraft electrical power distribution applications, in order to estimate the upstream and downstream cable impedances for the proposed SSPC SPICE system model. The dimensions of a Boeing 747 were used to estimate typical cable lengths. The developed series arc fault model and simple transmission line models were integrated into a simple SPICE SSPC system model thus allowing series arc simulation to be carried out in a representative system.

SPICE simulations were completed addressing arc strike and arc burn for a range of resistive, capacitive and inductive loads. The simulated arc voltage V_{arc}, arc current I_{arc}, load voltage V_{load}, rate of change of arc current with respect to time $\frac{dI_{arc}}{dt}$ and rate of change of SSPC output voltage with respect to time $\frac{dV_{sspcout}}{dt}$ results were compared to experimental data and the were found to be well correlated when using the arc parameters extracted during the drawn arc study.

An additional feature was identified in the experimental arc voltage V_{arc} waveform, where prior to arc strike in the "loose terminal" scenario, the arc voltage was typically in the range $2.5 \leq V_{arc} \leq 5V$. It is proposed that this was due to the formation of a point contact between ring tag and bolt at the instant prior to arc strike, which led to an increase in current density, and thus a high voltage drop. The fast voltage step seen during arc strike is therefore lower than the predicted 15V, and the available signal level for arc fault detection is reduced.

The simulation verified the experimental data and demonstrated that the isolated differential voltage probe used to measure arc voltage influenced the arc voltage signal especially during arc strike and arc quench due to the parasitic probe lead inductance and probe capacitance / resistance. Although measuring arc voltage was useful for determining where an arc strikes and quenches, the presence of the differential probe affected the behaviour of the arc itself and could therefore invalidate a proposed arc fault detection system if the influence of any given probe is not considered. It was concluded that during the experimental verification of a proposed passive electrical series arc fault detection system using a loose contact configuration, the arc voltage should not be monitored since this will invalidate the test results.

The proposed technique for feature extraction of arc periods and arc durations from experimental loose terminal data in scenario 3 allowed the simulation of a series arc fault on a macroscopic scale.

It was demonstrated by analysis that the SSPC transient suppression, leakage current management, flywheel diode, main switch and anti-parallel diode components both have negligible impact on series arc fault behaviour, and similarly are not influenced significantly by the presence of series arc faults.

The simulation demonstrated that during arc strike a positive voltage peak appears on the SSPC output voltage, and this provides a method of detecting arc faults. Increasing the upstream inductance to total loop inductance ratio was found to increase the magnitude of this peak, and increasing the downstream wiring inductance to total loop inductance ratio was found to decrease the magnitude of this peak. It was demonstrated that the presence of the input/output snubber networks greatly reduced both the magnitude of the peak in SSPC output voltage and the rate of change of SSPC output voltage with respect to time during arc strike, thus making a given series arc fault more difficult to detect. The shape of the arc current waveform was also effected by the presence of the input/output snubber networks, however, the effect of this on the peak rate of change of arc current with respect to time was negligible. In conclusion the SSPC designer must consider the effect of input/output snubber networks on arc fault detection performance.

The simulation results for series arc faults with 28VDC and 270VDC supply voltages and load current levels of 2.5A and 10A were modelled with equal levels of accuracy and therefore the integrated SSPC arc fault model is versatile.

The effect of audio frequency ripple at the highest frequency of 15kHz specified by RTCA DO-160G Section 18 was investigated at a level of $4V_{pk-pk}$ for 28VDC simulations and $16V_{pk-pk}$ for 270VDC simulations [49]. It was determined that the presence of high levels of ripple in 28VDC systems can cause series arc faults to quench, where in the absence of ripple they would be stable. In contrast it was demonstrated that the presence of high levels of ripple in 270VDC systems has little impact on the stability and detectability of series arc faults.

Chapter 4

Development and Evaluation of a Voltage Invariant Series Arc Fault Detection System for Aerospace SSPCs

4.1 Introduction

4.1.1 Background

The literature review covering passive electrical series arc fault detection methods in Section 2.4.4 highlighted that passive electrical methods based on analysis of load current waveforms have been successful in detecting series arc faults in 28VDC and 115VAC aircraft electrical power distribution systems. The work of Brooks, Faifer and Zuercher further highlighted that detecting step changes in loop current provides a clear indication that a series arc has struck in the circuit under test based on an analysis of fundamental arc physics, although these step changes could be caused during the normal operation of some types of load [103; 106; 113; 121]. The characterisation work carried out in Appendix A further demonstrated that the step change in current experienced during arc strike in a 270VDC system is ∼5.6% compared with ∼54% in a 28VDC system thus providing a tough challenge to detect arc strike in a noisy 270VDC system with a relatively low current sensor dynamic range. Furthermore the modelling work discussed in Chapter 3 allowed the series arc fault electrical system behaviour to be understood for the different corner cases, which in turn enabled the top level requirements for the series arc fault detection system to be extracted.

The purpose of this chapter is therefore to explore the limits of passive electrical series arc fault detection based on detection of step changes in current due to arc strike, and to evaluate the performance of the proposed series arc fault detection

system. Demonstrating a baseline 270VDC passive electrical series arc fault detection system provides a reference against which more sophisticated detection methods can be compared.

4.1.2 Hypothesis

This chapter is underpinned by the hypothesis that series arc faults in a representative aircraft electrical power system can be detected by processing electrical data such as the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$.

4.1.3 Aims and Objectives

The main aim of this chapter is to develop and evaluate a voltage invariant series arc fault detection system for operation in aerospace SSPCs with source voltages of both 28VDC and 270VDC.

The main objectives are to firstly to identify and summarise the system, hardware and software requirements for the voltage invariant series arc fault detection system, based on the series arc fault characterisation and modelling activities carried out in Appendix A and Chapter 3 respectively. The second and third objectives are then to design and evaluate both series arc fault current and voltage monitors respectively. The fourth objective is to integrate the proposed series arc fault current and voltage monitor hardware with the Primary Electrical Power Distribution Centre (PEPDC) and Primary Electrical Power Solid state power Controller (PEPSC) SSPC modules. The fifth objective is to develop a software series arc fault confirmation algorithm. The final objective of the chapter is to gather practical test data to evaluate and analyse the performance of the overall series arc fault detection system.

4.2 Top Level System Requirements for the Voltage Invariant Arc Fault Detection System

Top level system requirements are needed in order to provide criteria against which to judge any candidate arc fault detection system, and based on the review of literature in Chapter 2 these requirements can be summarised thus, where **[01]** indicates a requirement, **[01g]** indicates a goal, and **[01_i]** indicates an information statement.

4.2.1 Detection Capability / Nuisance Trips

[01] The series arc fault detection system **shall** be capable of detecting series arc faults on the switched outputs of 120A SSPC modules where the attached aircraft load currents are in the range 5A through 120A.

[01_i] When considering a passive series arc fault detection system based on current and voltage measurement this requirement drives an upper and lower bound for the current measuring system, and determines also the required measurement resolution. The rated current of the PEPDC and PEPSC SSPC modules is 120A and therefore this sets the upper bound. The lower bound is a challenging target where 5A rated SSPC modules are common in secondary aircraft electrical power distribution systems.

[02] The series arc fault detection system **shall** be capable of detecting series arc faults on the switched outputs of 120A SSPC modules where the attached load features parallel load capacitances in the range 0 through 380μF and series load inductances in the range 0 through 100μH.

[02_i] Typical aircraft loads feature EMC filters, hold-up capacitors and other reactive elements which affect the detectability of series arc faults, and therefore detection performance needs to be characterised with different permutations of these load scenarios.

[03] The series arc fault detection system **shall** be capable of detecting series arc faults where the minimum SSPC upstream wiring inductance to total loop inductance ratio is $\geq$10%.

[03_i] The upstream to loop inductance ratio defines the magnitude of the voltage peak at the SSPC output during arc strike. The upstream to total loop inductance ratio therefore bounds the requirements on voltage monitor hardware. This scenario occurs when the power distribution panel is mounted close to the power source.

[04] The series arc fault detection system **shall** be capable of detecting series arc faults in systems with 270VDC and 28VDC nominal system voltages.

[04_i] It was demonstrated in Appendix A that higher system voltages reduce the percentage reduction in current during an arc fault and therefore this requirement further drives the required current measurement resolution.

[05] The series arc fault detection system **shall** be configurable such that it will either give indication of the presence of a series arc fault, or will trip the SSPC upstream from the series arc fault.

[05_i] This requirement is simple and convenient to implement in software and allows an indication of a fault to be given to the pilot during a series arc fault detection event, rather than directly tripping the given SSPC.

[06] The series arc fault detection system **shall** not be asserted by the effects of arc faults or other fault conditions on adjacent SSPC outputs.

[06_i] Crosstalk between wires can be an issue where many output wires are run in a tight bundle therefore a given series arc fault detection system needs to be sensitive enough to detect a series arc fault downstream from the SSPC to which it is fitted but specific enough not to detect crosstalk from adjacent SSPC outputs.

[07] The series arc fault solution **shall** be applied to each switched output of an electrical power distribution system.

[07_i] This requirement drives weight, volume and complexity for a given electrical power distribution system and therefore care must be taken to simplify any proposed series arc fault detection system. This is why a passive rather than a complex active series arc fault detection system is preferred.

4.2.2 Cost / Reuse

[08g] The series arc fault detection system **should** reuse the existing PEPDC SSPC current and voltage monitoring system to minimise cost of the full SSPC solution.

[08g_i] During the bid phase of the PEPDC project it was determined that arc fault detection is seen by customers as a "nice to have" option and in addition to this is seen by the author's business as a differentiating technology since competitors do not currently have robust series arc fault detection solutions. This drives the goal of minimising the cost of the series arc fault detection function, and attempting to reuse hardware from other SSPC functions in order to minimise the cost of the overall SSPC solution.

4.2.3 Weight / Volume

[09g] The series arc fault detection system **should** minimise the need for additional hardware which inflates unit weight and volume requirements.

[09g_i] Minimisation of weight and volume is critical for aerospace applications since this translates directly into fuel burn and thus aircraft running costs. Since the series arc fault detection solution is applied to each switched output of an electrical power distribution system this multiplies the weight and volume of a given series arc fault detection solution, and in similarity with the cost goal, the need for any additional hardware to realise the series arc fault detection function makes this goal prominent. In a live aerospace project a numerical weight / volume target would be applied, however, for a research project the goal is purely to minimise weight and volume.

4.2.4 Thermal / Power Dissipation / Voltage Drop

[10] The series arc fault detection system **shall** operate in an ambient temperature range of -40°C through +100°C.

[10_i] This requirement drives the need for high temperature capable electronics, and temperature related drift of current and voltage measurement systems also needs to be considered.

[11g] The series arc fault detection system **should** target <100mW power dissipation.

[11g_i] Power dissipation budget is <100mW for the PEPDC and PEPSC applications.

4.2.5 EMC / EPV

[12g] The series arc fault detection hardware **should** operate in accordance with the test requirements of RTCA DO-160G [49] Section 16 Category D 270VDC power input.

[12g_i] This goal will not be verified on the prototype hardware at this stage.

[13g] The series arc fault detection hardware **should** be designed to meet the Audio Frequency Conducted Susceptibility - Power Inputs conditions outlined in RTCA DO-160G [49], Section 18, for Category Z equipment.

[13g_i] This goal will not be verified on the prototype hardware at this stage. It was demonstrated in Chapter 3 that these signals have little impact on the detectability of 270VDC series arc faults.

[14g] The series arc fault detection hardware **should** be designed to meet the Induced Signal Susceptibility conditions outlined in RTCA DO-160G [49], Section 19 for Category CC equipment.

[14g_i] This goal will not be verified on the prototype hardware at this stage.

[15g] The series arc fault detection hardware **should** be designed to meet the Radio Frequency Susceptibility (Radiated and Conducted) conditions outlined in RTCA DO-160G [49], Section 20 for Category Y equipment.

[15g_i] This goal will not be verified on the prototype hardware at this stage. Since passive series arc fault detection systems may respond to the high frequency transients created by the electric arc, the presence of radiated and conducted Radio Frequency signals could cause nuisance trips at the SSPC.

[16g] The series arc fault detection hardware **should** be designed to meet the Emission of Radio Frequency Energy conditions outlined in RTCA DO-160G [49], Section 21 for Category L equipment.

[16g_i] This goal will not be verified on the prototype hardware at this stage. This goal ensures that the proposed series arc fault detection solution does not increase the level of Radio Frequency emissions over and above those emissions generated by the other SSPC functions.

[17g] The series arc fault detection hardware **should** be designed to meet the Lightning Induced Transient Susceptibility conditions outlined in RTCA DO-160G [49], Section 22 for Category B3D43 equipment.

[17g_i] This goal will not be verified on the prototype hardware at this stage. Lightning transients are a major consideration in aircraft electrical power distribution system design and great care is taken to manage these transients. Single-stroke lightning is less of a concern for passive series arc fault detection systems since a confirmation algorithm can be used to handle single transient events, however, the effects of multiple-stroke lightning must also be considered.

4.3 Series Arc Fault Current Sensor Development

4.3.1 Hardware Requirements for the Series AFD Current Sensor

There are five derived hardware requirements to consider for the series arc fault current sensor. Hardware requirements **[h01]**, hardware goals **[h01g]** and hardware information statements **[h01_i]** are provided thus.

4.3.1.1 Current Sensor Range, Sensitivity and Bandwidth

Parent Requirements: **[01]**, **[02]**, **[03]**, **[04]**, **[07]**, **[08g]**, **[09g]**

[h01] The series arc fault current sensor **shall** be sensitive enough to detect negative step changes in current of 260mA.

[h01_i] The minimum load current is $I_{load} = 5\text{A}$ and the maximum normal system voltage is 285VDC, the maximum state of a 270VDC bus according to RTCA DO-160G [49]. The reduction in current during this scenario can be calculated in accordance with Equation (4.1).

$$\Delta I_{loop} = \frac{V_{arc}}{V_{src}} I_{load} = \frac{15}{285} \times 5 = 260mA \tag{4.1}$$

[h02] The series arc fault current sensor **shall** be capable of detecting negative step changes in current up to 7.7A.

[h02_i] The maximum load current is $I_{load} = 120$A and the minimum system voltage is 235V, the minimum state of a 270VDC bus according to RTCA DO-160G [49]. The reduction in current during this scenario can be calculated in accordance with Equation (4.2).

$$\Delta I_{loop} = \frac{V_{arc}}{V_{src}} I_{load} = \frac{15}{235} \times 120 = 7.66A \tag{4.2}$$

[h03] The series arc fault current sensor **shall** have a bandwidth capable of detecting a minimum negative dI/dt magnitude of 0.3A/μs.

[h03_i] Based on the aircraft electrical transmission line model developed during the modelling activity in this thesis presented in Chapter 3 a maximum system inductance of $L_{total} = 50\mu$H can be assumed, based on a maximum combined cable length from generator-to-SSPC and SSPC-to-load of 50m. Assuming an arc voltage $V_{arc} = 15$V the minimum rate of change of loop current with respect to time can be calculated in accordance with Equation (4.3).

$$\frac{dI_{loop}}{dt} = \frac{V_{arc}}{L_{total}} = \frac{15}{50 \times 10^{-6}} = 0.3A/\mu s \tag{4.3}$$

4.3.1.2 SSPC Integration and High Voltage Isolation

Parent Requirements: **[04]**

[h04g] The series arc fault current sensor **should** be capable of providing an analogue signal in the range 0V through 3.3V to a microprocessor whose ground is referenced to the given SSPC output voltage.

[h04g_i] The microcontroller on both the PEPDC and PEPSC designs has a ground reference on the output of the SSPC in order to enable current monitoring and gate control for the MOSFETs used in the design. The microcontroller is powered from a 3.3VDC power supply which is also referenced to the SSPC output voltage. The SSPC output voltage can vary in the range -1VDC through 350VDC with respect to aircraft chassis.

[h05] The series arc fault current sensor **shall** be capable of providing electrical isolation for steady state voltages of at least +350VDC and transient voltages of at least +700VDC with respect to aircraft chassis.

[h05_i] This ensures that the SSPC output voltage referenced series arc fault current sensor hardware is suitably isolated from aircraft chassis for safety purposes.

4.3.2 Existing / Typical SSPC Current Sensor

To understand the requirement for a dedicated series arc fault current sensor it is first necessary to understand why a typical SSPC current monitoring system is not suitable for series arc fault detection in high voltage SSPCs. The PEPDC SSPC module current monitor circuit, illustrated in Figure 4.1, uses series sense resistors as this is a cost effective way of measuring the current flow through each semiconductor. Low value sense resistors are chosen to minimise heat losses and limit voltage drop for high current loads, and thus the PEPDC sense resistors have a value of $R_s = 3\text{m}\Omega$. The voltages developed across each sense resistor are amplified using an operational amplifier, and the current measurements from each semiconductor are averaged by an additional operational amplifier. The SSPC is a unidirectional switch, however, both positive currents up to 550% of the SSPC rating and negative currents down to -100% of the switch rating need to be monitored to allow measurement of positive fault currents and regenerative currents returned from the load. The current monitor therefore needs to monitor a range of 650% rated current which for the 120A rated PEPDC SSPC gives a full scale range of $I_{fs} = 780\text{A}$.

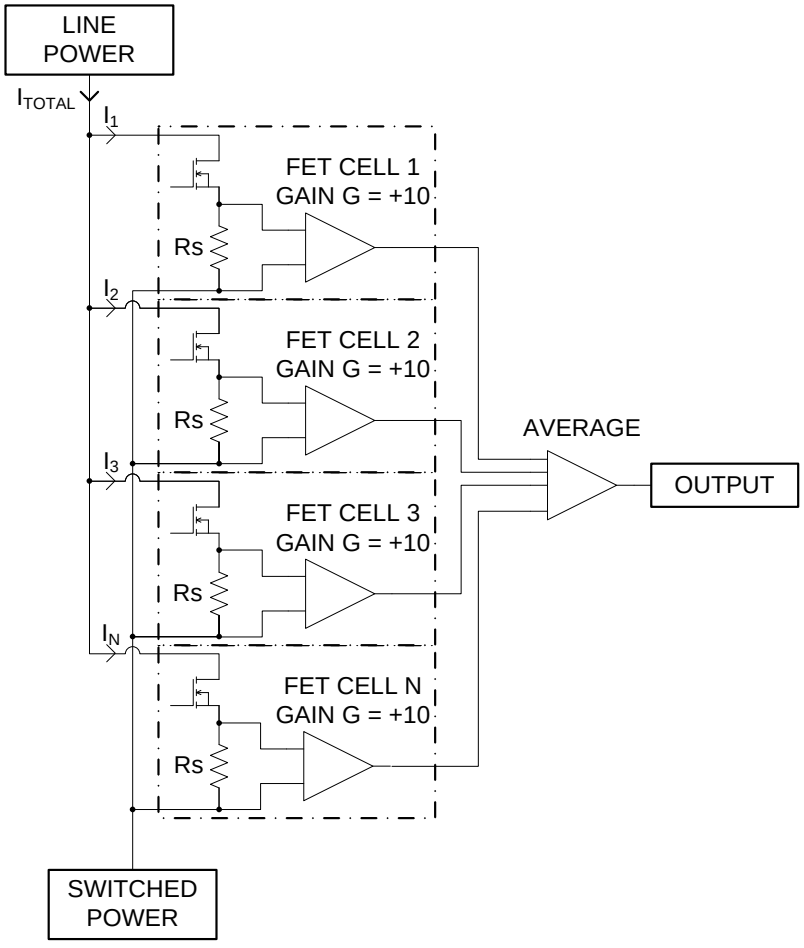


Figure 4.1: Typical SSPC Current Sensor

The voltage at the output of the current monitor circuit V_{output} reflects the average of each current flowing through each semiconductor device I_N for N MOSFET cells and is summarised by Equation (4.4).

$$V_{output} = \frac{\sum_{1}^{N} GI_N R_s}{N} \tag{4.4}$$

Assuming that current is shared evenly between all semiconductors in a given switch then the current monitor output voltage V_{output} can be simplified to Equation (4.5).

$$V_{output} = GI_N R_s \tag{4.5}$$

$$I_{sspc} = NI_N \tag{4.6}$$

Furthermore SSPC output current is given by Equation (4.6). Dividing Equation (4.5) by Equation (4.6) yields a transfer function in Equation (4.7) which relates current monitor output voltage V_{output} to overall SSPC output current I_{sspc}.

$$TF = \frac{V_{output}}{I_{sspc}} = \frac{GI_N R_s}{NI_N} = \frac{GR_s}{N} \tag{4.7}$$

A numerical transfer function can be then obtained given that the PEPDC SSPC has $N = 16$ semiconductors, each current sense amplifier has a gain of $G = 10$, the sense resistor value used is $R_s = 3\text{m}\Omega$ and the overall SSPC output current is $I_{SSPC} = 1\text{A}$.

$$TF = \frac{GR_s}{N} = \frac{10 \times (3 \times 10^{-3})}{16} = 1.875mV/A \tag{4.8}$$

Equation (4.8) shows that the current to voltage transfer function for the PEPDC SSPC current monitor is 1.875mV/A. This signal is fed into an Analogue to Digital Converter (ADC) where a microcontroller interprets the current monitor data. This circuit has been successfully verified over aerospace temperature ranges and is a simple robust solution for the SSPC current monitoring function.

From the series arc fault characterisation work in Appendix A, summarised in hardware requirement **[h01]**, it was determined that the minimum reduction in load current seen during an series arc fault in a 270VDC electrical power distribution system occurs when feeding the lowest resistive load current of 5A at the maximum normal bus voltage state of 285VDC. For a $5A$ nominal resistive load current, a deviation ΔI_{load} would be seen during an arc strike / quench event in accordance with Equation (4.9), which would yield a corresponding current monitor deviation of $\Delta V_{monitor}$ given in Equation (4.10).

$$\Delta I_{load} = I_{load}\frac{V_{arc}}{V_{src}} = 5 \times \frac{15}{285} = 263mA \tag{4.9}$$

$$\Delta V_{monitor} = 1.875 \times \Delta I_{load} = 1.875 \times 0.263 = 493\mu V \tag{4.10}$$

The required dynamic range DR for a current monitor capable of servicing both series arc fault detection requirements and SSPC functional requirements is given by Equations (4.11) and (4.12) respectively, where the full scale current range I_{fs} for the 120A rated PEPDC SSPC between -100% and 550% is 780A.

$$\text{DR} = \frac{I_{fs}}{\Delta I_{load}} = \frac{780}{263 \times 10^{-3}} = 2108 \tag{4.11}$$

$$\text{DR(dB)} = 20\log(\frac{I_{fs}}{\Delta I_{load}}) = 20\log(2108) = 66dB \tag{4.12}$$

The $V_{monitor}$ signal is further amplified by a voltage gain of 2 to fit the -100% to 550% current monitoring range to the $V_{adcref} = 3$V Analogue to Digital Converter (ADC) window, and thus the resulting signal of $V_{final} = 986\mu$V appears at the ADC input as a result of the worst case series arc fault scenario. Assuming to accurately measure the 986μV series arc fault signal that at least 10 Least Significant Bit (LSB) levels are required, then the required resolution B of the Analogue to Digital Converter (ADC) can be estimated by Equation (4.13).

$$B = \left\lceil \sqrt{\frac{10V_{adcref}}{V_{final}}} \right\rceil = \left\lceil \sqrt{\frac{10 \times 3}{986 \times 10^{-6}}} \right\rceil = 175 \tag{4.13}$$

A resolution of $B = 175$bits for this application is completely unrealistic given the estimated required sampling rate of $F_s = 100$kSPS based on the feature extraction activity carried out in Section A.3.3. Furthermore in an aerospace environment the signal level is too small when considering the various noise sources: Electrical Power Variation (EPV), Radiated and Conducted Susceptibility, thermal and amplifier noise sources. In conclusion the existing SSPC current monitor solution is not appropriate for dual-use as a series arc fault current sensor, and therefore a dedicated series arc fault current sensor is required.

4.3.3 Design of a Multi-Layer, Planar, PCB Current Transformer

During the development of the arc fault planar current transformer a new project PEPSC was started in parallel with PEPDC, which performs the same function as PEPDC but is implemented as a hybrid power module. As a result of the second project, a dual implementation of the arc fault planar current transformer is required which will fit into the PEPSC form factor. This section covers the design activity carried out for both projects beginning with the preliminary confidence testing stage.

4.3.3.1 Preliminary Confidence Testing

The major concerns for a multi-layer PCB air-core current transformer implementation were sensitivity and resonance. Without a high permeability core the transformer may suffer from high frequency resonance and/or low sensitivity. Resonance can be problematic if the unit under test is in the presence of a radiated RF field since

this may cause the arc fault detection system to become "blind" or cause nuisance trips. To gain confidence in the proposed planar current transformer approach before committing to an expensive PCB design, the Rogowski coil hardware de-risk rig in Figure 4.2 was created. This rig was designed to emulate the busbar structure from the PEPDC PCB hardware in order to enable representative Rogowski coil current transformer performance data to be captured. A full drawing of the de-risk rig can be found in Appendix C.3.

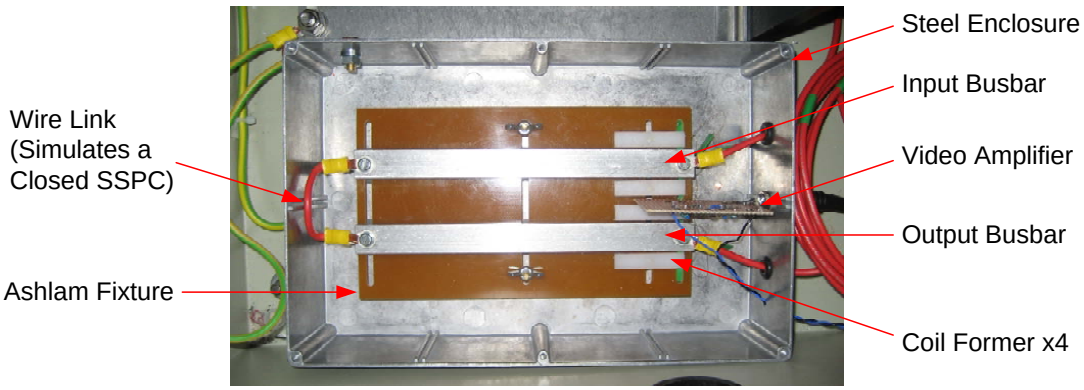


Figure 4.2: Rogowski Coil Current Transformer Hardware De-risk Rig Photograph

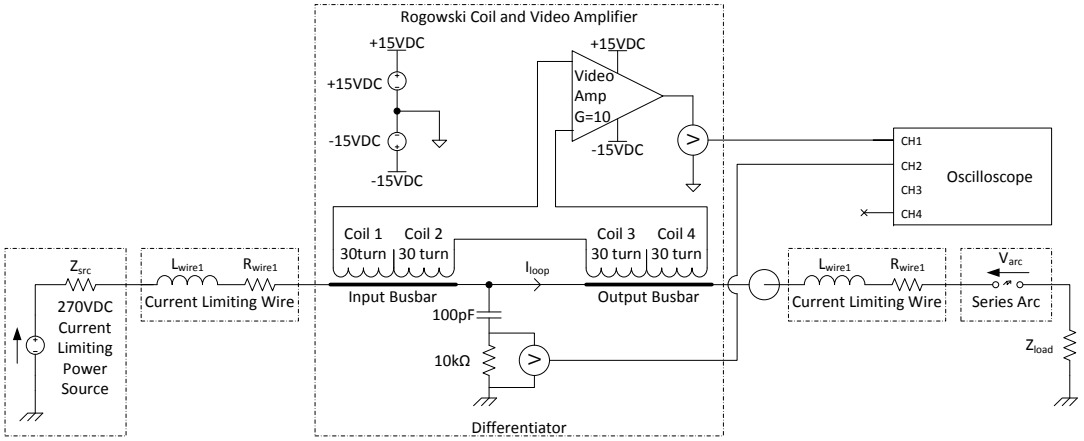


Figure 4.3: Rogowski Coil Current Transformer Hardware De-risk Rig Schematic

The Rogowski coil de-risk rig was configured in accordance with the schematic in Figure 4.3 for preliminary testing purposes. Each coil former was wound with 30 turns of enamelled Copper wire, and the video amplifier gain was set to 10. The video amplifier has a very high impedance input so that the Rogowski coils under test are not heavily loaded. The busbar was connected in circuit with a low impedance 270VDC power source, a 2A resistive load, and a "loose terminal" series arc fault consistent with the experimental method presented in Section A.3.2. The de-risk rig also contained an RC differentiator circuit for detection of SSPC output voltage

transients, and this will be discussed later in Section 4.4. Isolated differential voltage probes were used for the measurement of all voltages and a Hall effect current probe was used for measurement of current, where the bandwidth of all probes was 50MHz.

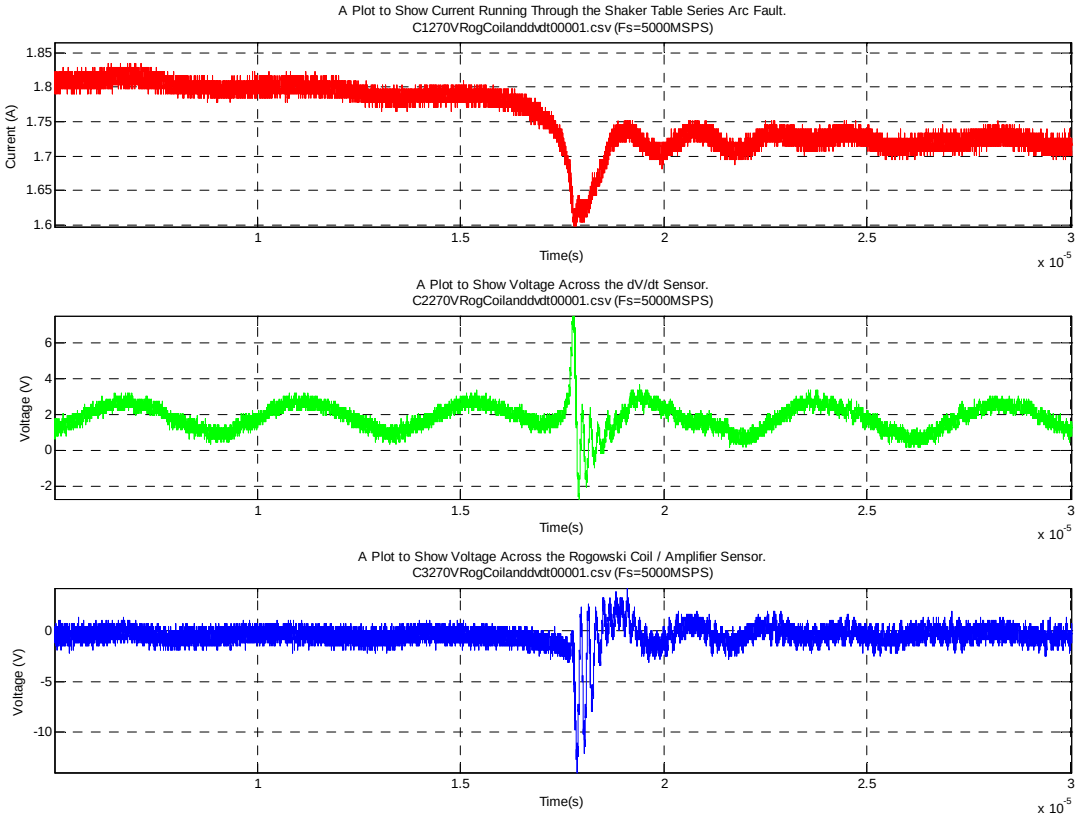


Figure 4.4: 270VDC Series Arc Waveform Plot Showing Rogowski Coil Behaviour

The results in Figure 4.4 show that during series arc strike there is a reduction in arc current, indicated in red, and the video amplifier output signal, indicated in blue, features a corresponding 10V peak signal which implies that a 1V peak output signal was present across the coils under test. High frequency resonance can also be observed and this is thought to be due to high interwinding capacitance. However, this does not affect the ability to detect the arc strike events or to determine the polarity of the $\frac{dI_{arc}}{dt}$ events. Furthermore the output from the voltage differentiator, indicated in green, shows a positive 7.5V signal thus providing confidence that an RC differentiator is capable of detecting the effect of series arc faults. These results gave the author confidence that 30 turns on the each of the four air cored coils was sufficient for series arc fault detection purposes, and thus the next stage of the project was to implement a planar Rogowski coil current transformer in the PEPDC PCB structure.

4.3.3.2 Planar Current Sensor Transfer Characteristics

The first stage of the planar current sensor design process was to determine the parameters which affect transformer performance. To maximise coupling between primary and secondary conductors the loop area of the secondary windings should be maximised and the secondary windings should be placed as close as possible to the primary conductor in order to maximise the mutual inductance between primary and secondary windings. Figure 4.5 shows a generic example of a single coil proposed for the PEPDC series arc fault detection current monitor solution. Since eight layer PCBs can be obtained readily, it is proposed that an eight layer board will provide flexibility for dense winding patterns. An eight layer board allows for six layers of turns with two empty layers on the outer faces of the PCB which protect the turns from harsh environments and offer an extra level of dielectric to limit high voltage voltage effects such as corona or partial discharge. Since there is a desire to maximise turn density it is assumed that track width w_{track} and gap width w_{gap} will be equal and set to the minimum gap size for the given PCB technology. Track width and gap width will be designated r hereafter. Figure 4.5 also presents an equivalence between the actual spiral configuration and an approximation consisting of concentric rectangles which simplify the evaluation of mutual inductance.

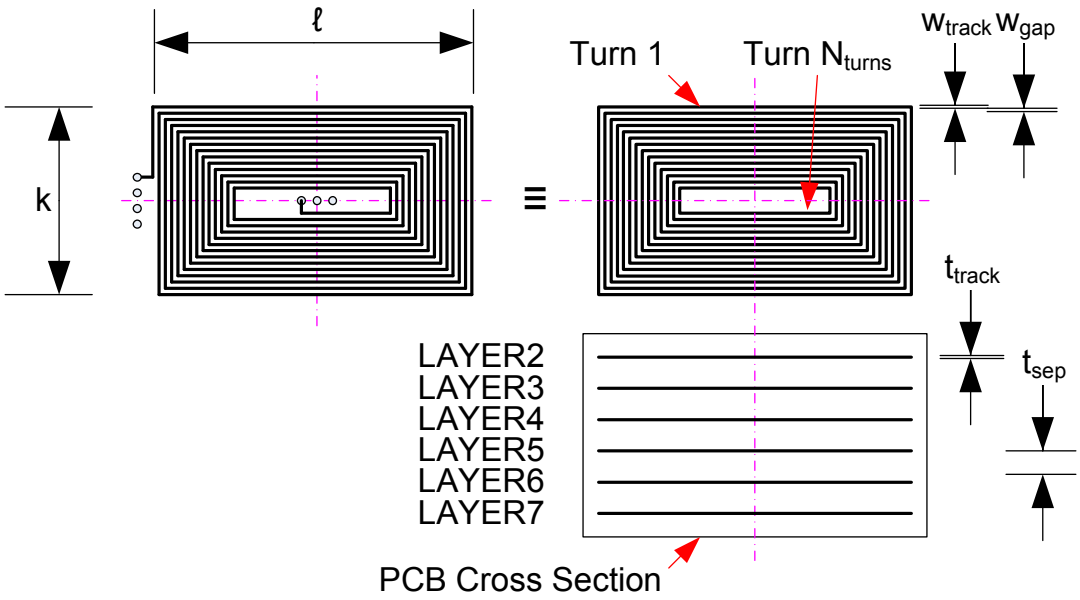


Figure 4.5: Proposed Spiral Inductor and Equivalent Model

Taking further inspiration from Gan who performed extensive work on optimisation of multi-layer current transformers with silicon substrates [231], it was determined that optimisation of a multi-layer PCB Rogowski coil implementation is complex. It was decided that rather than attempting to compute or model all parameters of a given Rogowski coil, the maximisation of the mutual inductance or coupling between

primary and secondary windings, and the minimisation of interwinding and interlayer capacitance would form the main focus of the project. To achieve this an equivalent circuit model of the proposed multi-layer current transformer was required.

Figures 4.6 and 4.7 show PEEC (Partial Element Equivalent Circuit) models of the proposed printed current transformer structure. The PEEC models were inspired by the work of Guillod et al regarding simpler PCB-based Rogowski coil structures [232]. The PEEC models are based on the 8 layer 2oz/ft^2 PEPDC PCB technology.

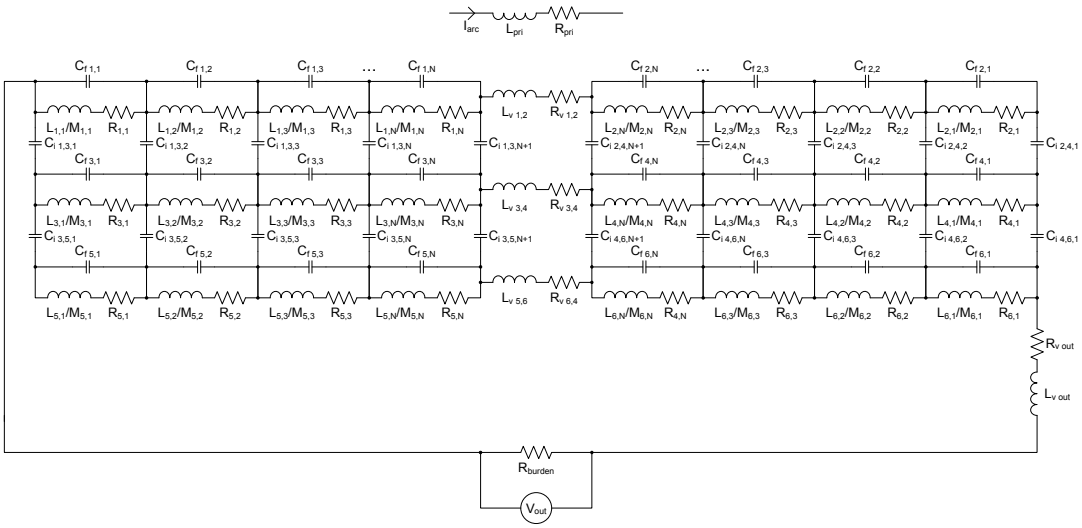


Figure 4.6: PEEC Model of Planar Current Transformer (Inc. Fringe Capacitance)

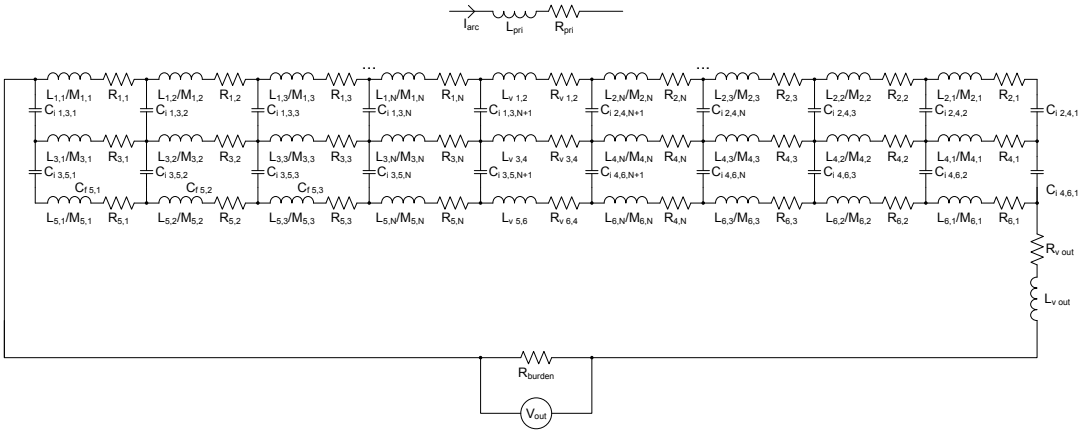


Figure 4.7: PEEC Model of Planar Current Transformer (Exc. Fringe Capacitance)

To understand how to maximise mutual inductance and minimise interwinding and interlayer capacitance to achieve maximum sensitivity and reduce the effects of resonance, it is necessary to determine how the printed current transformer structure

affects its performance, and therefore fringe capacitance, self inductance, interlayer capacitance, turn resistance and mutual inductance must be analysed.

Fringe Capacitance, $C_{f\,N_{layer},N_{turn}}$
Fringe capacitances are represented by $C_{f\,N_{layer},N_{turn}}$ and relate to the fringe capacitance between the PCB trace edges of two adjacent turns on the same PCB layer. Figure 4.6 shows a model including fringe capacitances and the simplified model in Figure 4.7 neglects the effect of fringe capacitances since PCB trace thickness t_{trace} is typically small with respect to the trace widths, where 2oz/ft^2 copper is 70μm thick and typical minimum trace widths t_{trace} are in the order of 0.15 to 0.2mm.

Self Inductance, $L_{N_{layer},N_{turn}}$
Self inductances are represented by $L_{N_{layer},N_{turn}}$ and refer to the self inductance of a given turn on a given layer of the PCB. Note that via inductance $L_{v\,N_{layer},N_{turn}}$ has been included in this model, although this is only important for very high frequency modelling. Computing self inductance for a multi-layer coil is a complex activity and it is proposed not to affect coil performance significantly. However, should self inductance calculation be necessary Kythakyapuzha proposes a method for calculating the self inductance by dividing the coil into a grid and calculating the flux by considering the effect of each turn on each layer on the flux within each compartment in the grid [233, p. 41]. Self inductance can also be computed easily using a 3D field solver tool.

Interlayer Capacitance, $C_{i\,N_{layer},N_{turn}}$
Interlayer capacitances are represented by $C_{i\,N_{layer},N_{turn}}$ and characterise the capacitance between every other layer since adjacent layers are offset by one track / gap width in order to ensure that there is no broadside capacitive coupling between directly adjacent PCB layers. This is the primary method of minimising parasitic capacitance and maximising resonant frequency of the current sensor design. It is therefore assumed that the fringe capacitance between turns on adjacent PCB layers is minimal. Capacitance between parallel plates can be computed in accordance with Equation (4.14) where A is equal to the plate area, d is equal to plate separation, and ϵ_0 and ϵ_r are the permittivity of free space and relative permittivity of the dielectric material respectively.

$$C = \frac{\epsilon A}{d} = \frac{\epsilon_0 \epsilon_r A}{d} \tag{4.14}$$

$$\begin{aligned} A &= (\ell - 4r(N-1))\,(k - 4r(N-1)) \\ &- (\ell - 4r(N-1) - 2r)\,(k - 4r(N-1) - 2r) \\ &= (l\ell - 4r(N-1))\,(k - 4r(N-1)) \\ &- (\ell - 4r(N-1) - 2r)\,(k - 4r(N-1) - 2r) \\ &= 2r(\ell - 2r - 4(N-1)(r-1)) \end{aligned} \tag{4.15}$$

$$C_i = \frac{2\epsilon_0 \epsilon_r r(\ell - 2r - 4(N-1)(r-1))}{2t_{sep}} \tag{4.16}$$

For an FR-4 PCB the relative permittivity is typically $\epsilon_r = 4.4$. Note that electric field fringe effects could result in fringe capacitances, which although difficult to compute by hand may be computed easily with 3D field solver tools. Equation (4.15) represents the coupling area between turn N on two opposing layers based on an simple algebraic analysis of Figure 4.5. For turn N on a given layer, the capacitance between this turn and the broadside coupled turn can be expressed as per Equation (4.16) where the spacing d between turns is $2t_{sep}$.

Turn Resistance, $R_{N_{layer},N_{turn}}$

Turn resistance is represented for each turn across each layer of the transformer coil. For example $R_{N_{layer},N_{turn}}$ represents the resistance of turn number N_{turn} on layer number N_{layer}. Turn resistance is affected by PCB metallisation resistivity ρ, track thickness t_{track} and PCB track width r. Resistance of the primary winding is given by R_{pri}, and via resistance although negligible is given by $R_{v\,N_{layer},N_{turn}}$. Turn resistance $R_{N_{layer},N_{turn}}$ is given in Equation (4.18), and can be derived by substituting PCB track cross sectional area A and turn perimeter length ℓ into the standard resistance Equation (4.17). Total resistance of a given spiral with N_{turns} turns, N_{layer} layers and N_{coils} can be found by evaluating Equation (4.19).

$$R = \frac{\rho\ell}{A} \tag{4.17}$$

$$R_{N_{layer},N_{turn}} = \frac{2\rho((\ell + k - 8r(N_{turn} - 1)))}{rt_{track}} \tag{4.18}$$

$$R_{total} = N_{layers}N_{coils}\sum_{N=1}^{N_{turns}} \frac{2\rho((\ell + k - 8r(N - 1)))}{rt_{track}} \tag{4.19}$$

Burden Resistors, R_{burden}

Burden resistors designated R_{burden} are connected to each planar coil to provide a controlled output impedance for the coil to drive. The output voltage of a given coil can be calculated in accordance with Equation (4.20).

$$V = M\left(\frac{R_{burden}}{R_{burden} + R_{coil}}\right)\frac{dI}{dt} \tag{4.20}$$

The key to maintaining sensitivity here is to ensure that $R_{burden} >> R_{coil}$, while choosing a sufficiently low value of R_{burden} to limit self resonance. For this application 100Ω burden resistors are used since they are two orders of magnitude greater in resistance and thus have minimal interaction with the coil resistance of 4.35Ω, which is given later in Table 4.1.

Mutual Inductance, $M_{N_{layer},N_{turn}}$

Mutual inductance between the primary winding L_{pri} and the other secondary windings is represented by $M_{N_{layer},N_{turn}}$.

The busbars used in both the PEPDC and PEPSC products are formed from rectangular profile material. Figure 4.8 illustrates a cross section of an arbitrary rectangular conductor. To understand the coupling in the PEPDC and PEPSC planar current transformers it is necessary to determine the mutual inductance between the rectangular busbar primary, and planar coil secondary. Mutual inductance varies with frequency, so to simplify the calculation of mutual inductance it is assumed that DC steady state magnetic field analysis allows calculation of the order of magnitude of the low frequency mutual inductance.

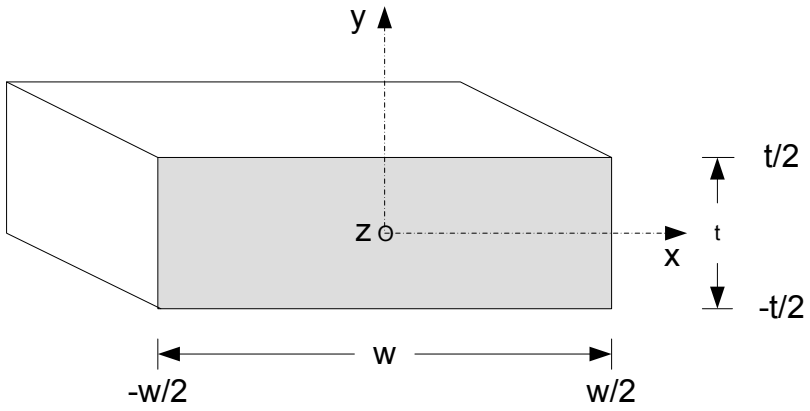


Figure 4.8: Cross Section of an Arbitrary Rectangular Conductor

Magnetic Field Around a Rectangular Cross Section

For an arbitrary cross section of straight conductor with current flowing along the z-axis (out of the page), the B-fields can be obtained from the z component of the magnetic vector potential A. For an arbitrary straight conductor with current I flowing along the z-axis, the x and y components B_x and B_y of the $\vec{B}$ field can be expressed in Equations (4.21) and (4.22) respectively [234].

$$B_x = \frac{\partial}{\partial y} A_z \tag{4.21}$$

$$B_y = -\frac{\partial}{\partial x} A_z \tag{4.22}$$

The magnetic vector potential for a long current-carrying conductor can be expressed as per Equation (4.23) where μ_0 is the permeability of free space.

$$A_z = -\frac{\mu_0}{4\pi} \int J \ln \left[\left(x - x^{'} \right)^2 + \left(y - y^{'} \right)^2 \right] dx^{'} dy^{'} + C \tag{4.23}$$

Current density J in the conductor can be expressed for total conductor current I, conductor width w and conductor thickness t which are illustrated in Figure 4.8.

$$J = \frac{I}{wt} \tag{4.24}$$

Evaluating Equation (4.23) with the conductor dimensions gives Equation (4.25).

$$A_z = -\frac{\mu_0 I}{4\pi wt} \int_{-t/2}^{t/2} \int_{-w/2}^{w/2} \ln \left[\left(x - x^{'} \right)^2 + \left(y - y^{'} \right)^2 \right] dx^{'} dy^{'} + C \tag{4.25}$$

With Equation (4.25) the x and y components of the magnetic field $\vec{B}$ can be determined, as given in Equations (4.26) and (4.27) respectively.

$$B_x = \frac{\mu_0 I}{2\pi wt}\int_{-t/2}^{t/2}\int_{-w/2}^{w/2}\frac{y^{'}-y}{(x^{'}-x)^2+(y^{'}-y)^2}dx^{'}dy^{'} \tag{4.26}$$

$$B_y = -\frac{\mu_0 I}{2\pi wt}\int_{-t/2}^{t/2}\int_{-w/2}^{w/2}\frac{x^{'}-x}{(x^{'}-x)^2+(y^{'}-y)^2}dx^{'}dy^{'} \tag{4.27}$$

In order to simplify the presentation of this mathematics, x and y components of magnetic field $\vec{B}$ can be represented as Equations (4.28) and (4.29) respectively.

$$B_x = \frac{\mu_0 I}{2\pi wt}W_1 \tag{4.28}$$

$$B_y = -\frac{\mu_0 I}{2\pi wt}W_2 \tag{4.29}$$

Where W_1 and W_2 can be defined in Equations (4.30) and (4.31) respectively.

$$\begin{aligned} W_1 = & \left(\frac{w+2x}{4}\right)\ln\left[\frac{(w/2+x)^2+(t/2-y)^2}{(w/2+x)^2+(t/2+y)^2}\right] \\ & +\left(\frac{w-2x}{4}\right)\ln\left[\frac{(w/2-x)^2+(t/2-y)^2}{(w/2-x)^2+(t/2+y)^2}\right] \\ & +(t/2-y)\left[\tan^{-1}\left(\frac{w-2x}{t-2y}\right)+\tan^{-1}\left(\frac{w+2x}{t-2y}\right)\right] \\ & -(t/2+y)\left[\tan^{-1}\left(\frac{w-2x}{t+2y}\right)+\tan^{-1}\left(\frac{w+2x}{t+2y}\right)\right] \end{aligned} \tag{4.30}$$

$$\begin{aligned} W_2 = & \left(\frac{t+2y}{4}\right)\ln\left[\frac{(w/2-x)^2+(t/2+y)^2}{(w/2+x)^2+(t/2+y)^2}\right] \\ & +\left(\frac{t-2y}{4}\right)\ln\left[\frac{(w/2-x)^2+(t/2-y)^2}{(w/2+x)^2+(t/2-y)^2}\right] \\ & +(w/2-x)\left[\tan^{-1}\left(\frac{t-2y}{w-2x}\right)+\tan^{-1}\left(\frac{t+2y}{w-2x}\right)\right] \\ & -(w/2+x)\left[\tan^{-1}\left(\frac{t-2y}{w+2x}\right)+\tan^{-1}\left(\frac{t+2y}{w+2x}\right)\right] \end{aligned} \tag{4.31}$$

These equations were plotted using MATLAB® in order to visualise the field pattern around both the PEPDC and PEPSC busbar cross-sections, the output can be found in Figures 4.9 and 4.10 respectively.

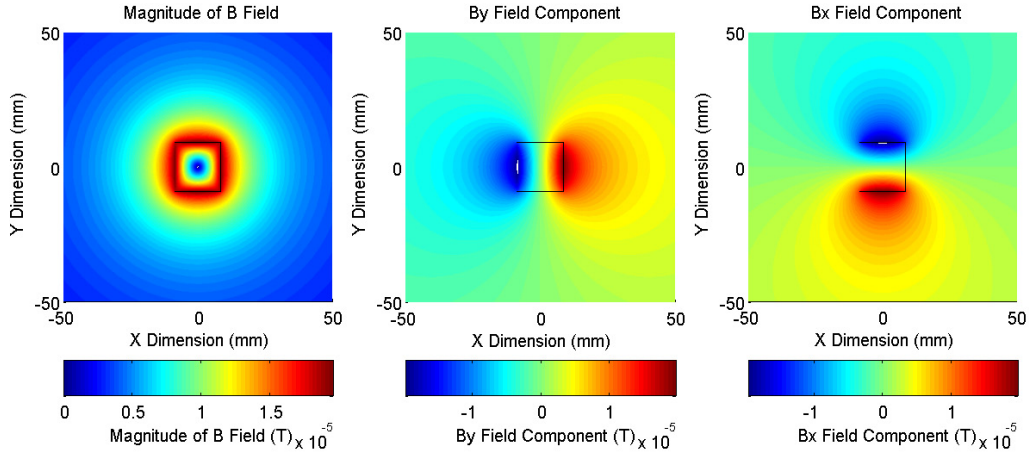


Figure 4.9: Cross Section of PEPDC Busbar (t =18.2mm,w =17mm)

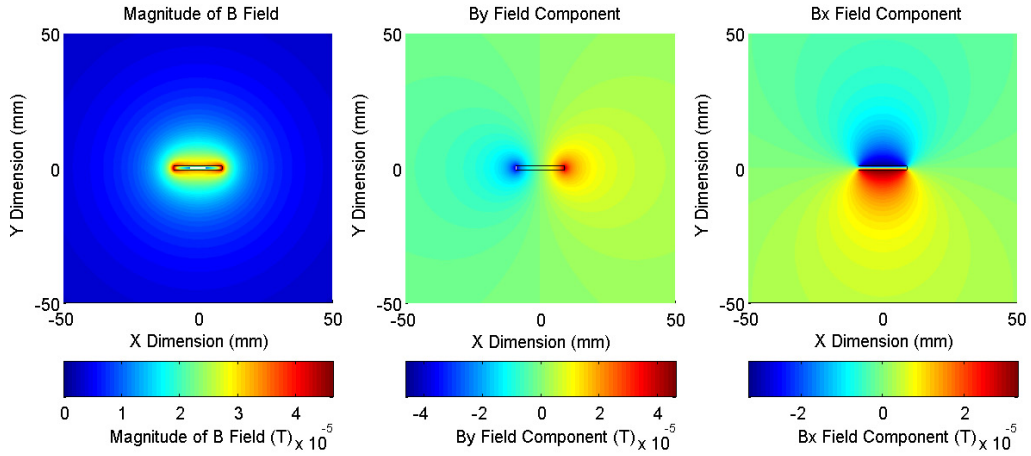


Figure 4.10: Cross Section of PEPSC Busbar (t =1.5mm,w =18mm)

Case 1 - PEPDC - Coils Mounted at $y = -t/2$

Using Faraday's Law of induction given in Equation (4.32) it is possible to derive an expression for mutual inductance between the rectangular conductor and rectangular loops positioned in the XZ plane at positions $y = -t/2$ and $y = 0$ representing the PEPDC and PEPSC scenarios respectively.

$$\phi = \int \vec{B} \cdot d\vec{A} \tag{4.32}$$

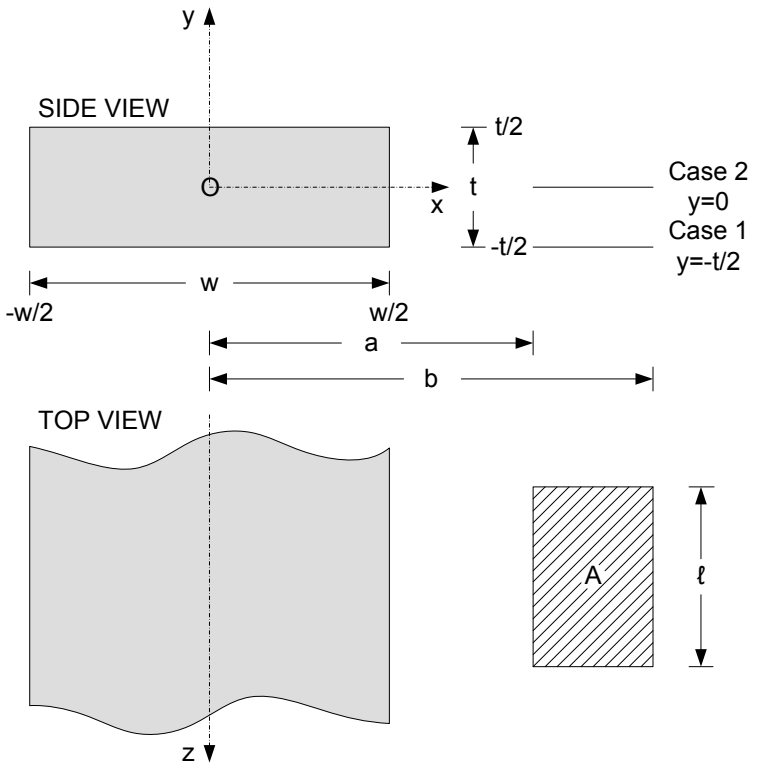


Figure 4.11: Arbitrary Rectangular Conductor Showing Two Rectangular Coil Cases

Firstly make the assumption that the coil is mounted in plane with the underside of the rectangular conductor as is the case with the PEPDC busbar configuration which is illustrated in Figure 4.11 where $y = -t/2$.

Magnetic flux ϕ induced by the rectangular conductor into the rectangular coil can be expressed by Equation (4.33), where the rectangular coil is sensitive to the y component of the magnetic field B_y only.

$$\phi = \frac{\mu_0 I \ell}{2\pi w t} \int B_y dx \tag{4.33}$$

Mutual inductance M between the rectangular conductor and a given rectangular turn can therefore be expressed by Equation (4.34).

$$M = \frac{\phi}{I} = \frac{\mu_0 \ell}{2\pi w t} \int B_y dx \tag{4.34}$$

Considering mutual inductance M between limits b and a as illustrated in Figure 4.11 gives Equation (4.35). The PTC Mathcad® symbolic processor [235] was used to evaluate the Equation (4.35), which yielded the mutual inductance $M(a, b, \ell)$ in Equation (4.36) as a function of the rectangular coil dimensions.

$$M = \frac{\mu_0 \ell}{2\pi w t} \int_{x=a}^{x=b} B_y dx \tag{4.35}$$

$$
\begin{aligned}
M(a,b,\ell) \;=\; & \frac{\mu_0 \ell}{2\pi w t}\left[\frac{tx\ln\left(\dfrac{t^2+\left(x-\dfrac{w}{2}\right)}{t^2+\left(x+\dfrac{w}{2}\right)}\right)}{2} + tx\right. \\
& + \frac{t\ln\left(t^2+w\sqrt{-t^2}-\dfrac{w^2}{4}+x^2\right)\left(\sqrt{-t^2}-\dfrac{w}{2}\right)}{2} \\
& - \frac{t\ln\left(t^2-w\sqrt{-t^2}-\dfrac{w^2}{4}+x^2\right)\left(\sqrt{-t^2}+\dfrac{w}{2}\right)}{2} \\
& - \frac{x^2\arctan\left(\dfrac{2t}{w-2x}\right)}{2} + \frac{x^2\arctan\left(\dfrac{2t}{w+2x}\right)}{2} \\
& - \frac{t^2\arctan\left(\dfrac{x-\frac{w}{2}}{t}\right)}{2} - \frac{t^2\arctan\left(\dfrac{x+\frac{w}{2}}{t}\right)}{2} \\
& - \frac{w^2\arctan\left(\dfrac{x-\frac{w}{2}}{t}\right)}{8} - \frac{w^2\arctan\left(\dfrac{x+\frac{w}{2}}{t}\right)}{8} \\
& \left. + \frac{wx\arctan\left(\dfrac{2t}{w-2x}\right)}{2} + \frac{wx\arctan\left(\dfrac{2t}{w-2x}\right)}{2}\right]_{x=a}^{x=b}
\end{aligned}
\tag{4.36}
$$

Total mutual inductance between the primary and secondary windings M_{total} can be computed by evaluating Equation (4.37), which references the mutual inductance function $M(a,b,\ell)$ from Equation (4.36), for N_{layer} layers and N_{coils} coils with N_{turns} turns per layer.

$$
M_{total} = N_{layers}N_{coils}\sum_{N=1}^{N_{turns}}\left[\frac{\mu_0\left(\ell-4r(N-1)\right)}{2\pi w t}M(a,b,\ell)\right] \tag{4.37}
$$

where...

$$
a \;=\; s+k-2r(N-1) \tag{4.38}
$$

$$
b \;=\; s+2r(N-1) \tag{4.39}
$$

Case 2 - PEPSC - Coils Mounted at $y = 0$

Now for the PEPSC busbar implementation make the assumption that the coil is mounted in the XZ plane of x with the centre of the rectangular conductor where $y = 0$. Magnetic flux ϕ_{21} induced by the rectangular conductor into the rectangular coil can be expressed by Equation (4.40), where the rectangular coil is sensitive to the y component of the magnetic field B_y only.

$$\phi = \frac{\mu_0 I \ell}{2\pi w t} \int B_y dx \tag{4.40}$$

Therefore mutual inductance M between the rectangular conductor and the rectangular coil can be expressed by Equation (4.41).

$$M = \frac{\phi}{I} = \frac{\mu_0 \ell}{2\pi w t} \int B_y dx \tag{4.41}$$

Considering mutual inductance M between limits b and a as illustrated in Figure 4.11 gives Equation (4.42). Again the PTC Mathcad® symbolic processor [235] was used to evaluate Equation (4.41) which yielded the mutual inductance $M(a, b, \ell)$ in Equation (4.43) as a function of the rectangular coil dimensions.

$$M = \frac{\mu_0 \ell}{2\pi w t} \int_{x=a}^{x=b} B_y dx \tag{4.42}$$

$$\begin{aligned}
M(a,b,\ell) = \frac{\mu_0 \ell}{2\pi w t} \Bigg[& \frac{tx \ln\left(\dfrac{\dfrac{t^2}{4} + \left(x - \dfrac{w}{2}\right)^2}{\dfrac{t^2}{4} + \left(x + \dfrac{w}{2}\right)^2}\right)}{2} + tx \\
& + \frac{t \ln\left(\dfrac{t^2}{4} + w\sqrt{-\dfrac{t^2}{4}} - \dfrac{w^2}{4} + x^2\right)\left(\sqrt{-\dfrac{t^2}{4}} - \dfrac{w}{2}\right)}{2} \\
& - \frac{t \ln\left(\dfrac{t^2}{4} - w\sqrt{-\dfrac{t^2}{4}} - \dfrac{w^2}{4} + x^2\right)\left(\sqrt{-\dfrac{t^2}{4}} + \dfrac{w}{2}\right)}{2} \\
& - x^2 \arctan\left(\frac{t}{w - 2x}\right) + x^2 \arctan\left(\frac{t}{w + 2x}\right) \\
& + \frac{t^2 \arctan\left(\dfrac{w - 2x}{t}\right)}{4} - \frac{t^2 \arctan\left(\dfrac{w + 2x}{t}\right)}{4} \\
& + \frac{w^2 \arctan\left(\dfrac{w - 2x}{t}\right)}{4} - \frac{w^2 \arctan\left(\dfrac{w + 2x}{t}\right)}{4} \\
& + wx \arctan\left(\frac{t}{w - 2x}\right) + wx \arctan\left(\frac{t}{w + 2x}\right) \Bigg]_{x=a}^{x=b}
\end{aligned} \tag{4.43}$$

Total mutual inductance between the primary and secondary windings M_{total} can be computed by evaluating Equation (4.44), which references the mutual inductance function $M(a, b, \ell)$ from Equation (4.43), for N_{layer} layers and N_{coils} coils with N_{turns} turns per layer.

$$M_{total} = N_{layers} N_{coils} \sum_{N=1}^{N_{turns}} \left[\frac{\mu_0 \left(\ell - 4r(N-1) \right)}{2\pi wt} M(a, b, \ell \right] \tag{4.44}$$

where...

$$a = s + k - 2r(N-1) \tag{4.45}$$

$$b = s + 2r(N-1) \tag{4.46}$$

4.3.3.3 Final Current Monitor Design Baseline

Table 4.1 illustrates the parameters used to create the planar current transformers for the PEPDC and PEPSC units, based on the maximum coil dimensions and maximum number of coil layers allowable for both the PEPDC and PEPSC applications. Table 4.1 also shows the computed mutual inductance and coil resistances for each scenario.

Parameter	**PEPDC Value**	**PEPSC Value**
Number of Turns per Layer, N_{turns}	14	14
Number of Layers, N_{layer}	6	6
Number of Coils, N_{coils}	4	2
Turn Width, k (mm)	12.0	12.2
Turn length, ℓ (mm)	20.4	16.6
PCB Track/gap Width, r (mm)	0.2	0.2
Busbar Thickness, t (mm)	16.2	1.5
Busbar Width, w (mm)	17	18
Burden Resistor, R_{burden} (Ω)	100	100
Total Mutual Inductance, M_{total} (nH)	385.02	210.80
Total Coil Resistance R_{total} (Ω)	4.35 per coil	7.33 per coil

Table 4.1: PEPDC and PEPSC Planar Current Transformer Parameters

Figure 4.12 shows a block diagram representation for the series arc fault current monitor system for both the PEPDC and PEPSC units. A signal is derived from variations in the SSPC output current which is detected by the planar Rogowski current transformer. This transformer is loaded with a burden resistor in order to limit coil resonance and to provide a finite resistance across the windings. This signal is fed into a two stage amplifier with selectable bypass, thus enabling the current transformer output signal to be scaled as necessary. At this stage the signal can be fed directly into a microcontroller ADC, or peak detected and compared to a set threshold which can be used to trigger a series arc fault event within a microcontroller. The series arc fault current monitor is hardware configurable such that the first attempt

at a hardware solution can be adjusted in order to give reliable detection results. The full hardware schematic for the series arc fault current monitor can be found in Appendix C.7.

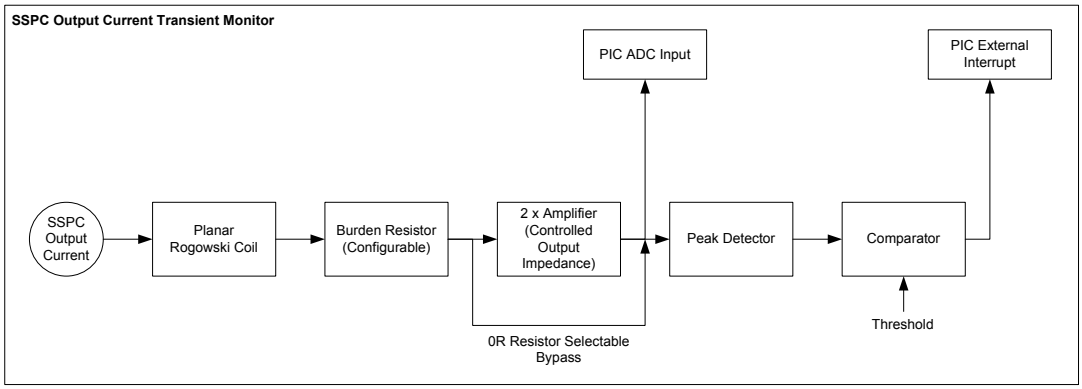


Figure 4.12: SSPC Series Arc Fault Current Monitor Block Diagram

4.3.4 Testing and Analysis of Multi-Layer PCB Current Monitors

With candidate planar current transformer designs in place for the PEPDC and PEPSC SSPC modules, the performance of both designs can now be evaluated. The time domain testing in this section allows the step response of the planar current transformer design to be measured thus determining the magnitude of the mutual inductance and the sensitivity to series arc fault events. Frequency domain testing is included in Appendix C.4 for completeness, and this allows the resonant characteristics of the planar current transformer design to be measured, where the goal is to achieve a high resonant frequency thus allowing a wide measurement bandwidth.

4.3.4.1 PEPSC Current Step Response

The step response of the planar current transformer to current can be used to measure the mutual inductance. Figure 4.13 shows the secondary winding response to a current step with a given rate of change of primary current in the time domain. Although there is a sign of resonant behaviour in the secondary winding during the transient event this is minimal in comparison to the desired signal and can be filtered if necessary to prevent disruption to other control electronics in the SSPC.

Figure 4.14 displays the peak secondary winding time domain voltage data illustrated in Figure 4.13 as a function of rate of change of current, where it can be seen that the experimental data follows the predicted mutual inductance trend.

Measured coil resistance was $R_{coil} = 9.8\Omega$ in contrast to the predicted 7.33Ω. With a large burden resistor R_{burden} of 100Ω this deviation is very small. It is proposed that this is due to track width and track thickness variation in the PCB.

In conclusion the sensitive PEPSC current transformer provides peak output signals in the order of 100mV through 5V for the six different current step waveforms with rates of change of current in the range 1 through 25A/μs. The interwinding capacitance optimised layout provides a step response with good stability.

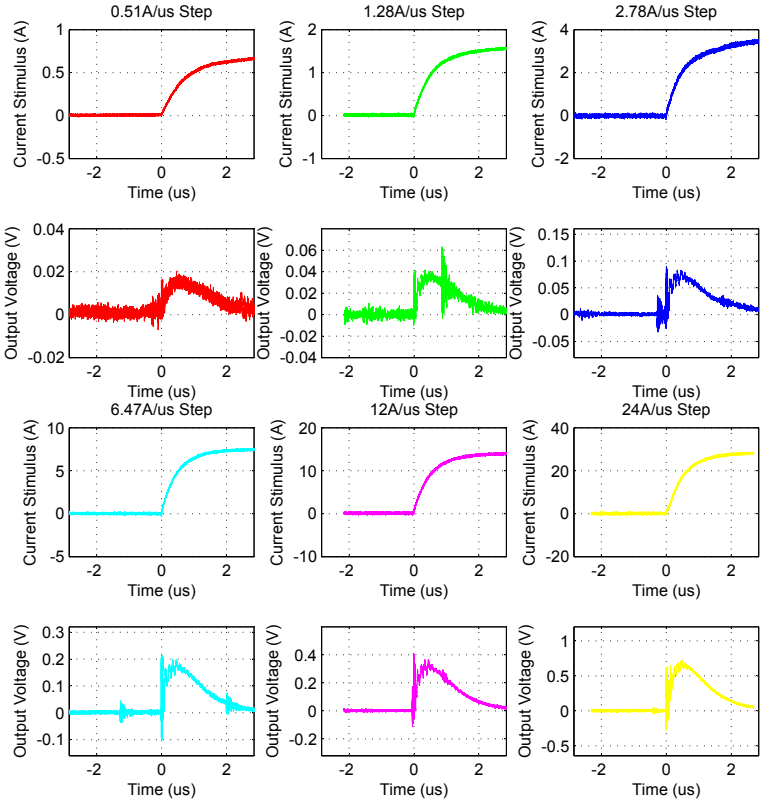


Figure 4.13: PEPSC Planar Coil Voltage Response to Current Step

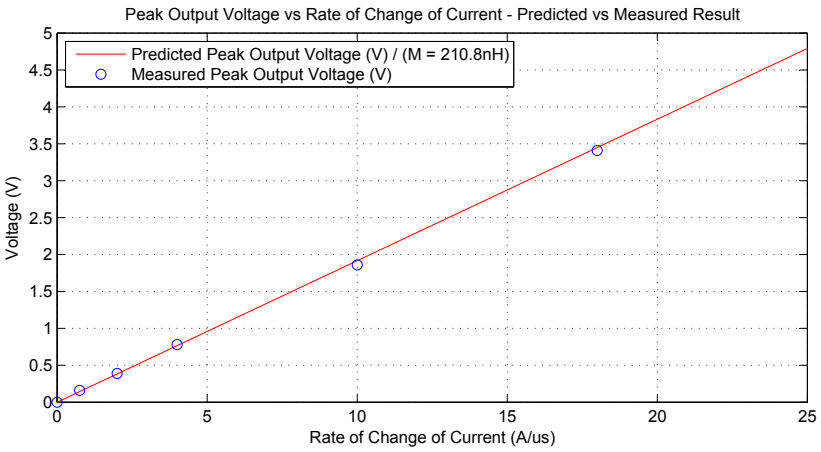


Figure 4.14: PEPSC Planar Coil Output Voltage - Predicted vs Measured

4.3.4.2 PEPDC Current Step Response

Again with the PEPDC hardware the critical performance requirement here is the current step response of the planar current transformer. Figure 4.15 shows the PEPDC secondary winding response to a current step with a given rate of change of primary current in the time domain. Although there is a sign of resonant behaviour in the secondary winding during the transient event this is minimal in comparison to the desired signal and can be filtered if necessary to prevent disruption to other control electronics in the SSPC.

Figure 4.16 displays the peak secondary winding time domain voltage data illustrated in Figure 4.15 as a function of rate of change of current, where it can be seen that the experimental data follows the predicted mutual inductance trend.

Measured coil resistance was $R_{coil} = 6.2\Omega$ in contrast to the predicted 4.35Ω suggesting variation in the PCB copper weight and/or trace widths, and additional parasitic resistances in the measuring system. With a burden resistor R_{burden} of 100Ω this deviation is insignificant.

Comparing the mutual inductances of the PEPDC and PEPSC current transformers reveals that the PEPDC current transformer is 84% more sensitive than the PEPSC solution given the additional coils and larger winding areas, and provides peak output signals in the order of 100mV through 5.5V for the fifteen current step waveforms with rates of change of current in the order 1 through 15A/μs.

In conclusion both the PEPSC and PEPDC multi-layer interwinding capacitance optimised planar current transformers provide good step response and stability performance in the time domain, where the experimental measurements accurately match the predicted mutual inductance values calculated in Section 4.3.3.

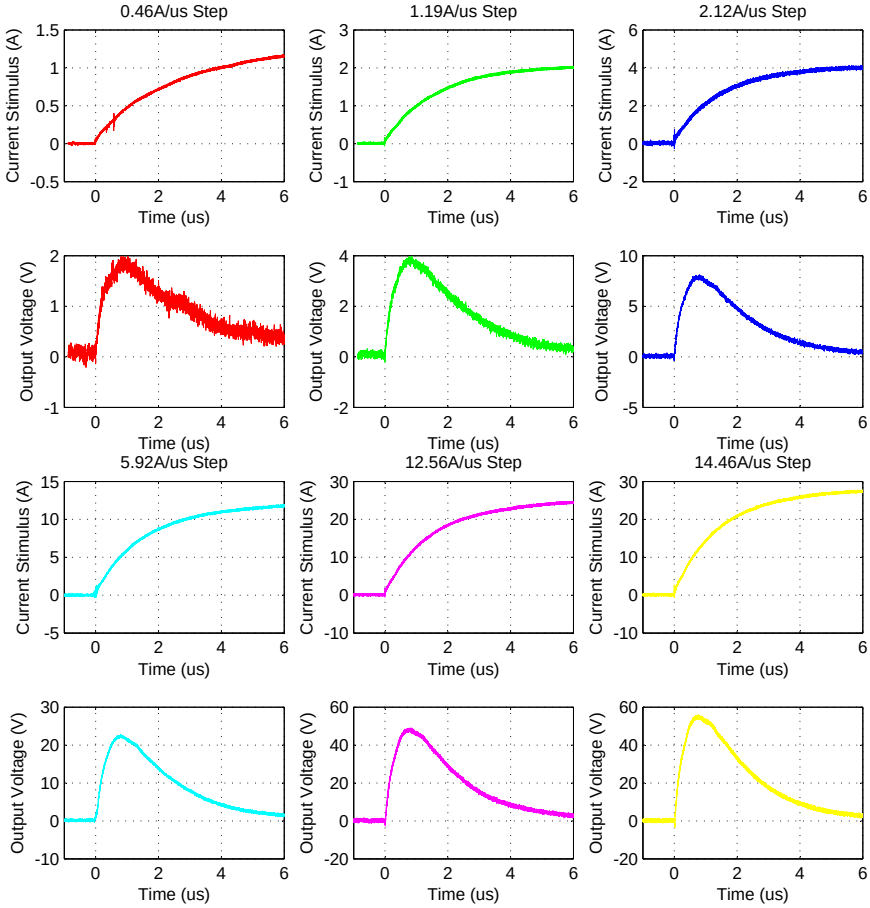


Figure 4.15: PEPDC Planar Coil Time Domain Measurements

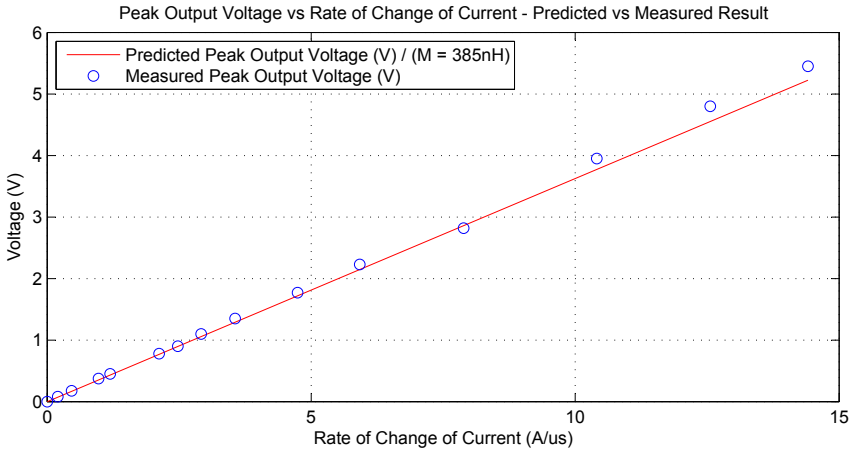


Figure 4.16: PEPDC Planar Coil Output - Predicted vs Measured

4.4 Series Arc Fault Voltage Sensor Development

4.4.1 Hardware Requirements for the Series AFD Voltage Sensor

There are five derived hardware requirements to consider for the series arc fault detection voltage sensor. Hardware requirements [**h01**], hardware goals [**h01g**] and hardware information statements [**h01_i**] are provided thus.

4.4.1.1 Voltage Sensor Range, Sensitivity and Bandwidth

Parent Requirements: [**01**], [**02**], [**03**], [**04**], [**07**], [**08g**], [**09g**]

[**h06**] The series arc fault voltage sensor **shall** be sensitive enough to detect positive step changes in voltage of at least $\Delta V_{sspcout} = 1.36\text{V}$.

[**h06_i**] Assuming firstly that the line/load snubber networks in the SSPC do not affect the SSPC output voltage signal $V_{sspcout}$ when the switch is closed, secondly that there is a minimum ratio of 1:10 between upstream inductance L_{up} and downstream inductance L_{dn} giving Equation (4.47), and finally that the minimum arc voltage V_{arc} during arc strike is 15V, then the minimum voltage deviation at the SSPC output during arc strike can be calculated in Equation (4.48).

$$L_{dn} = 10L_{up} \tag{4.47}$$

$$\Delta V_{sspcout} = V_{arc}\frac{L_{up}}{L_{up}+L_{dn}} = 15 \times \frac{1}{11} = 1.36V \tag{4.48}$$

[**h07**] The series arc fault voltage sensor **shall** have a bandwidth sufficient to capture a $1.36\text{V}/\mu\text{s}$ step in SSPC output voltage during arc strike.

[**h07_i**] The bandwidth of the series arc fault voltage sensor needs to be sufficient to capture the rising edge of the arc voltage, which is superimposed on the SSPC output voltage during an arc strike event, where the rise time of the minimum voltage step $\Delta V_{sspcout} = 1.36\text{V}$ is in the order of $1\mu\text{s}$.

[**h08**] The series arc fault voltage sensor **shall** have a high-pass 3dB cutoff frequency above 1MHz.

[**h08_i**] This requirement is intended to reject line resonance caused predominantly by cable inductance and load capacitance. This cutoff frequency also filters out low frequency power quality variations and audio frequency susceptibility signals.

4.4.1.2 SSPC Integration and High Voltage Insulation

Parent Requirements: [**04**]

[**h09g**] The series arc fault voltage sensor **should** be capable of providing an analogue signal in the range 0V through 3.3V to a microprocessor whose ground is referenced to the given SSPC output voltage.

[h09g_i] The microcontroller on both the PEPDC and PEPSC designs has a ground reference on the output of the SSPC in order to enable current monitoring and gate control for the MOSFETs used in the design. The microcontroller is powered from a 3.3VDC power supply which is also referenced to the SSPC output voltage. The SSPC output voltage can be in the range -1VDC through 350VDC with respect to aircraft chassis.

[h10] The series arc fault voltage sensor **shall** be capable of providing electrical isolation for steady state voltages of at least +350VDC and transient voltages of at least +700VDC with respect to aircraft chassis.

[h10_i] This requirement ensures that the SSPC output voltage referenced series arc fault voltage sensor hardware is suitably isolated from aircraft chassis for safety purposes. In addition to safety the voltage sensor and processing electronics needs to tolerate the +700V switching transient which occurs each time that the SSPC is opened under load.

4.4.2 Existing / Typical SSPC Voltage Sensor

In the interest of designing a cost-competitive product the goal outlined in the top level system requirements is to reuse the existing SSPC voltage monitoring system. The PEPDC and PEPSC units both feature hardware and software which samples the output voltage of the SSPC with a resolution of $N_{bits} = 12$ bits and a sampling rate of 50kSPS. The output voltage range covers approximately $V_{range} = 1000$V and therefore the value of 1 Least Significant Bit (LSB) can be calculated in accordance with Equation (4.49).

$$1LSB = \frac{V_{range}}{2^{N_{bits}}} = \frac{1000}{2^{12}} = 0.24V \tag{4.49}$$

Based on requirement **[h06]** it was determined that a minimum positive voltage step of 1.36V would be present at the SSPC output voltage during arc strike and therefore the Analogue-to-Digital Converter (ADC) has sufficient resolution to measure the voltage step. Unfortunately a sampling rate of 50kSPS gives a sampling period is 20μs and referring to requirement **[h07]** it was determined that the voltage step occurs in 1μs and therefore the sampling rate is insufficient to measure this edge. In addition to this the sampling rate is limited by the throughput of the PIC microcontroller used for the main SSPC function, and there is no scope to increase the sampling rate significantly due to the processing overhead of the other SSPC functions. Therefore the sampled voltage monitor is adequate for the other SSPC protection mechanisms, but it is not suitable for series arc fault detection.

4.4.3 Design of a Series Arc Fault Voltage Sensor

Since cost is an issue and the existing SSPC voltage monitor cannot be used due to the deliberately low sampling rate of the SSPC output voltage, a simple hardware RC differentiator circuit was used for this application. The differentiator needs to capture the arc strike voltage transient of 1.36V/μs, and limit bandwidth to 1MHz to prevent susceptibility to power quality variations.

4.4.3.1 Voltage Monitor Block Diagram

Figure 4.17 shows a proposed block diagram representation for the series arc fault voltage monitor system for both the PEPDC and PEPSC units.

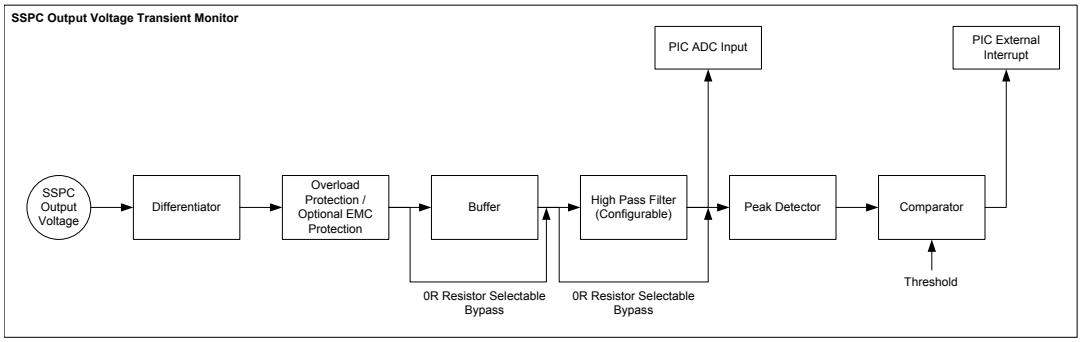


Figure 4.17: SSPC Series Arc Fault Voltage Monitor Block Diagram

The series arc fault voltage monitor first uses an RC differentiator to detect fast changes in SSPC output voltage. Overload protection and provision for EMC protection are included to minimise the risk of PCB re-spin after the initial prototyping activity. A buffer circuit is provided with a selectable 0Ω bypass resistor, to allow control of the signal impedance supplied to the next stage. A Sallen-Key second order high pass filter is included if a steeper slope is required for the differentiator circuit to reject low frequency interference in a given aircraft application. The output of this filter is then fed into a microcontroller ADC for sampling, if required, and is also fed into a peak detector / comparator with a configurable threshold, where a discrete detection output is fed into a microcontroller external interrupt port allowing immediate response to a given arc event.

4.4.3.2 Differentiator Design

The high-side microprocessor design used on the PEPDC / PEPSC, where the microprocessor is referenced to the SSPC output voltage, drives the design of a novel differentiator circuit since the ground reference for the microprocessor floats on the signal of interest. Figures 4.18 and 4.19 show SPICE frequency domain and time domain simulation schematics respectively, where V_{src} represents the line power input at

270VDC, R_{up} and L_{up} represent the input feeder impedance, S1 represents the SSPC switch, R_{dn} and L_{dn} represent the output feeder impedance and R_{load} represents the load element. Also included are $R_{snubber1}$ and $C_{snubber1}$, $R_{snubber2}$ and $C_{snubber2}$ which represent the input and output snubber impedances respectively. A 3V0 precision DC reference voltage V2 is also available to provide accurate offsets and thresholds.

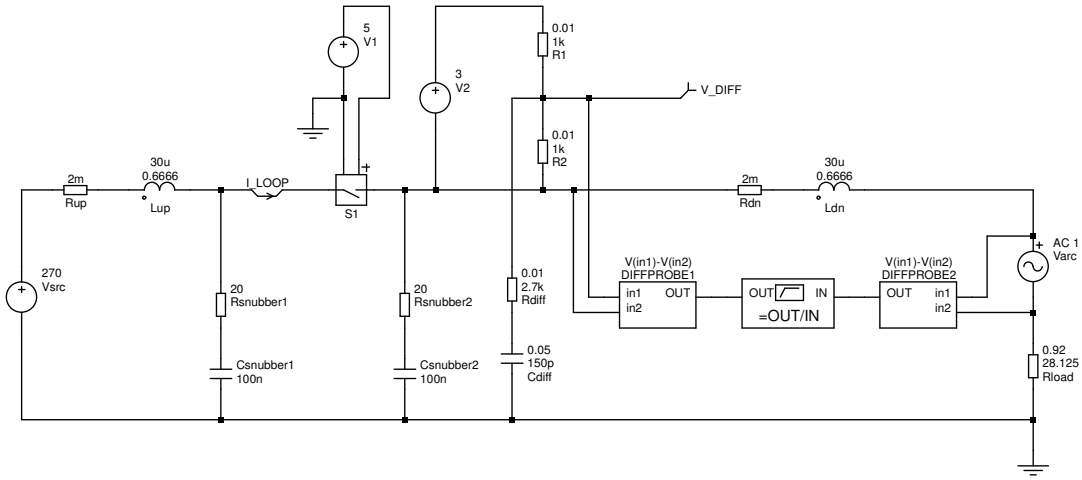


Figure 4.18: Series Arc Fault Voltage Monitor Frequency Domain Analysis Schematic

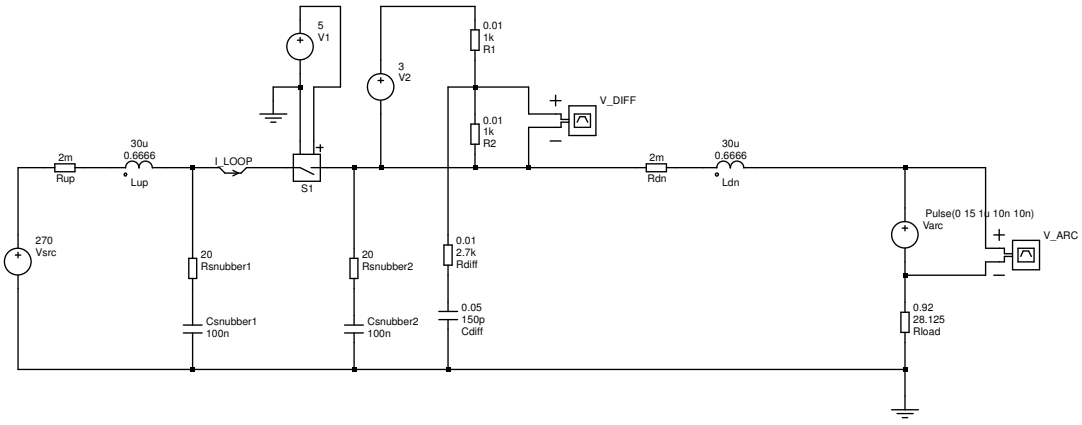


Figure 4.19: Series Arc Fault Voltage Monitor Time Domain Analysis Schematic

The novel differentiator circuit consists of resistors R_1 and R_2 which create an SSPC output voltage referenced Thévenin equivalent source with source voltage 1.5V and an output impedance of 500Ω [236]. The centre point between R_1 and R_2 is connected via resistor R_{diff} and capacitor C_{diff} to the aircraft chassis reference. When there is a positive step in SSPC output voltage, current flows out of resistors R_1 and R_2 through resistor R_{diff} and capacitor C_{diff} to aircraft chassis, resulting in a voltage drop at the junction of resistors R_1, R_2 and R_{diff}, thus indicating that an arc strike event has taken place. The change in voltage seen at the SSPC output $\Delta V_{sspcout}$ assuming

that the rise time of the arc voltage is instantaneous is given by Equation (4.50), and the corresponding peak differentiator voltage output $\hat{V}_{diff}$ is given by Equation (4.51). Varying R_{diff} therefore allows the peak differentiator voltage output $\hat{V}_{diff}$ to be configured for the required attenuation.

$$\Delta V_{sspcout} = V_{arc}\frac{L_{up}}{L_{up}+L_{dn}} \tag{4.50}$$

$$\hat{V}_{diff} = \Delta V_{sspcout}\frac{R_1 \parallel R_2}{(R_1 \parallel R_2)+R_{diff}} \tag{4.51}$$

From requirement **[h06]** it was determined that a minimum positive voltage step of 1.36V is present on the SSPC output voltage during arc strike, based on a minimum arc voltage $V_{arc} = 15$V and an upstream to downstream inductance ratio of 1:10. From these assumptions the peak differentiator output voltage $\hat{V}_{diff}$ can be calculated in accordance with Equation (4.52).

$$\hat{V}_{diff} = 1.36 \times \frac{500}{500+2700} = 0.213V \tag{4.52}$$

A value of 0.213V when subtracted from the 1.5V offset voltage created by R_1 and R_2 allows a detection threshold voltage for the hardware comparator detection circuit to be set to 1.3V, thus allowing detection of the minimum series arc fault voltage signal.

The value of capacitor C_1 is selected to give the required high frequency response while attenuating audio frequency and low frequency RF interference. Voltages up to +700V can be seen across capacitor C_1 during operation of the SSPC so the minimum dielectric withstand voltage for the capacitor must be at least 1000V to fulfil aerospace component derating requirements. A high stability dielectric such as NP0 is required for capacitor C_1 since variation in the capacitance value dramatically affects series arc fault detection performance. Since the PEPDC and PEPSC PCBs contain predominantly surface mount components, a surface mount capacitor is desired, and thus to achieve IPC-2221A [237] compliant conductor clearance requirements for 1000V signals a 2220 Multi Layer Chip Capacitor (MLCC) package is required. The aerospace environment subjects components to high levels of vibration and temperature cycling and with standard rigid capacitor terminations, there is a high risk that capacitors will fail open circuit. Introducing larger surface mount chip capacitors with rigid terminations reduces robustness significantly, and as such the 2220 packaged capacitor used in the PEPDC and PEPSC features flexible terminations to avoid component fracture under thermal and mechanical stress. Since the project needs to use Commercial Off-The-Shelf (COTS) parts, this limits the range of available values and the most suitable value available was 150pF. The 3dB cutoff frequency f_{3dB} of the resulting circuit is given by Equation (4.53).

$$f_{3dB} = \frac{1}{2\pi\left(R_{diff}+\frac{R_1R_2}{R_1+R_2}\right)C_{diff}} = \frac{1}{2\pi\left(2.7k+\frac{1k\times 1k}{1k+1k}\right)150p} = 332kHz \tag{4.53}$$

To validate the differentiator design two 2000 cycle Monte Carlo simulations were carried out to determine the frequency and time domain responses for the scenario where L_{up} and L_{dn} is in the range 10μH through 50μH and R_{load} is in the range 54Ω through 2.25Ω representing the required 5A through 120A load current range. It is assumed that the effects of R_{up} and R_{dn} are not significant since the resistances are typically three orders of magnitude less than the load resistor. Snubber capacitors $C_{snubber1}$ and $C_{snubber2}$ have a tolerance of $\pm$5%, and the remaining resistors $R_{snubber1}$, $R_{snubber2}$, R_1, R_2 and R_{diff} have a tolerance of $\pm$1%. Figures 4.20 and 4.21 illustrate the results of the frequency domain and time domain Monte Carlo simulations

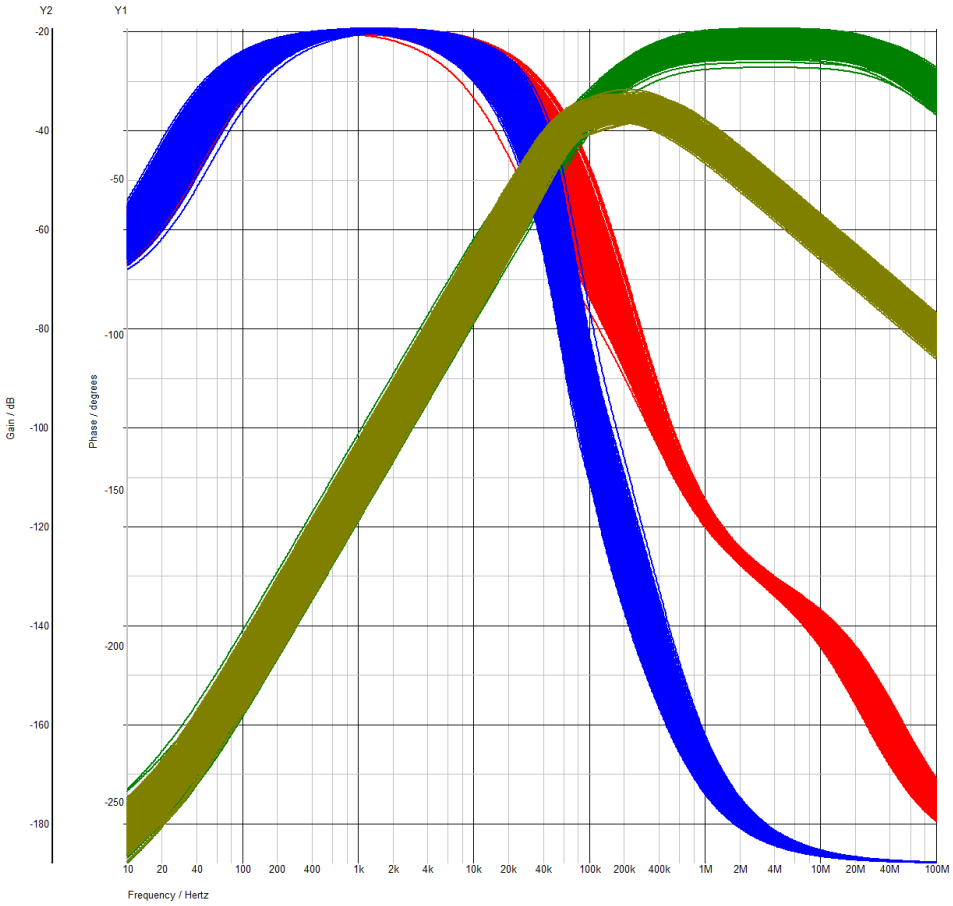


Figure 4.20: SSPC Series Arc Fault Voltage Monitor Monte Carlo Frequency Domain Analysis Plot (Green = Gain (No Snubber), Red = Phase (No Snubber), Beige = Gain (With Snubber), Blue = Phase (With Snubber))

Figure 4.20 presents the variation of the transfer function between arc voltage V_{arc} and differentiator output V_{diff} over the frequency range 10Hz through 100MHz. Figure 4.20 illustrates clearly the effect of the snubber components $C_{snubber1}$, $C_{snubber2}$, $R_{snubber1}$ and $R_{snubber2}$ where these components lead to high frequency attenuation. The 3dB cutoff frequency of the differentiator circuit is approximately 300kHz and

with the snubbers absent and approximately 50kHz with the snubbers fitted. The differentiator slope below 100kHz shows a slope of 40dB/decade and a possible variation of 16dB at a given frequency due to system tolerances. This plot reveals the difficulty in providing good attenuation at low frequencies (below 100kHz) and high gain at high frequencies (above 1MHz) while using a simple differentiator circuit in an application where the variation in electrical system parameters affect the performance of the differentiator, and suggests that this scheme will perform well if the snubber components are omitted.

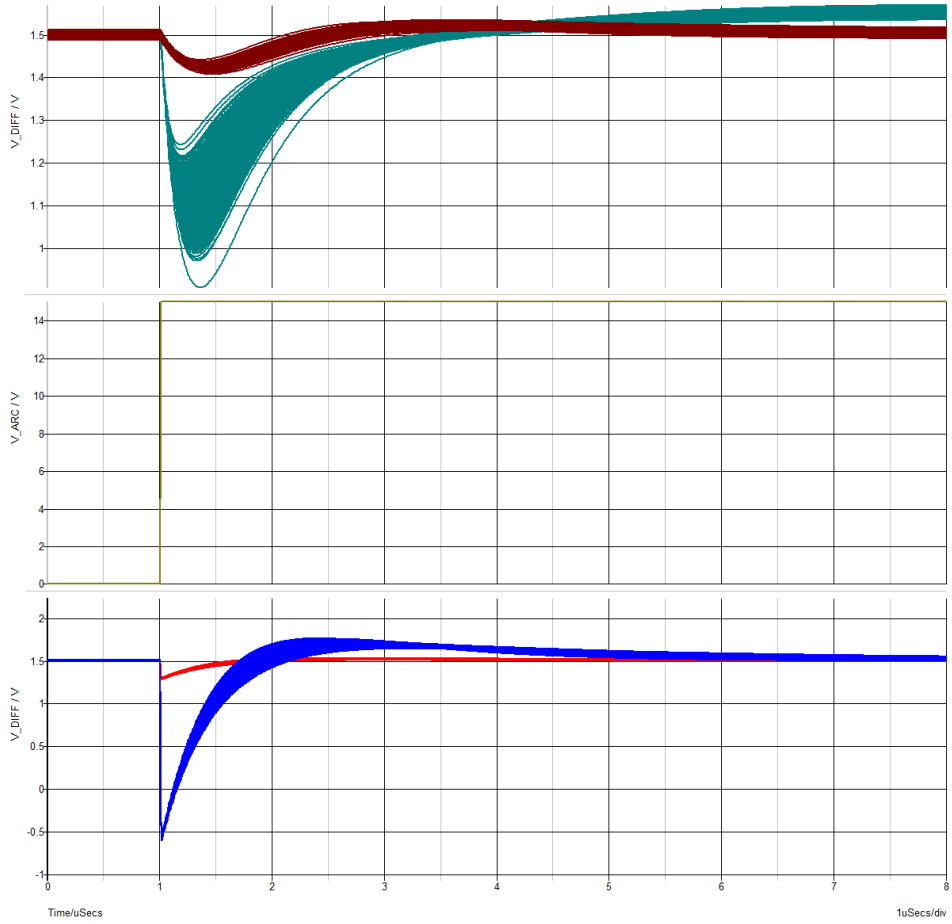


Figure 4.21: SSPC Series Arc Fault Voltage Monitor Monte Carlo Time Domain Analysis Plot (Beige = Arc Voltage, Red = 10:1 L_{up}:L_{dn} (No Snubber), Blue = 1:10 L_{up}:L_{dn} (No Snubber), Teal = 10:1 L_{up}:L_{dn} (With Snubber), Brown = 1:10 L_{up}:L_{dn} (With Snubber))

Figure 4.21 illustrates the results of four 2000 plot Monte Carlo time domain simulation runs, firstly the beige trace indicates a 0 to 15V arc voltage transient with a rise time of 10ns. The blue and red traces indicate the output voltage of the differentiator circuit where no snubber components are fitted and the upstream inductance L_{up} to downstream inductance L_{dn} split is 10:1 (50μH:5μH) and 1:10 (5μH:50μH)

respectively. The teal and brown traces indicate the output voltage of the differentiator circuit where snubber components are fitted and the upstream inductance L_{up} to downstream inductance L_{dn} split is 10:1 (50μH:5μH) and 1:10 (5μH:50μH) respectively. The first observation is that the time domain differentiator output is highly attenuated with the snubber components fitted, and a voltage threshold of 1.45V would be required to detect series arc faults where snubber components are fitted. Conversely observing the worst case scenario where no snubbers are fitted and the wire inductance ratio is 1:10 (5μH:50μH) the red plot requires a 1.25V threshold voltage compared with the predicted threshold of 1.3V determined in Equation (4.52). Finally the blue plot illustrates that without snubber devices fitted and a wire inductance ratio is 1:10 (5μH:50μH) the differentiator output voltage is -0.6V, and this drives a requirement for steering diodes across each of the resistors R_1 and R_2 in order to protect the given Analogue-to-Digital Converter (ADC) and comparator inputs. The settling time of the system following excitation is approximately 10μs, where the characterisation work in Appendix A shows that arc periods are typically greater than this value and therefore this will not impact detection performance.

The simulations provided have successfully validated the series arc fault voltage monitor against the hardware requirements, and the voltage monitor can now be included in the wider passive electrical series arc fault detection system.

4.5 Series Arc Fault Detection Software Development

Now that series arc fault detection current and voltage sensors have been developed they can be integrated into the SSPC hardware. The block diagram in Figure 4.22 shows how the outputs from the current and voltage sensors are compared to preset thresholds and four logic signals are provided to enable detection of positive and negative voltage, and positive and negative current events.

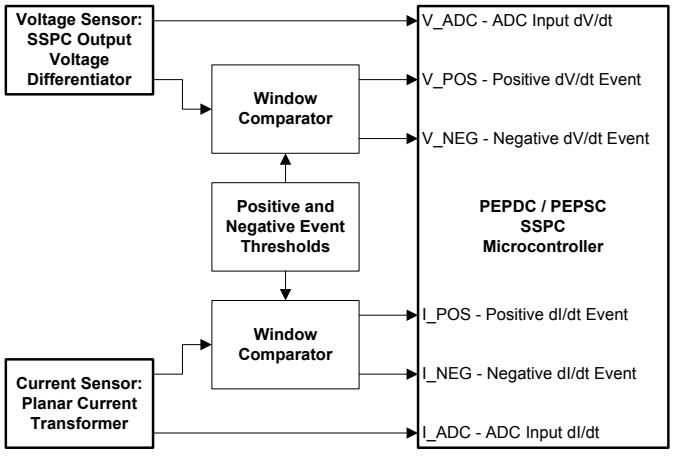


Figure 4.22: PEPDC/PEPSC Hardware Block Diagram

The outputs from the current and voltage sensors are also fed into the internal ADC on the microcontroller for built-in test purposes. This section of the document describes the SSPC microcontroller software development exercise for the proposed passive electrical series arc fault detection system.

4.5.1 Software Requirements for the Series AFD System

There are four main software requirements for the series arc fault detection system, where software requirements [**s01**] and software information statements [**s01_i**] are provided thus.

4.5.1.1 Event Capture and Confirmation

Parent Requirements: [**01**], [**04**]

[**s01**] The series arc fault detection software function **shall** be capable of capturing positive voltage, negative current events and passing them to the software confirmation function.

[**s01_i**] The positive and negative voltage and current events occur simultaneously during arc strike and when these two signals are asserted an arc fault event can be captured.

[**s02**] The series arc fault detection software function **shall** use a configurable confirmation algorithm to provide robustness against nuisance trip and detection events.

[**s02_i**] An adjustable confirmation algorithm allows the sensitivity and specificity of the series arc fault detection function to be adjusted in order to provide a method of rejecting noise signals which are not present in the provided simulation data.

4.5.1.2 Trip Status and Reporting

Parent Requirements: [**05**]

[**s03**] When arc fault detection is enabled, the series arc fault detection software function **shall** be capable of reporting series arc fault trip status to the Solid State Power Manager (SSPM).

[**s03_i**] It is important to be able to enable and disable the series arc fault detection system since it may not be required on certain loads due to safety requirements and load criticality. Series arc fault detection reporting is important in order to allow the electrical system controller to monitor health of the electrical system.

[**s04**] The series arc fault detection software function **shall** be configurable in order to either provide indication of a series arc fault, or to directly trip the SSPC.

[s04_i] Different customers have different opinions with regard to the purpose of the series arc fault detection system and have different views on reporting and tripping in response to series arc fault detection events. This requirement allows the response to series arc fault events to be set as required.

4.5.2 Software Design

4.5.2.1 Top Level Software Design

To simplify the series arc fault event detection process it was proposed to use a hardware AND gate to combine negative current and positive voltage logic events. However, during development the hardware / software interface given in Figure 4.23 was proposed since there was a risk that the negative current / positive voltage logic events may not be in phase over the full range of system operating conditions.

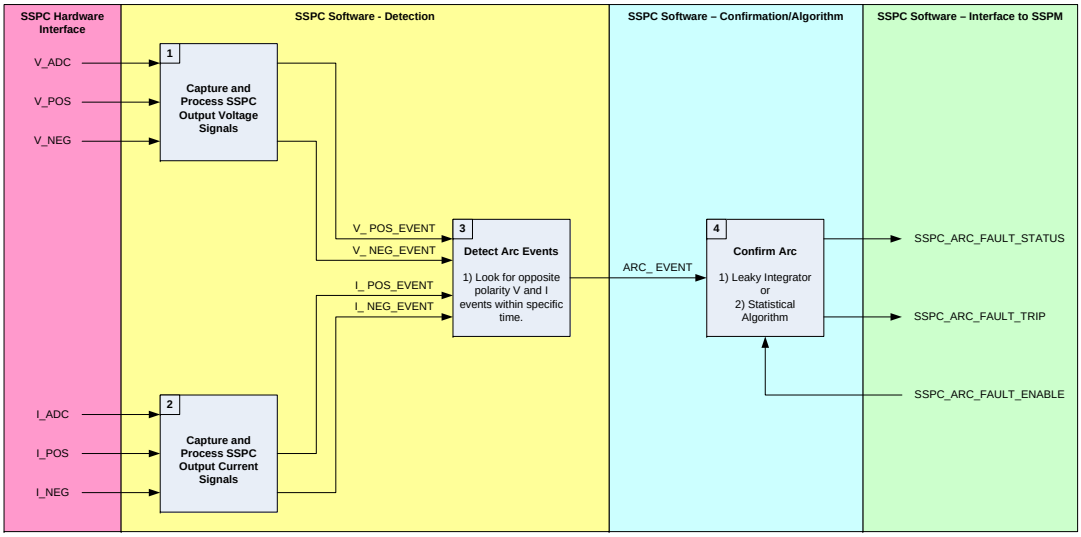


Figure 4.23: Initial PEPDC/PEPSC Hardware/Software Interface Diagram

To minimise the risk of unsynchronised negative current and positive voltage logic events it was therefore decided to feed the logic event signals into a microcontroller where a detection algorithm firstly captures edges in blocks 1 and 2 and subsequently compares arrival times in order to determine whether multiple pulses are correlated.

The captured events are then fed through to block 3 where the positive voltage / negative current and negative voltage / positive current edges are correlated, and successful events are passed as an ARC_EVENT to the confirmation algorithm. When enabled by the Solid State Power Manager (SSPM) module, the purpose of the confirmation function in Block 4 is to present SSPC_ARC_FAULT_STATUS to the SSPM and to minimise nuisance tripping by observing several arc events before making a decision to create an SSPC_ARC_FAULT_TRIP event. Confirmation in Block 4 can

take the form of a leaky integrator or a more complex statistical processing algorithm. When the discrimination of the arc fault detection hardware is sufficient to reject noise caused by the normal operation of the system and by the aerospace environment, a leaky integrator approach will suffice, whereas a statistical algorithm reduces nuisance trips by correlating a detected arc period / duration profile to a preset threshold.

4.5.2.2 Block 1,2,3: Capturing and Detecting Arc Events

In Blocks [1] and [2] events are captured by a Microchip dsPIC33FJ128GP206 [238] microcontroller using four external interrupt channels to capture the value of a free-running high resolution peripheral timer and Direct Memory Access (DMA) is used to pass event/timing data from the Interrupt Service Routine (ISR) to the main series arc fault detection function. This process is a relatively simple yet highly memory-intensive operation, which is not an issue for a dedicated microcontroller running the series arc fault detection function, but is an issue when integrating the series arc fault detection function with the wider SSPC function.

Block [3] can be characterised by Equation (4.54) which describes a simple boolean expression which was initially used to generate ARC_EVENT events.

$$ARC\_EVENT = V\_POS \cdot I\_NEG \tag{4.54}$$

$$ARC\_EVENT = V\_POS \cdot \overline{V\_NEG} \cdot I\_NEG \cdot \overline{I\_POS} \tag{4.55}$$

It was later considered that creating an expression considering all four input signals would provide the ability to reject nuisance events where more than two input signals are asserted, and Equation (4.55) describes the final boolean logic expression implemented in the microcontroller for the purpose of generating ARC_EVENT events.

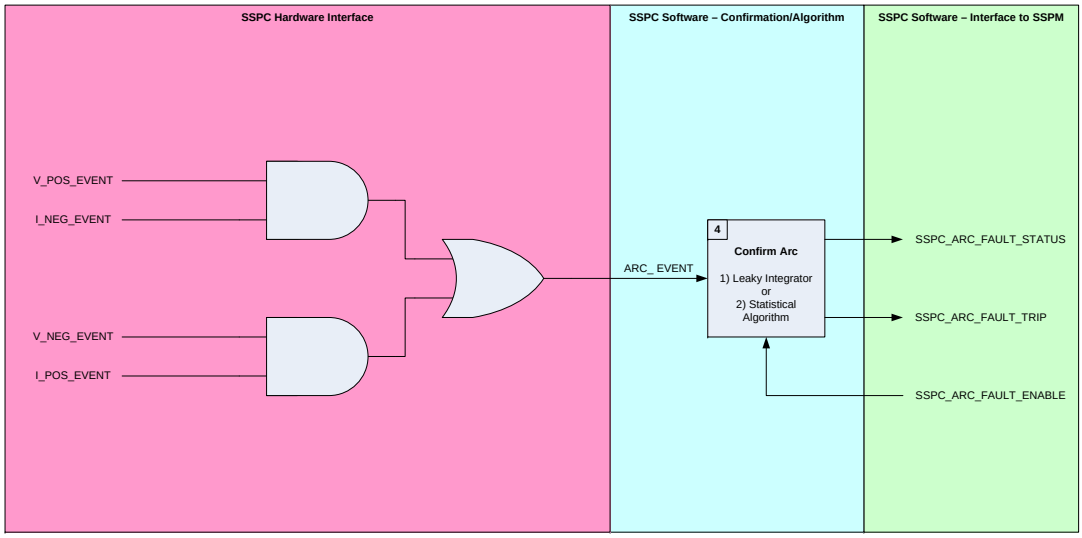


Figure 4.24: Final PEPDC/PEPSC Hardware/Software Interface Diagram

The provision of the precautionary timing analysis in Block 3 of the preliminary software design was subsequently shown to be unnecessary since both current and voltage logic signals were found to be asserted simultaneously. The hardware / software interface was then simplified by implementing the boolean detection function in hardware in accordance with Figure 4.24.

4.5.2.3 Block 4: Confirm Arc / Leaky Integrator

Block 4 provides confirmation that a series arc fault has occurred, rather than tripping on an individual arc event which could lead to nuisance trips. A leaky integrator is proposed for arc fault confirmation since it requires a number of events within a specific time to cause an SSPC trip. The leaky integrator also has memory of previous arc events and therefore intermittent series arc faults can be detected.

The discrete form of a leaky integrator takes the form of a recursive or Infinite Impulse Response (IIR) filter which is represented by the difference equation given in Equation (4.56) [239]. The difference equation can be expressed in the z-domain with Equation (4.57), and the transfer function $H(z)$ can be calculated in Equation (4.58).

$$Y[n] = (1 - k_{dec})Y[n-1] + k_{inc}X[n] \tag{4.56}$$

$$Y(z) = k_{inc}X(z) + k_{dec}z^{-1}Y(z) \tag{4.57}$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{k_{inc}z}{z - k_{dec}} \tag{4.58}$$

Equation (4.56) describes a leaky integrator difference equation which can further be visualised in Figure 4.25. Optimisation of leaky integrator algorithms is a topic which has been studied at length, and this is critical for balancing series arc fault detection sensitivity against nuisance trip rate where the focus of this chapter is to develop a sensitive series arc fault detection system.

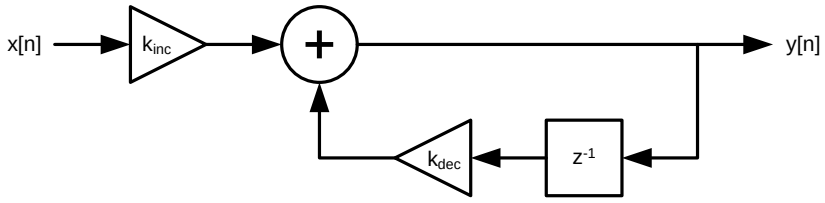


Figure 4.25: Leaky Integrator Recursive Digital System

The proposed series arc fault detection leaky integrator system is run with a sampling period of $T_s = 20\mu$s. The integrator increment constant k_{inc} is set to 1 which provides a normalised value that aids qualitative analysis of the leaky integrator algorithm. The time constant of the leaky integrator is set to $\tau = 1$s which allows arcing distributed over hundreds of milliseconds to be accumulated.

From the time constant τ the integrator decrement constant k_{dec} can be calculated with Equation (4.59).

$$k_{dec} = \frac{T_s}{\tau} = \frac{20 \times 10^{-6}}{1} = 20 \times 10^{-6} \tag{4.59}$$

Figures 4.27 and 4.26 (overleaf) illustrate the results of MATLAB® simulations which extract an arc strike signal from the data captured during the characterisation activity in Appendix A and implement the proposed leaky integrator algorithm. Figure 4.26 shows the result of loose terminal series arcing in a system with a 25A resistive and 180μF capacitive load in parallel, and here the arc behaviour is heavily affected by the interaction of the electrical and mechanical domains thus resulting in long periods between arcs as characterised in Appendix A. Since this scenario features the longest arc periods the peak leaky integrator output of 8 can be used as a threshold value giving $k_{thr} = 8$. In this scenario the series arc fault detection trip time is $t_{trip} =$ 2.49s. A practical maximum trip time of 2.5s was therefore selected such that under a majority of test scenarios the trip time falls well within this threshold, and this also limits the series arc fault energy significantly. Figure 4.27 shows the result of loose terminal series arcing in a system with a 5A resistive load where the arc behaviour is not significantly influenced by the interaction of the electrical and mechanical domains and the result here is that the leaky integrator output rises to 250 over 3s, and thus the threshold k_{thr} of 8 is met quickly giving a trip time of $t_{trip} = 135$ms. For the case where $k_{dec} << k_{thr}$ the fastest possible trip time t_{fst} assuming an arc every sampling period T_s is given by Equation (4.60).

$$t_{fst} \quad = \quad (k_{thr} + 1)T_{dec} = (8 + 1) \times 20 = 180\mu s \tag{4.60}$$

This is a passive approach to series arc fault detection so it is never possible to reduce the nuisance trip rate to zero, as discussed during the literature review in Section 2.9, and thus the author did not see any value in spending significant time further optimising the leaky integrator parameters until experimental results have been captured over the full range of system operating conditions.

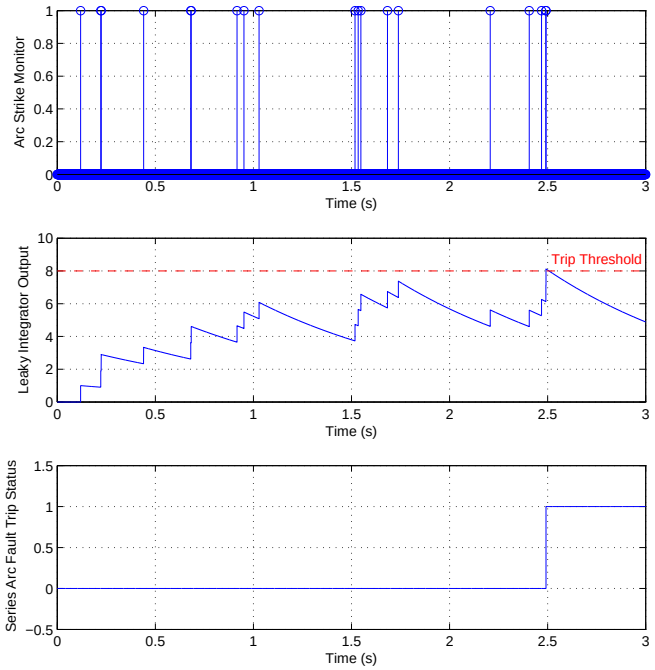


Figure 4.26: Leaky Integrator Example - 25A Resistive || 180μF Capacitive Load

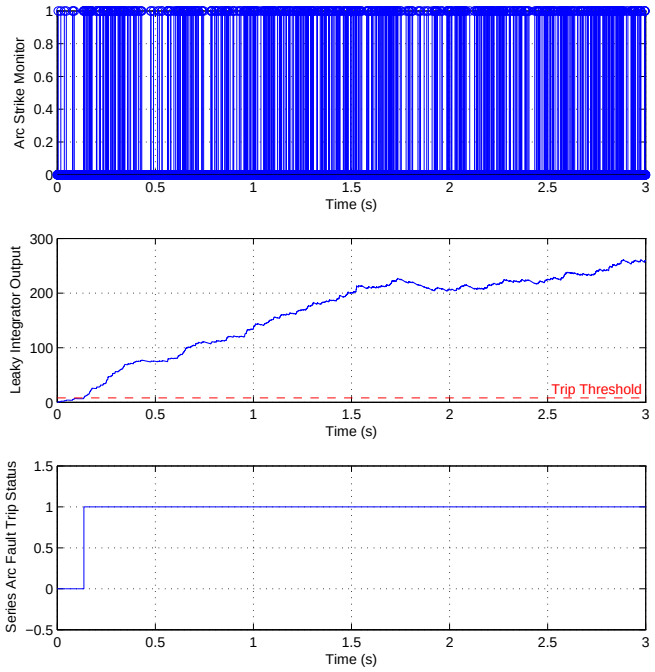


Figure 4.27: Leaky Integrator Example - 5A Resistive Load

4.5.2.4 Block 4: Alternate "Statistical" Algorithm

A novel alternative statistical arc fault confirmation algorithm for Block 4 was considered whereby a software algorithm computes arc periods by measuring the time between arc strike events, and computes arc durations by monitoring the duration between arc strike and arc quench. The measured arc periods and durations are processed into histogram and each bin in the histogram is compared against a preset window as illustrated in Figure 4.28.

This scheme may offer benefit for detecting consistent loose terminal series arc faults in fault scenarios with a well defined frequency profile. However, an experimental loose terminal series arc fault under random vibration will not exhibit the exact arc period and duration profile from one fault to the next due to the chaotic behaviour of the fault, and the interaction of the electrical and mechanical domains. Furthermore the relatively complex software algorithm illustrated in Figure 4.28 is both processor intensive, and expensive to implement and verify under RTCA DO-178C [240], therefore it was decided to first explore the limits of the simple leaky integrator.

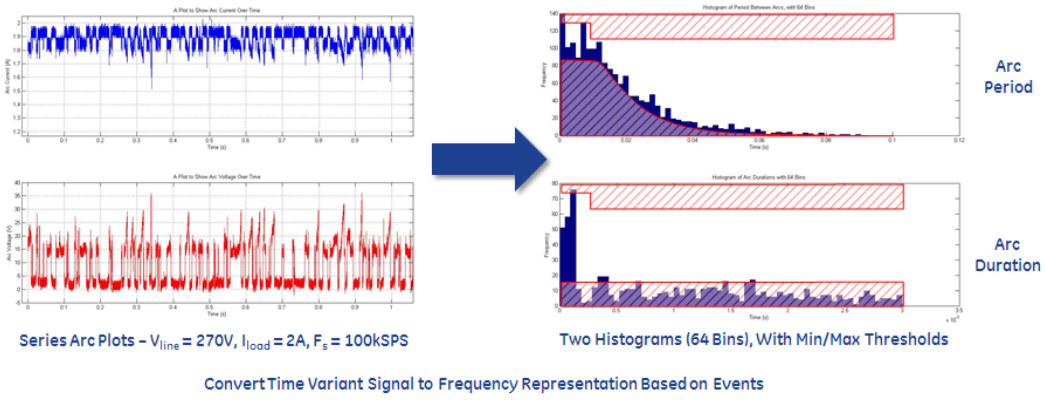


Figure 4.28: Statistical Algorithm Time to Frequency Conversion Example

4.6 Test Methodology

A loose terminal series arc fault scenario was used to verify the performance of the passive electrical series arc fault detection system developed in this chapter. The loose terminal method is identical to that used for characterisation of series arc faults in Section A.3.2. Figure 4.29 illustrates the block diagram and top level test schematic used to evaluate the performance of the series arc fault detection system.

The test schematic used here is very similar to that used during the characterisation activity, where the series arc fault detection hardware has been integrated into the SSPC under test. During this evaluation activity an HBM Genesis 16t data acqui-

sition system was used to capture performance data at 100MSPS. The logic level outputs from the series arc fault voltage and current monitors were captured, along with SSPC output voltage $V_{sspcout}$ and SSPC loop current I_{loop}. SSPC output voltage was measured using a differential voltage probe and SSPC loop current was measured using a Hall effect current probe. Capturing and processing SSPC output voltage and SSPC loop current in MATLAB® allowed the series arc events to be identified.

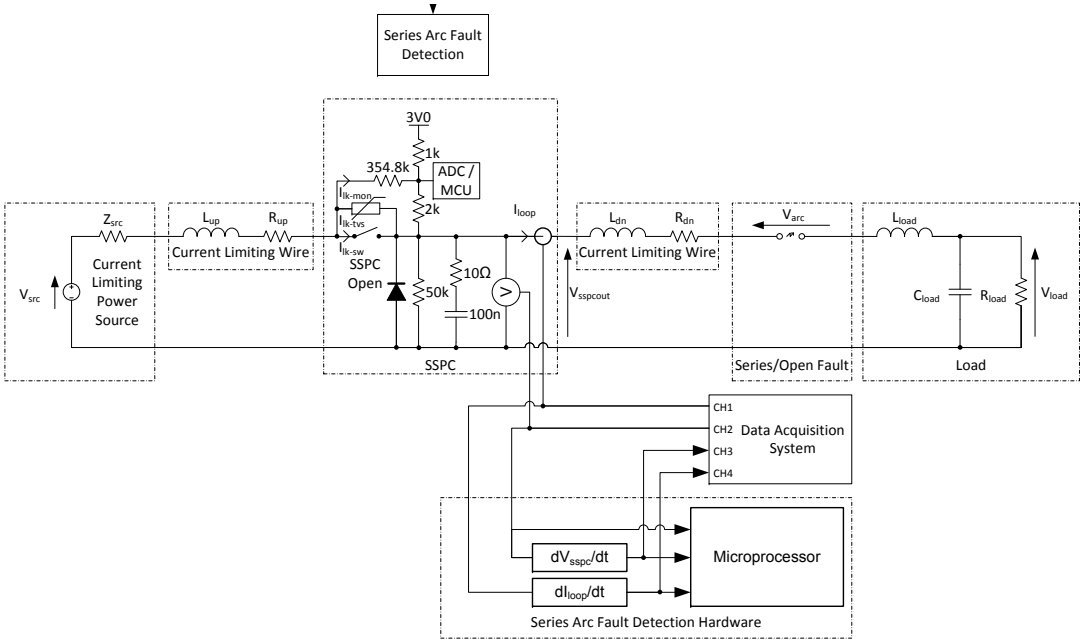


Figure 4.29: Experimental Test Schematic / Block Diagram for Verification of the Series Arc Fault Detection System

Perhaps the easiest method for identifying an arc strike event is to monitor the arc voltage V_{arc} as per the characterisation activity. However, it was found during the modelling activity in Section 3.6.2 that the isolated differential voltage probe used to measure arc voltage presented a small but significant capacitance across the arc electrodes which affected the high frequency behaviour of the arc, and this is a particular issue as arc current tends to zero. The probe also tended to excite resonant arc voltage behaviour in the low MHz region which could compromise the validity of the test results. To prevent parasitic capacitance in the differential voltage probe from skewing the series arc fault detection performance results, arc strike events were identified from the loop current I_{loop} waveforms using the MATLAB® feature extraction scripts.

Three seconds of electrical series arc fault detection data was captured for each combination of loads in Table 4.2. It should be noted that although the SSPC under test is rated at 120A the series arc fault detection system was not tested with resistive load current levels above 25A due to the spot welding issue encountered during Appendix

A. Higher vibration levels would be required in order to simulate series arcing of the loose terminal above this current level.

Parameter	**Minimum Value**	**Maximum Value**
$R_{load}(I_{loop})$	10.8Ω (25A)	270Ω (1A)
L_{up}	75μH	175μH
$L_{dn} + L_{load}$	23μH	123μH
C_{load}	0μF	380μF

Table 4.2: Series Arc Fault Detection Test Parameters

By capturing and comparing the logic level outputs from the series arc fault voltage and current monitors against the SSPC output voltage and SSPC loop current respectively, the success rate of the series arc fault detection system was evaluated for the each of the specified load and cable configurations.

Figure 4.30 shows 30ms sample of an example MATLAB® plot used to visually communicate the verification methodology. This example test was chosen because the high downstream wiring inductance $L_{dn} = 123\mu$H resulted in a slow rate of change of current, and a low peak SSPC output voltage. The loop current waveform shows three separate arc events which strike at 361.5ms, 369.4ms and 379ms respectively. A backward difference derivative was used to monitor for step changes in loop current from the Hall effect current probe, and changes above a preset threshold are displayed on the corresponding arc strike monitor trace. Figure 4.30 shows that AFDIDISC0 (Negative $\frac{dI_{loop}}{dt}$ Event) and AFDVDISC0 (Positive $\frac{dV_{sspcout}}{dt}$ Event) were asserted during the first and third arc strike but not during the second arc strike. Two series arc events were therefore successfully detected and one was missed. The AFDVDISC0 (Positive $\frac{dV_{sspcout}}{dt}$ Event) signal showed that there was voltage noise on the SSPC output, and this was found to occur due to high frequency noise from the lab power supply used for these experiments, where similar noise is likely to appear in a realistic aircraft application.

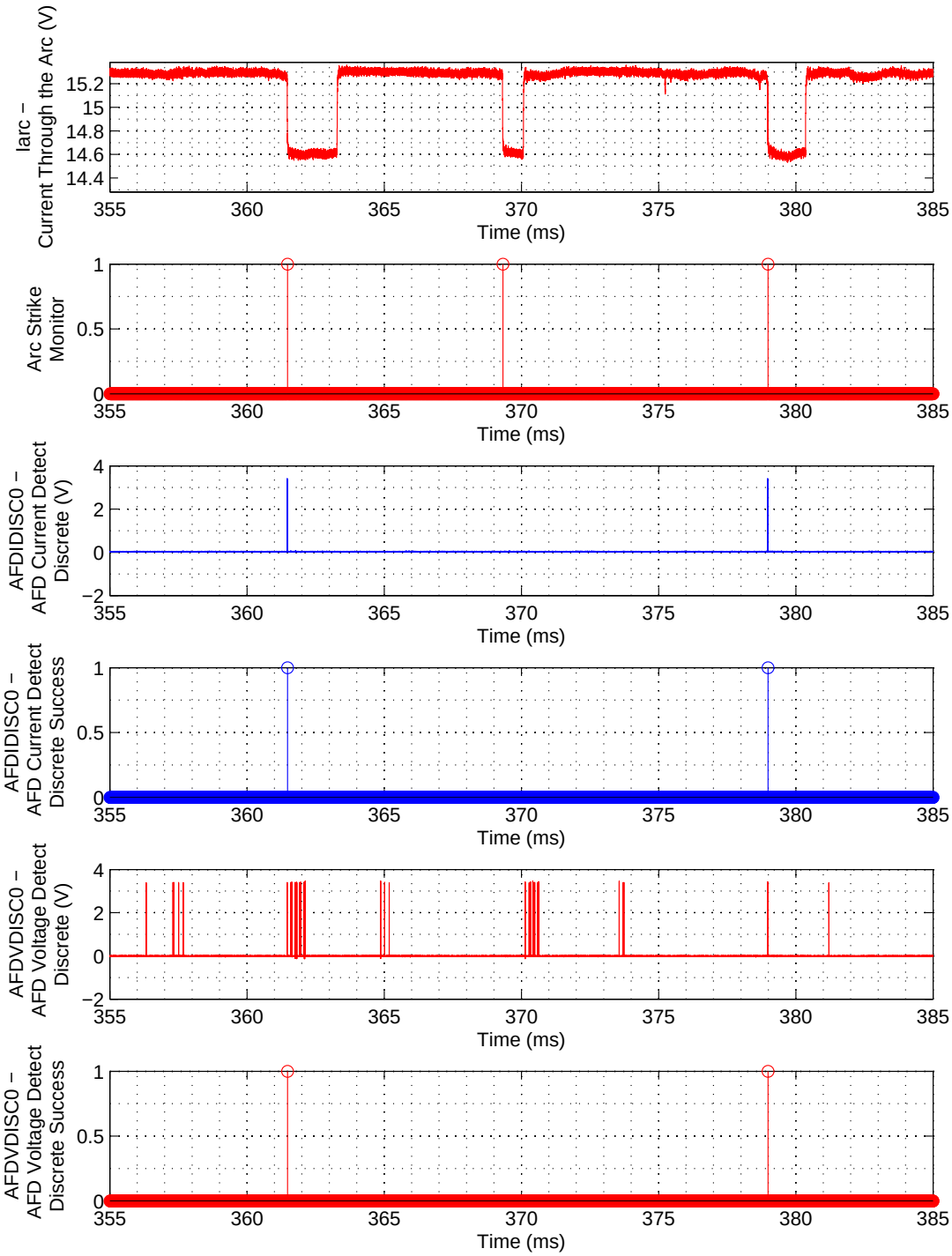


Figure 4.30: A Plot Showing the Method of Evaluating Series Arc Fault Current and Voltage Sensor Performance (15A Resistive Load / 123μH Downstream Inductance)

4.7 Results

The results in Sections 4.7.1, 4.7.2, and 4.7.3 show the ratio of successful current / voltage detection events to the total number of series arc events as a percentage, for each test scenario in Table 4.2, thus providing a map of the series arc fault detection performance. The series arc events are extracted from the current waveforms, as illustrated in Figure 4.30, and fed into the leaky integrator algorithm described in Section 4.5.2.3, where the resulting trip times are presented in Section 4.7.4.

4.7.1 Series AFD Performance vs Resistive Load Current

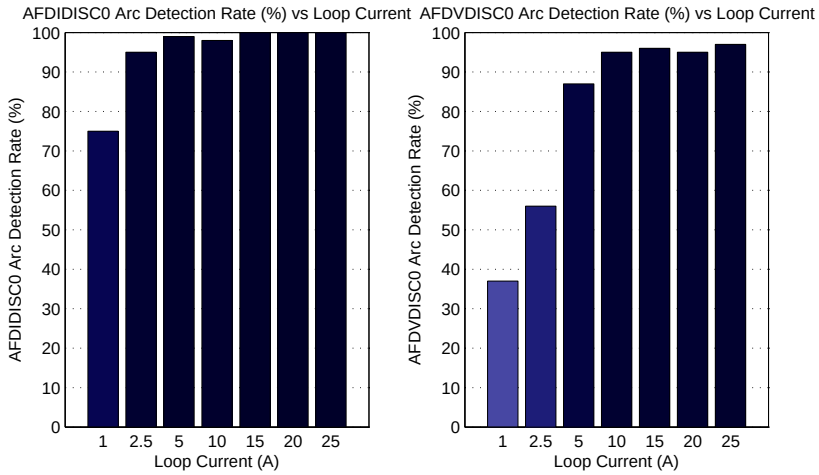


Figure 4.31: Series Arc Detection Rate vs Resistive Load Current

4.7.2 Series AFD Performance vs Resistive / Capacitive Load

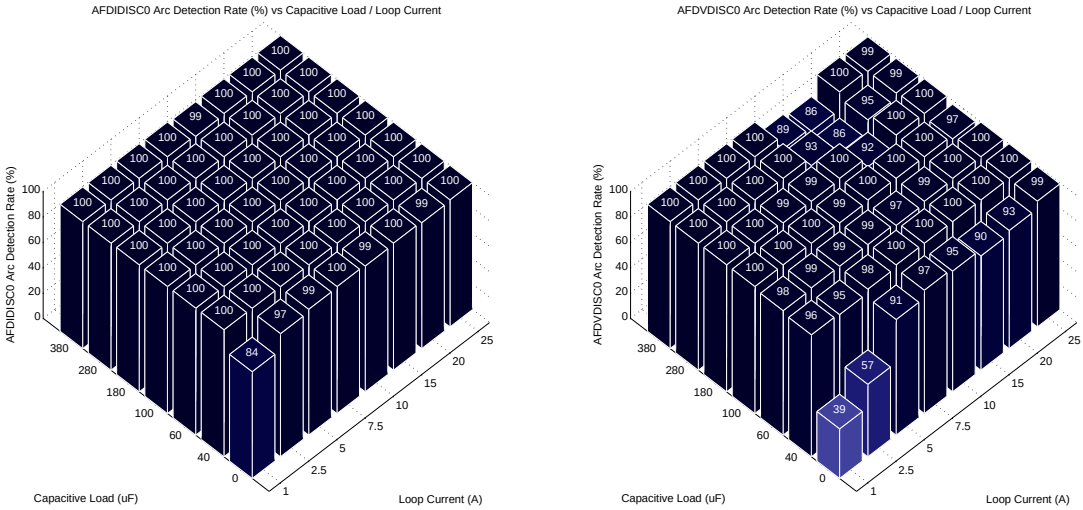


Figure 4.32: Series Arc Detection Rate vs Load Capacitance / Current

4.7.3 Series AFD Performance vs Resistive Load/System Inductance

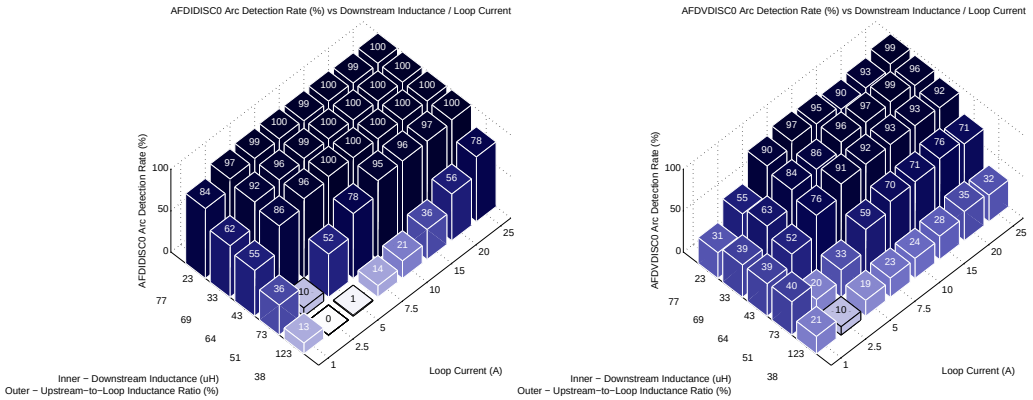


Figure 4.33: Series Arc Detection Rate vs Downstream Cable Inductance / Current

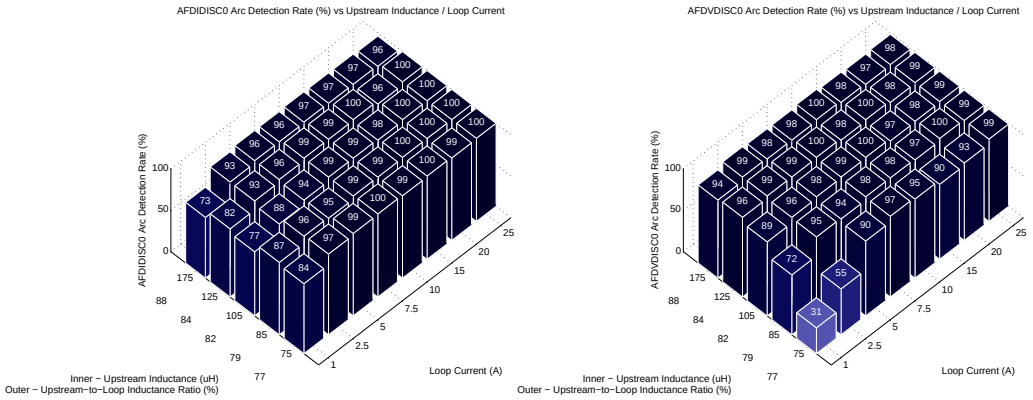


Figure 4.34: Series Arc Detection Rate vs Upstream Cable Inductance / Current

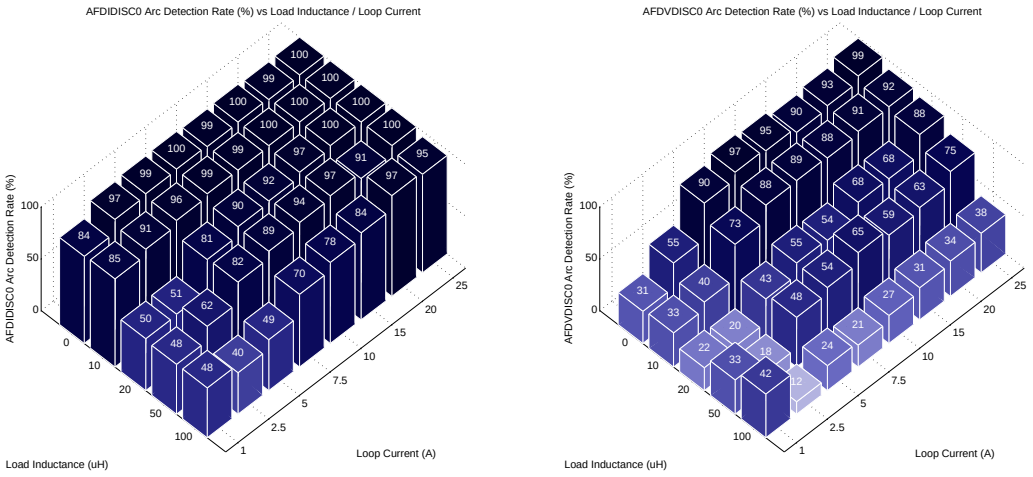


Figure 4.35: Series Arc Detection Rate vs Load Inductance / Current

4.7.4 Leaky Integrator Trip Time vs Resistive Load Current

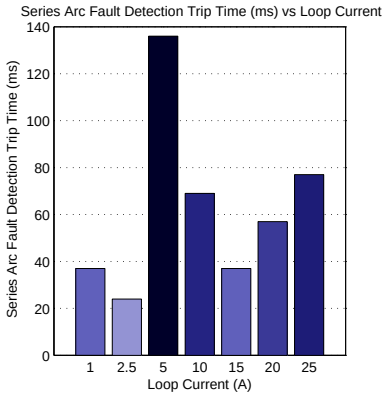


Figure 4.36: Series Arc Trip Time vs Resistive Load Current

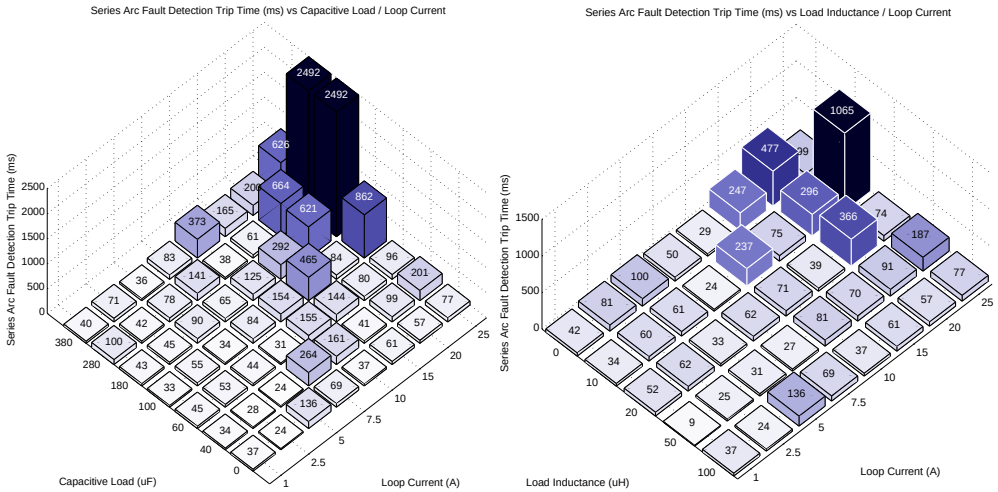


Figure 4.37: Series Arc Trip Time vs Load Inductance and Capacitance / Current

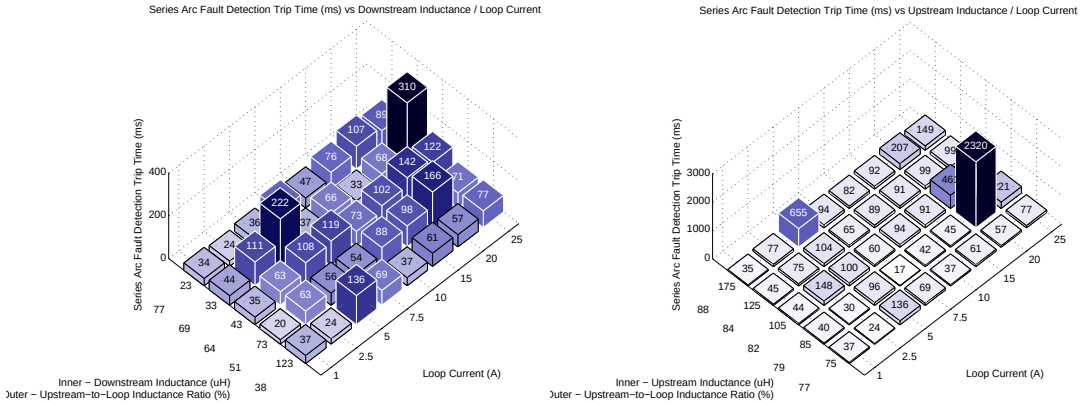


Figure 4.38: Series Arc Trip Time vs Up and Downstream Cable Inductance / Current

4.8 Discussion

The discussion section for this chapter is focussed on characterising the passive series arc fault detection system implemented in the exemplary PEPDC unit, and verifying functional operation and performance against the top level system requirements for the voltage invariant passive electrical series arc fault detection system outlined in Section 4.2.

4.8.1 Series AFD Resistive Load Detection Performance

Requirement: **[01]** Detect series arcs on loads current in the range 5A through 120A.

The results of the resistive load analysis in Figure 4.31 show that the series arc fault current monitor detects ≥95% of series arcs for currents over 5A. The series arc fault voltage monitor detects 85% of series arcs for currents over 5A. The detection hardware therefore meets the requirement for detection on load currents above 5A.

Theoretically the SSPC output voltage peak which occurs during arc strike should be both line voltage invariant and load current invariant, however, this assumes that there is minimal capacitance between the SSPC output and chassis. When the SSPC is closed, both the input and output snubbers appear in parallel at the SSPC, and it is proposed that the reduced series arc fault voltage detection rate occurs because the SSPC input/output snubbers reduce the voltage peak at the SSPC output, thus reducing the sensitivity of the voltage monitor circuit. The series arc fault voltage monitor detection rate remains above 85% for resistive load currents above 5A and therefore the sensor performs adequately.

It is expected that the PEPDC system would achieve similar detection rates to those reported for the load current range 25A to 120A but currents above 25A caused the loose terminal to become spot welded preventing effective characterisation.

The results of the resistive load tests illustrated in Figure 4.36 show that trip times range between 25ms for the 2.5A test scenario and 135ms for the 5A test scenario. The spread of trip times illustrates the significant variation between successive loose terminal series arc fault test runs. All trip times are within the goal of 2.5s and therefore the detection hardware functions satisfactorily for resistive load scenarios.

4.8.2 Series AFD Resistive/Capacitive Load Detection Performance

Requirement: **[02]** Detect series arcs with load capacitances of 0 through 380μF.

The results of the resistive / capacitive load analysis in Figure 4.32 show that the detection rate of the series arc fault current monitor for load capacitances up to 380μF and load currents ≥5A is ≥99%. Capacitive loads induce instability which

allows arcs to quench more readily thus ensuring that the series arc fault detection current monitor has a signal sufficient to detect a majority of arc strike events.

The detection rate of the series arc fault voltage monitor for capacitances $\geq 40\mu$F and currents $\geq$1A is $\geq$85%. An interesting phenomena for load capacitances $\geq 180\mu$F and currents between 10A and 15A is a reduction in series arc fault voltage monitor success rate due to more stable loop current behaviour, and thus a reduction in the severity of the corresponding SSPC output voltage behaviour. This result further proves the conclusion from the series arc fault characterisation activity in Section A.5, which hypothesises that even a modest load capacitance allows series arc faults in 270VDC systems to be quenched, thus making them more detectable.

The results of the resistive / capacitive load tests illustrated in Figure 4.37 show that trip times range between 24ms for the 2.5A / 0μF test scenario and 2.492s for the 25A / 280μF test scenario. The results also show that high load currents and highly capacitive loads result in relatively long trip times. All trip times are within the goal of 2.5s and therefore the detection hardware functions satisfactorily for resistive / capacitive load scenarios.

4.8.3 Series AFD Resistive/Inductive Load Detection Performance

Requirement: **[02]** Detect series arcs with inductive loads of 0 through 100μH.

The results of the resistive / inductive load analysis in Figure 4.35 show that the series arc fault current monitor detection rate decreases with increased load inductance since additional inductance slows down the falling edge of the current waveform during arc strike. For SSPC loop currents $\geq$5A and load inductances $\leq 50\mu$H, the current monitor detection rate is $\geq$81%, representing an acceptable detection rate. At currents $<$5A and inductances $>50\mu$H the current monitor success rate falls as low as 40%, where lower currents and higher load inductances would reduce this further.

In contrast to the excellent current monitor detection performance, the series arc fault voltage monitor performance is less impressive. For SSPC loop currents $\geq$5A and load inductances $\leq 50\mu$H the voltage detection success rate is $\geq$43%. While this is still a sufficient number of events to positively identify a series arc event, the leaky integrator threshold may need to be reduced, thus increasing the probability of nuisance trips. Increasing the load inductance to 100μH results in a 24% voltage detection success rate at 5A and this may be insufficient for reliable detection depending on the arc period distribution. An interesting observation is that for load currents in the order of 1A, where there is insufficient current to maintain an arc following arc strike, the quenching arc results in an easily detectable signal, which in this scenario arcs can be detected in the presence of higher load inductances.

The results of the resistive / inductive load tests illustrated in Figure 4.37 show that trip times range between 9ms for the 1A / 50μH test scenario and 1.065s for the 25A / 10μH test scenario. The spread of these results again illustrates how there is significant variation between successive loose terminal series arc fault test runs, and how higher current series arc faults result in longer detection times. All trip times are well within the goal of 2.5s and therefore the detection hardware functions satisfactorily for resistive/inductive load scenarios.

4.8.4 Series AFD Upstream/Total Loop Inductance Ratio and Resistive Load Detection Performance

Requirement: **[03]** Detecting series arcs where the minimum SSPC upstream wiring inductance to total loop inductance ratio is $\geq$10%.

To vary the upstream wiring inductance to total loop inductance ratio, varying levels of downstream inductance were introduced, thus increasing the total loop inductance. Figure 4.33 references both the downstream inductance value and the upstream wiring inductance to total loop inductance ratio as a percentage. The results of the downstream inductance analysis given in Figure 4.33 show that the success rate of the series arc fault current monitor decreases with increased downstream inductance since the additional inductance slows down the falling edge of the current waveform during arc strike events. The ratio of upstream wiring inductance to total loop inductance ratio does not affect current monitor performance, it is the way that the ratio is modified by adding downstream inductance. For SSPC loop currents $\geq$5A and downstream inductances $\leq$73μH (an increase of +50μH from the baseline downstream inductance) the current monitor success rate is $\geq$52%, representing an acceptable detection rate. At currents <5A and inductances >73μH, the current monitor success rate falls as low as 0% and therefore downstream inductance is a key parameter to manage in electrical power distribution systems requiring series arc fault detection.

The series arc fault voltage monitor performance is marginally worse than that of the current monitor under decreased upstream wiring inductance to total loop inductance ratio conditions. For SSPC loop currents $\geq$5A and downstream inductances $\leq$73μH (51% up:total ratio) the voltage detection success rate is $\geq$33%. This is still a sufficient number of events to positively identify a series arc event, however, this may require the leaky integrator threshold to be reduced, thus increasing the probability of nuisance trips. Increasing the downstream inductance to 123μH (38% up:total ratio) representing an upstream-to-total inductance ratio of 38% results in a 19% voltage detection success rate at 5A and this may be sufficient for reliable detection depending on the arc period distribution. This result implies that satisfying the worst case 1:10 upstream-to-total inductance ratio from requirement [03] is not easily achievable without removing or switching out the SSPC input/output snubbers, thus providing

a higher SSPC output voltage signal to detect.

The results of the downstream inductance tests illustrated in Figure 4.38 show that trip times range between 24ms for the 2.5A / 23μH test scenario and 310ms for the 25A / 33μH test scenario. Yet again the spread of these results illustrates how there is significant variation between successive loose terminal series arc fault test runs. All trip times are well within the goal of 2.5s and therefore the detection hardware functions satisfactorily for resistive load / high downstream inductance scenarios.

The results of the upstream inductance analysis given in Figure 4.34 show that the success rate of the series arc fault current monitor remains broadly consistent with increased upstream inductance. For SSPC loop currents $\geq$5A and upstream inductances $\leq$175μH (88% up:total ratio) the current monitor success rate is $\geq$94% thus representing an excellent detection rate. At currents $\geq$1A and inductances $\leq$175μH the current monitor success rate falls as low as 73% which still represents a very good detection rate.

The series arc fault voltage monitor performance is comparable to that of the current monitor under increased upstream inductance conditions. For SSPC loop currents $\geq$5A and upstream inductances $\geq$75μH the voltage detection success rate is $\geq$90%. This success rate is excellent and allows detection of the majority of arc events. Reducing loop current to 2.5A reduces the minimum voltage detection rate to 55%, which still allows for successful arc strike detection.

The results of the upstream inductance tests illustrated in Figure 4.38 show that trip times range between 24ms for the 2.5A / 75μH test scenario and 2.320s for the 20A / 85μH test scenario. Again increased resistive load currents correlate with increased trip times due to the interaction of the electrical and mechanical domains. All trip times are well within the goal of 2.5s with the exception of the 20A / 85μH case which has a trip time of 2.32s, and therefore the detection hardware functions satisfactorily for resistive load / high upstream inductance scenarios.

4.8.5 Further Observations

Requirement: **[04]** Detect series arc faults in 28VDC and 270VDC systems.

Characterisation of series arc fault detection performance for this thesis prioritised the 270VDC system since the earlier studies in Section A.5 demonstrated it to be more difficult. Furthermore 270VDC detection for the PEPDC and PEPSC projects was one of the main thesis objectives. Further characterisation work will be required in the future to confirm this expectation based on evidence from this study.

Requirement: [**05**] Trip or report in response to a series arc fault.

The test software implemented on the PEPDC hardware was configured to provide indication of a series arc fault without tripping in order to allow repetitive detection tests to be carried out.

Requirement: [**06**] Do not trip due to crosstalk.

The crosstalk test was out of scope for this thesis and this is recommended for future work. Further work is also required to define a crosstalk test requirement for arc fault detection systems, which complements standard EMC test practices.

Requirement: [**07**] Provide series arc fault detection for multiple SSPCs

The requirement to apply the series arc fault detection system to each SSPC output was met by design since the engineering solution can be discretely applied to each switched output in a given solid state electrical power distribution system. The total mass of the series arc fault detection solution is in the order of 10g which represents an increase in SSPC mass of around 2%. This has negligible impact in a primary power distribution system since there are a limited number of switched outputs. However, for secondary power distribution systems where there are hundreds of switched outputs with lower current ratings, the mass increase is more significant and a more optimised solution may be required.

Requirement: [**08**] Use existing SSPC current and voltage measurement. [**09**] Minimise additional hardware. [**10**] -40 to +100°C operating temperature, [**11**] Minimise power dissipation.

Unfortunately it was not possible to reuse the existing SSPC current and voltage monitors for series arc fault detection purposes. This inherently drove additional material cost into the engineering solution. This was minimised by implementing a PCB-based current sensor and using only a few additional passive components and operational amplifiers. Maintaining a simple bill of materials also allowed thermal dissipation to be minimised to 80mW which is well within the 100mW budget, and the parts used are capable of operation between -55°C to +125°C, thus easily allowing operation in ambient temperatures up to +100°C. Further integration work is required to determine the effect of this dissipation on a power distribution unit featuring multiple SSPC modules.

Requirement: [**12**], [**13**], [**14**], [**15**], [**16**], [**17**] EMC and EPV test requirements.

The EMC / EPV results are not presented in the results section of this chapter since they are out of scope for the thesis. The series arc fault detection system did not nuisance trip under the radiated and conducted susceptibility testing in accordance with RTCA DO-160G Section 19 Cat Y. The series arc fault detection system and

SSPC also passed the emissions requirement in RTCA DO-160G Section 21 Cat L. The series arc fault detection system was also tested in accordance with RTCA DO-160G Section 16 Cat D for 270VDC systems and no nuisance trips were encountered.

Audio frequency conducted susceptibility and induced signal susceptibility should be carried out in the future work. Lightning induced transient susceptibility was not explicitly tested, however the SSPC was subjected to repetitive switching at 270VDC with a 120A load and 50μH of downstream inductance which is similar to a single-strike lightning test and no nuisance trips were observed.

4.9 Chapter Summary

The aim of this chapter was to develop and evaluate a voltage invariant passive electrical series arc fault detection system for deployment in aerospace SSPCs. The existing SSPC current monitor was not suitable for use in a series arc fault detection application due to insufficient dynamic range of the measurement system. Furthermore the existing SSPC voltage monitor was not suitable for the series arc fault detection application due to a conservative 50kHz sampling rate which is insufficient to capture short duration SSPC output voltage transients.

A series arc fault detection current monitor trade study was carried out to identify available current monitoring technologies and a Rogowski coil approach was selected. A novel multi-layer planar current transformer solution was developed for the PEPDC and PEPSC SSPC PCBs. A PEEC model was developed to qualitatively understand the circuit level behaviour of the Rogowski coil structure. The mutual inductance of the proposed solution was calculated and experimentally verified in the time domain. The PEPDC and PEPSC planar current transformer structures were evaluated in the frequency domain where resonant behaviour of the coils was analysed to understand the performance limitations.

The current and voltage monitor systems were integrated into the PEPDC and PEPSC SSPC modules. Significant circuit simulation and analysis was completed since the prototype PEPDC and PEPSC SSPC assemblies are highly complex. The detection performance of the current and voltage monitors was successfully demonstrated for a range of resistive, capacitive and inductive loads.

A software series arc fault detection / confirmation algorithm was developed. Two possible algorithms were considered in this chapter, a simple IIR leaky integrator and a statistical algorithm based on the arc period / duration profile. The leaky integrator was selected as the most appropriate solution and was tested under the loose terminal series arc fault scenario over the full range of electrical conditions. The leaky integrator parameters were optimised and experimentally demonstrated to detect arcs within 2.5s under each system permutation.

Chapter 5

Development and Evaluation of an Arc Fault Perturbation / Confirmation and Initiated Built-In Test (IBIT) Scheme

5.1 Introduction

5.1.1 Background

Strobl and Meckler have published papers describing the electrical behaviour of drawn electric arcs in aircraft DC power networks, and the effect of inductive and capacitive loads on arc faults in aircraft AC power networks [80; 68]. Passive electrical arc fault detection systems which use current and voltage behaviour are common, with many patents in existence [241]. There are also a number of current waveform analysis techniques that have been proposed, using Short Time Fourier Transform (STFT) [145] and wavelet analysis [148; 150] techniques. Kim presents an analysis which observes electromagnetic radiation created as a result of a similar drawn arc scenario [133]. Again there are many patents which cover the use of electromagnetic arc characteristic for arc fault detection [130]. The common feature in these papers is the use of a passive detection scheme, where the arc fault detector "listens" to the system in an attempt to "hear" an arc fault. The detection scheme does not know specifically when the arc fault is going to occur, and therefore must listen to the system continuously. Steps are taken to minimise interference from the environment and electrical load suppliers should comply with strict EMC regulations to prevent such interference from propagating to a given arc fault detection system. However, the aircraft electrical power distribution system has to endure a harsh electromagnetic environment, and therefore continual monitoring for arc faults can lead to nuisance trips. Further to the successful demonstration of a passive electrical series arc fault

detection system in Chapter 4 there is a need to investigate a series arc fault detection scheme which is more robust against nuisance trips.

There are a number of active arc fault and wire fault detection schemes which function on a stimulus / response basis, therefore reducing the occurrence of nuisance trips. These schemes typically use travelling wave techniques such as Time Domain Reflectometry (TDR), Sequence Time Domain Reflectometry (STDR), Frequency Domain Reflectometry (FDR), Standing Wave Reflectometry (SWR), Spread Spectrum Time Domain Reflectometry (SSTDR), Low Energy High Voltage (LEHV) and combinations thereof [183; 187; 242]. These techniques are capable of detecting and locating impedance discontinuity events, but do not explicitly use specific arc fault characteristics to categorise the type of fault beyond open or short circuit. Parkey et al propose combining SSTDR, LEHV, TDR and a Digital Multimeter (DMM) in order to detect and characterise arc faults [243]. To implement this scheme the aircraft solid state electrical power distribution system scenario would require a number of expensive ASIC / FPGA devices to be added to each switched output, which would result in an expensive arc fault detection solution, and thus a simple and more cost effective solution is required.

The switching time for a typical 270VDC capable electromechanical contactor, such as the Tyco LEV200, is 47ms to close (including contact bounce) and 12ms to release [244]. The switching times for the PEPDC and PEPSC SSPCs are in the order of 1μs for both close and release, with a command latency time of approximately 20μs. The comparatively fast switching of the SSPC technology provides the opportunity to use switch current modulation for the purposes of fault detection and diagnostics. Nemir et al demonstrated an arc fault management system which continuously monitored the switch output current waveform for arc faults, where on successful detection of an arc the switch was opened in order to quench the arc, and the switch was then reclosed after a predetermined delay [65]. This technique was used to minimise the damage caused by arc faults in electrical systems. The first focus of this chapter is therefore active SSPC state modulation for the purpose of series arc fault detection.

In contrast to electromechanical circuit breakers and relays, SSPCs pass a small leakage current when they are in the open state. This phenomena is typically undesirable since leakage current can result in phantom voltages which appear at disconnected SSPC outputs. The second focus of this chapter is therefore to investigate the interaction of SSPC leakage currents with series arc faults.

To further reduce the occurrence of nuisance trips there is an opportunity to apply Built-In Test (BIT) methodologies. The PEPDC and PEPSC SSPC designs contain an Initiated Built-In Test (IBIT) function which is used to test the turn on, turn off and current limit functionality for each MOSFET device, along with transient

suppressor status in a multi-semiconductor SSPC in accordance with the patents of Tyler and Collins [245; 246; 247; 248; 249; 250; 251; 252]. The IBIT scheme features a semiconductor switch between the SSPC output and chassis which short circuits the SSPC load and allows large currents with fast dI/dt characteristics to be generated on request by opening and closing the SSPC. It is proposed that this artificially generated test signal can be used to verify on request that the passive electrical series arc fault detection system hardware dI/dt and dV/dt sensors developed in Chapter 4 are healthy. This scheme has the potential to identify manufacturing and installation errors during the installation of a given solid state power distribution panel, thus improving sensitivity and robustness of the series arc fault detection system against nuisance trips.

5.1.2 Hypotheses

The hypothesis underpinning the arc fault perturbation experiment is that if the SSPC state is modulated during a high voltage DC series arc fault, the system loop current and SSPC output voltage will exhibit unique behaviour which can be used to confirm that an arc fault is present in the system.

The hypothesis for the arc fault confirmation experiment is that when the SSPC is in the open state, the SSPC output leakage voltage derived from the SSPC switching semiconductor leakage current is modulated by downstream series wire faults and this modulation can be used to confirm that a series wire fault is present in a given system.

The hypothesis for the Initiated Built-In Test (IBIT) experiment is that by artificially stimulating loop current and SSPC output voltage during installation of a given solid state power distribution panel, the health of the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ detection hardware, and thus the functionality of the arc fault detection system can be verified.

5.1.3 Aims and Objectives

The aims of this chapter are firstly to determine whether turning off the SSPC during a series arc fault and monitoring arc quenching behaviour in the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ can be used as a method of detecting or confirming the presence of series arc faults in high voltage DC systems. The secondary aim of this chapter is to demonstrate whether undesirable SSPC leakage current can be used as a method of detecting series wire faults. The tertiary aim of this chapter is to demonstrate whether artificial stimulation of the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ can be used as a method of Initiated Built-In Test (IBIT) during the installation of the solid state power distribution panel into an aircraft platform and as part of regular maintenance and fault finding activities.

This chapter is split into three main sections addressing each of the three aims respectively, where the first Section 5.2 covers the arc fault perturbation and confirmation scheme. The first objective in this section is to determine the theory behind the series arc fault perturbation scheme, the second objective is to back up the theoretical analysis with a simulation of the series arc fault perturbation scheme using the model developed in Section 3.4, and the final objective is to demonstrate this scheme in physical hardware.

Section 5.3 addresses SSPC leakage behaviour in the SSPC open state, where the first objective is to determine the theoretical interaction between SSPC leakage current and series wire faults, and the second objective is to demonstrate the SSPC leakage-based series arc fault confirmation scheme on physical hardware.

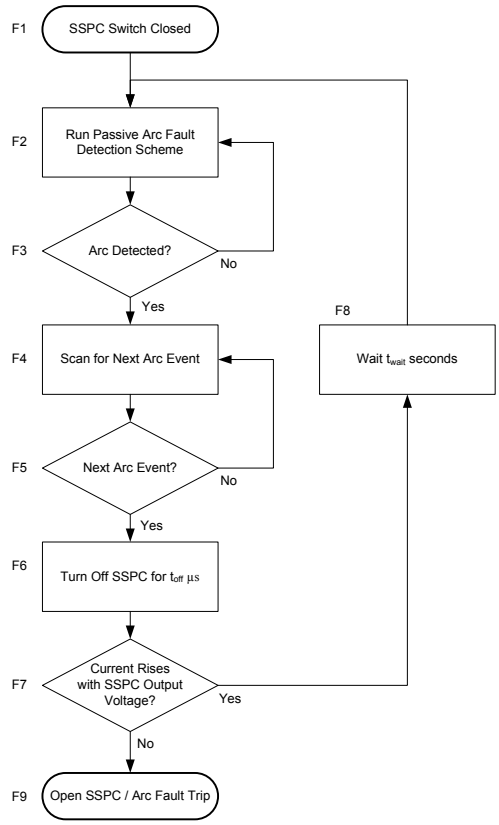
Section 5.4 of this chapter explores the Initiated Built-In Test (IBIT) Scheme, where the first objective is to identify the relevant theory behind the scheme, the second objective is to model the IBIT scheme using the model developed in Section 3.4, and the final objective is to further demonstrate the BIT scheme using physical hardware.

5.2 Arc Fault Perturbation / Confirmation Scheme

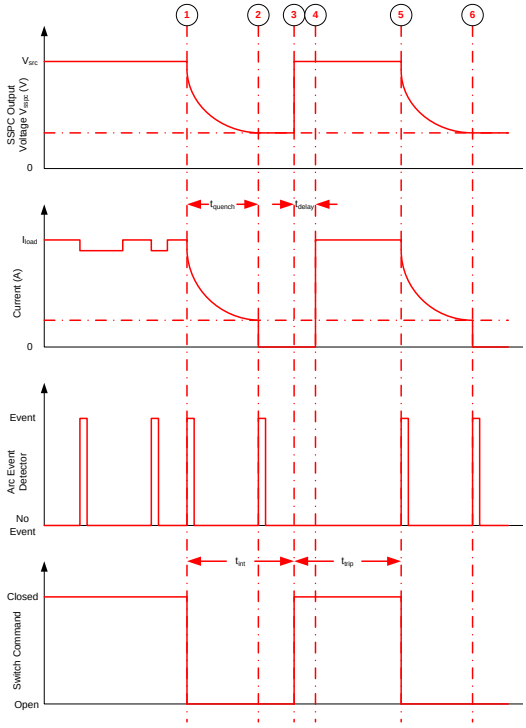
5.2.1 Theory and Predictions

In this experiment the SSPC is configured to interrupt the load current immediately after series arc strike, thus perturbing and confirming the series arc condition as illustrated in the flowchart given in Figure 5.1. The PEPDC SSPC used in this investigation is capable of 270VDC operation with steady state currents up to 120A, and is capable of opening and closing in less than 1μs.

The flowchart in Figure 5.1(a) was implemented in the SSPCs PIC microcontroller software. Figure 5.1(b) illustrates the concept waveforms for the arc fault perturbation / confirmation method. A critical parameter in this system is the time during which the SSPC will be turned off in order to quench the series arc fault in the electrical system. It is therefore important to derive the maximum time required for the load current running through a series arc fault to fall to a current level where the series arc will quench, and this is seen at Point (2) in Figure 5.1(b).



(a) Flowchart for Arc Fault Perturbation Investigation



(b) Concept Waveforms for Arc Fault Perturbation Investigation

Figure 5.1: Flowchart and Concept Waveforms for Series Arc Fault Perturbation

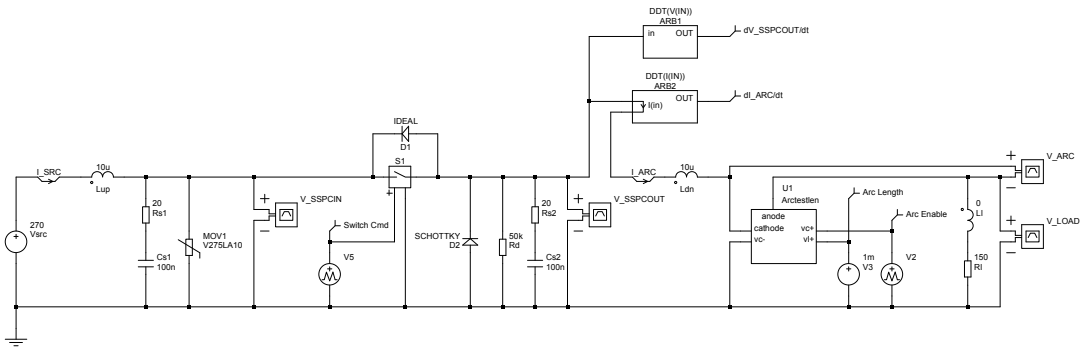


Figure 5.2: Schematic for the Arc Fault Perturbation / Confirmation SPICE Model

Assuming in Figure 5.2 that the system inductances and resistances dominate any capacitance in the system ($R_l >> R_{s2}$, $R_l >> R_d$), the time taken for the series arc to quench t_{quench} can be derived easily. The fall time t_{fall} for current in a first order RL circuit is given by Equation (5.1) and is the time taken for the current to fall below 1% of the original value. The time constant τ of the first order RL filter

presented in Figure 5.5 is given in Equation (5.2).

$$t_{fall} = 5\tau \tag{5.1}$$

$$\tau = \frac{L_{dn} + L_l}{R_l} \tag{5.2}$$

The arc current immediately following an arc strike I_{str} is approximated by Equation (5.4). Equation (5.6) shows an expression for quench time t_{quench} with respect to loop current $I(t)$, which allows the arc quench time t_{quench} to be calculated. Assuming that for short arcs (<1mm) in free air the quench current $I_{quench} \approx 400\text{mA}$ then it is possible to derive Equation (5.7).

$$R_l = \frac{V_{src}}{I_{load(nom)}} \tag{5.3}$$

$$I_{str} = \frac{V_{src} - V_{arc}}{R_l} \tag{5.4}$$

$$I(t) = I_{str} \exp\left[\frac{t}{\tau}\right] \tag{5.5}$$

$$t_{quench} = \frac{L_{dn} + L_l}{R_l} \ln\left[\frac{I_{str}}{I_{quench}}\right] = \frac{L_{dn} + L_l}{R_l} \ln\left[\frac{V_{src} - V_{arc}}{I_{quench} R_l}\right] \tag{5.6}$$

$$t_{quench} = \frac{L_{dn} + L_l}{R_l} \ln\left[\frac{I_{str}}{I_{quench}}\right] = \frac{L_{dn} + L_l}{R_l} \ln\left[\frac{V_{src} - V_{arc}}{0.4 R_l}\right] \tag{5.7}$$

When determining the quench time t_{quench} in a circuit configuration where the load resistance is not dominant, the output snubber resistor R_{s2} and capacitor C_{s2} have a greater influence, and therefore the fall time of the load current on interruption is significantly longer than a simple first order RL decay. As a consequence of this longer decay time the arc quench time t_{quench} is significantly longer. The initial condition for load current following arc strike is given by Equation (5.8) and the natural response of the SSPC output is given by $H(s)$ in Equation (5.10).

$$I_{load(strike)} = \frac{V_{src} - V_{arc}}{R_l} \tag{5.8}$$

$$L = L_{dn} + L_l \tag{5.9}$$

$$H(s) = \frac{s - \dfrac{L}{R_l}}{s^2 \left[L\left(R_{s2} + R_d\right)\right] + s\left[R_{s2}R_l + R_d R_l + R_d R_{s2} + \dfrac{L}{C_{s2}}\right] + \dfrac{R_l + R_d}{C_{s2}}} \tag{5.10}$$

Since the solution for Equation (5.10) is not trivial, MATLAB® was used to perform an inverse LaPlace transform on Equation (5.10) in order to give the SSPC output natural response in the time domain, thus allowing Figure 5.3 to be plotted.

Figure 5.3 shows the arc quench time envelope for the range of output current and downstream / load inductance supported in the SSPC specification. This plot indicates that a minimum SSPC off time of 57μs is required to ensure that arcs will quench for load currents up to 25A with downstream / load inductances up to 150μH.

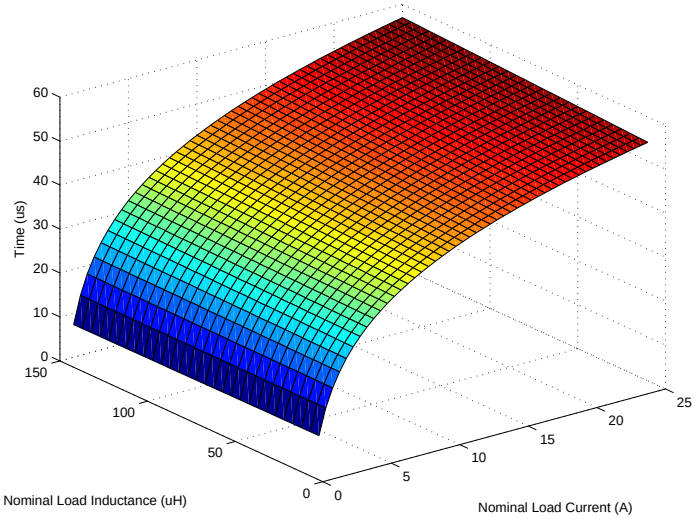


Figure 5.3: Surface Plot Showing Arc Current Quench Time as a Function of Downstream / Load Inductance and Steady State Load Current

One aspect of this concept assumes that the SSPC can be opened, the arc can be quenched, and the SSPC can be reclosed before the arc gap closes. This concept also assumes that after power is restored that this will not cause an electric breakdown across the open arc gap. Consequently the more lengthy the interruption time, the greater the ability to quench series arcs in highly inductive circuits, however, the arc gap may have closed in this time thus clearing the fault.

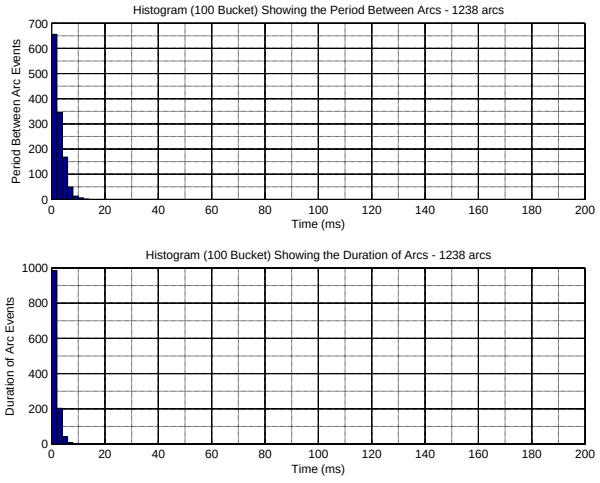


Figure 5.4: Histogram Showing Typical Arc Periods and Arc Durations for a Series Arc Fault - 270VDC, 2.5A Load

For shorter interruption times arc quench is not guaranteed, but the probability of detecting the series arc is increased, therefore the typical duration of series arcs captured during the loose terminal characterisation activity in Appendix A should be

considered. The distribution given in Figure 5.4 shows the arc durations and arc periods for a series arc fault in a 270VDC system with a 2.5A resistive load and downstream / load inductance totalling 24μH. From the raw arc duration data it can be determined that around 10% of arcs have a duration less than 100μs, and consequently this will allow time for arcs to quench with only 10% re-closing the arc gap during the interruption time. Note that the histogram scaling matches that used during the arc fault characterisation activity in Chapter 3 such that the data between multiple test runs can be easily compared.

There is a further risk that when the SSPC is reclosed following interruption, the reapplication of the SSPC output voltage across the arc gap will cause the arc gap to breakdown and current to resume flowing through the arc. This can be mitigated by running multiple test runs on each load current level. Electric breakdown during reapplication of SSPC output voltage is retarded as a result of oxidation at the arcing electrodes, which acts as weak dielectric barrier. Since the rate of change of current during arc quench at Point (2) in Figure 5.1(b) is very fast compared with that of normal load switching transients, this alone serves as an excellent indication that a series arc fault is present, and therefore breakdown on reapplication of SSPC output voltage is not a critical feature required for operation of the perturbation scheme.

Before implementing the series arc fault perturbation scheme in hardware it was necessary to validate the experimental method, and this was achieved through modelling and simulation. The schematic in Figure 5.2 illustrates the model developed in Section 3.4, which was tailored to allow simulation of the arc fault confirmation / perturbation algorithm. The source voltage V_{src} was set to 270VDC and the SSPC itself has been simplified to behave as a simple switch S_1 with representative wire inductance values for the upstream L_{up} and downstream L_{dn} wire feeders, where it is assumed that wire resistance can be neglected. Transient suppression device MOV_1, input snubber $R_{s1} + C_{s1}$, output snubber $R_{s2} + C_{s2}$, flywheel diode D_2, anti-parallel diode D_1 and leakage resistor R_d are fitted externally to allow flexible and accurate simulation. The series arc fault is simulated by U_1, where arc length is determined by V_3 and the arc is enabled by V_2. The model does not sense dI/dt and dV/dt to provide a closed-loop trigger the perturbation / confirmation scheme, but instead coordinates the operation of the perturbation / confirmation algorithm open-loop from the switch command voltage source in order to simplify simulation. The experimental and simulation results are given in Section 5.2.3.

5.2.2 Test Methodology for the Arc Fault Perturbation Scheme

The arc fault perturbation scheme was implemented in an SSPC in accordance with the flowchart in Figure 5.1(a) and tested under the representative "loose terminal" series arc fault scenario illustrated in Figure 5.5. Power was supplied by V_{src}, which in

these experiments was provided by a California Instruments MX45 power supply [253]. The power supply was connected to an SSPC through the upstream cabling shown as a simple equivalent inductance assuming negligible resistance, and the SSPC provided power through a loose terminal to a resistive load. Instrumentation was provided by a four channel digital storage oscilloscope, which allowed recording at sampling rates up to 600MSPS. The instrumentation recorded SSPC output voltage $V_{sspcout}$, loop current I_{loop}, switch command status, and the arc fault detection status.

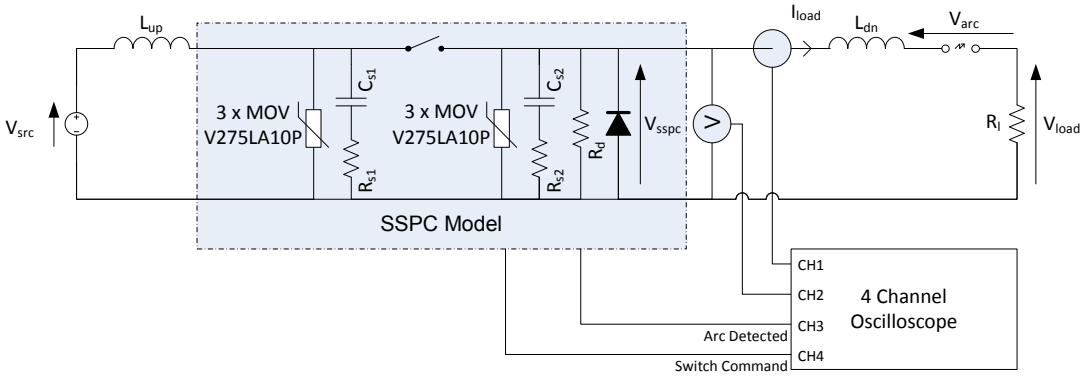


Figure 5.5: Schematic Configuration of the Arc Fault Perturbation Test System

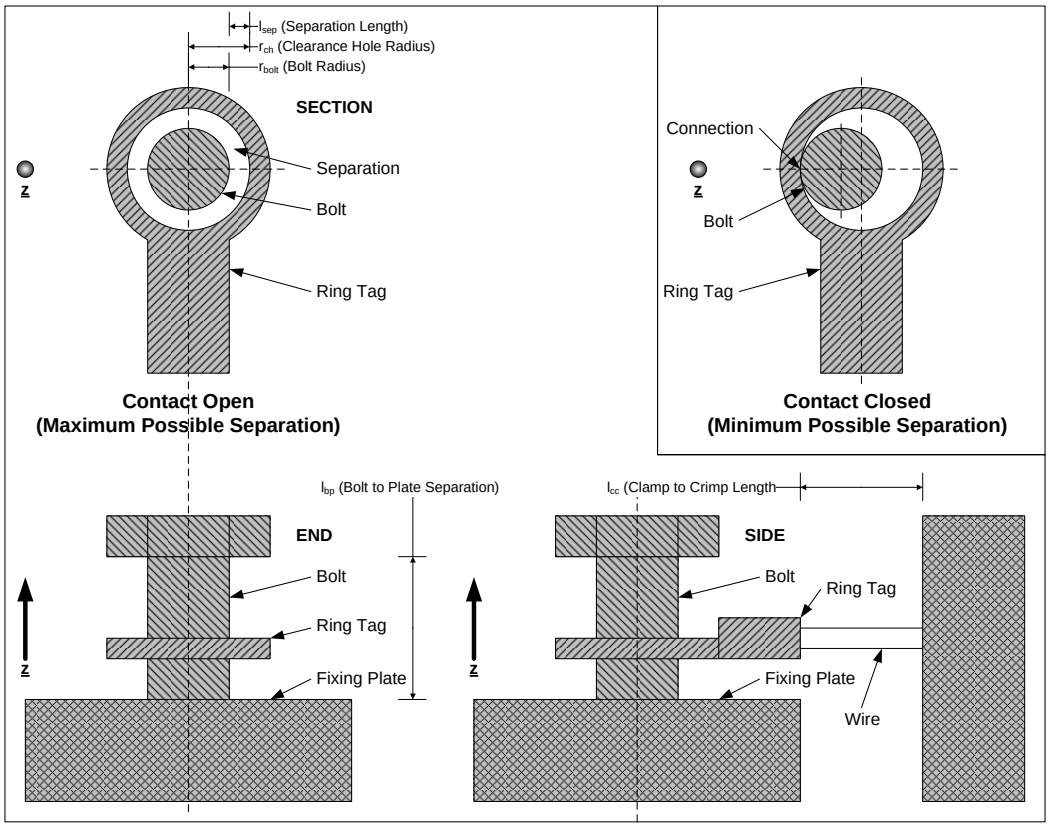


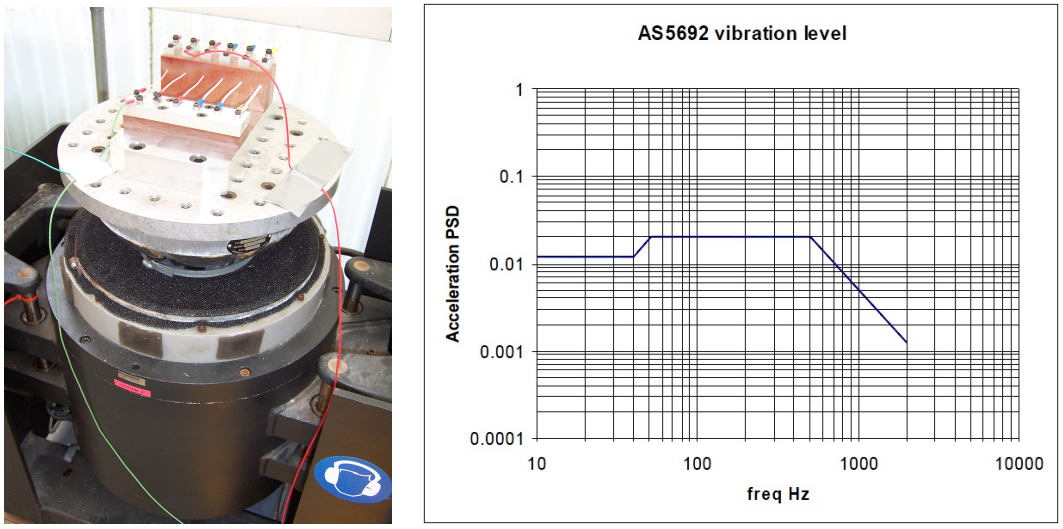
Figure 5.6: Experimental Configuration of the Loose Terminal Scenario

A common mechanical configuration illustrated in Figure 5.6 was used for all experiments. Mechanical parameters were kept constant in accordance with Table 5.1 for all experiments and arcing components were replaced after each test since the primary purpose of this series of experiments is to investigate the effect of series arc faults on electrical power distribution systems with different electrical parameters. This representative mechanical configuration given in SAE AS5692 [8] limits the arc length substantially to the order of millimetres.

The loose terminal mechanical configuration and random vibration profile are illustrated in context in Figure 5.7. The random vibration profile is taken from SAE AS5692 [8], and was originally derived from the environmental qualification requirements given in RTCA DO-160G [49] for a typical fixed wing commercial jet aircraft.

Parameter	**Description**	**Value**
r_{bolt}	Bolt Radius	1.92mm
r_{ch}	Clearance Hole Radius	2.7mm
l_{sep}	Maximum Electrode Separation Length	1.4mm
l_{bp}	Bolt to Plate Separation	2mm
l_{cc}	Clamp to Crimp Length	80mm
d_{wire}	Wire Diameter	3.3mm

Table 5.1: Mechanical Parameters for All Tests



(a) An Illustration of the Loose Terminal Block Mounted on a Vibration Table

(b) Vibration Profile for Loose Terminal Scenario Given in AS5692 [8] and RTCA DO-160G [49]

Figure 5.7: Vibration Table and Vibration Profile Illustrations

5.2.3 Experimental Results

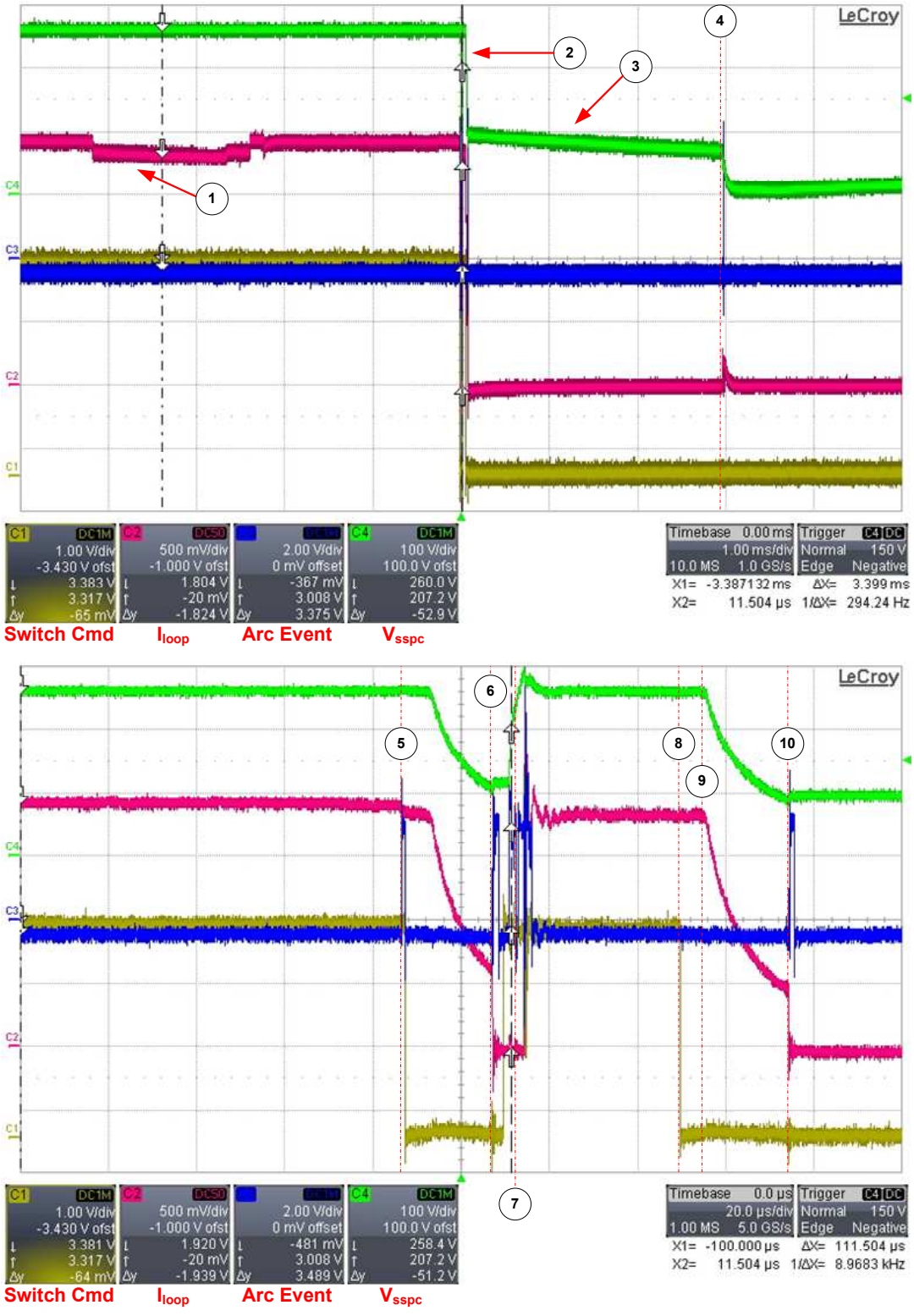


Figure 5.8: Recorded Waveforms from Arc Fault Perturbation Test Results for a Load Current of 2A

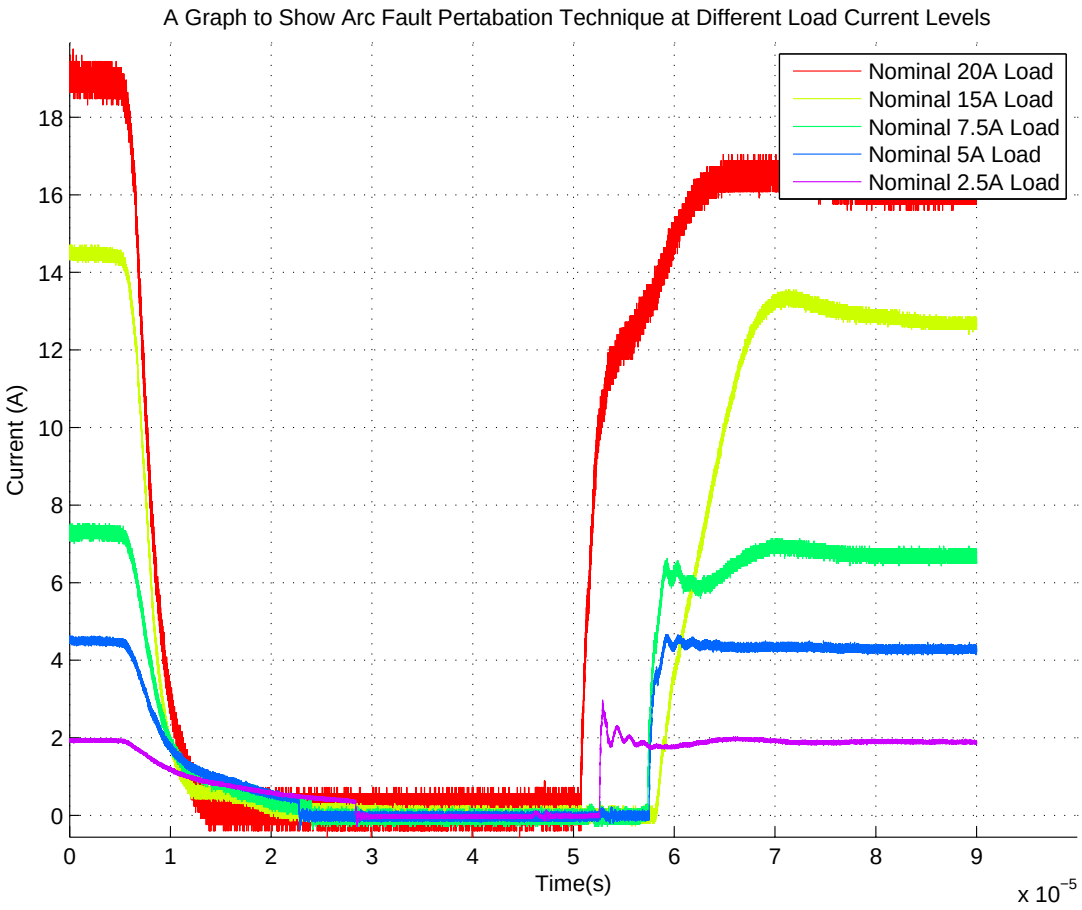


Figure 5.9: Recorded Load Current Waveforms for 2.5A, 5A, 7.5A, 15A and 20A Tests

DC Load Current (A)	**Quench Current (A)**	**Quench Time (μs)**
2.5	0.392	22.9
5	0.464	17.3
7.5	0.288	18.5
15	No Quench	No Quench
20	No Quench	No Quench

Table 5.2: Arc Quench Currents and Times for Experiments in Figure 5.9

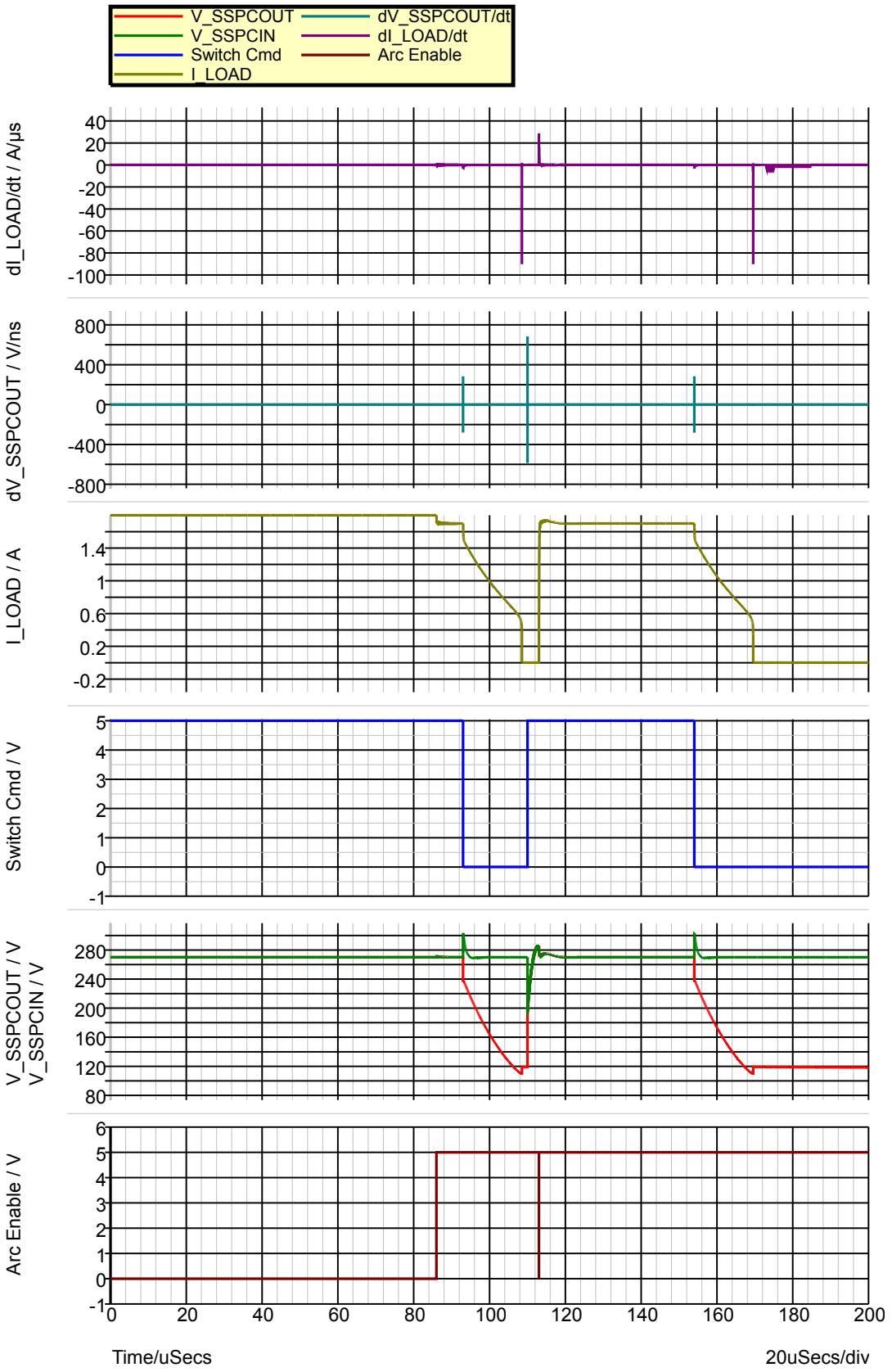


Figure 5.10: Plot Showing Results of the Arc Fault Perturbation SPICE Simulation

5.2.4 Discussion

The first part of this experiment demonstrates the basic series arc fault perturbation scheme outlined in the flowchart and concept waveforms in Figure 5.1 for a representative 270VDC power distribution circuit. The experimental results in Figure 5.8 show two relevant waveforms from this investigation in a 270VDC distribution system with a 2A resistive load that correlate with the theoretic concept waveforms, where Points (1) through (4) use a 1ms/div timebase to give an overview of the stimulus applied to the system. Point (1) shows historical series arcing. Point (2) occurs when the SSPC is turned off, the SSPC output voltage and arc current fall and the series arc quenches. Point (3) shows how the leakage current through the SSPC is slowly dissipated. Point (4) shows the reconnection of the arcing electrodes, which dissipates the SSPC leakage current, and this can be seen as a short spike in Channel C2.

Points (5) through (10) use a 20μs/div timebase and show greater detail. At Point (5) an arc strike is detected by a negative $\frac{dI_{loop}}{dt}$ event and the SSPC is immediately opened. At Point (6) the arc current falls to ~600mA, the series arc is quenched and the passive series arc fault detection output is asserted, thus providing the first method of confirmation that a series arc was present in the system. Similarly at Point (6) the SSPC output voltage falls to 100V, and since there is no longer current flowing through the series arc to the load, the charge stored in the output snubber capacitor is only discharged by the 50kΩ leakage resistor(s), and so the SSPC output voltage falls away slowly thus providing a second indication that a series arc fault was present. Note also that since the DC load here is 2A, the snubber capacitor dominates the natural response of the SSPC output stage and prevents the SSPC output voltage from falling sufficiently for the flywheel diode to conduct. At Point (7) the SSPC is reclosed and the SSPC output voltage rises again to 270VDC. However, the arc current does not immediately rise in direct accordance with the voltage due to an air gap between the arcing electrodes, and this provides the third and final indication that a series arc fault was present. At Point (8) the SSPC is tripped and commanded open as the result of a confirmed arc fault. At Point (9) the current to the load falls until again at Point (10) the arc quenches at ~500mA and the SSPC output voltage remains at 100V. The SSPC output voltage reduces over time as the snubber capacitance and any further leakage currents from the switching MOSFETs and voltage monitoring circuitry are discharged through the leakage resistor(s). Further work on exploiting SSPC leakage currents is included in Section 5.3. This confirmation / perturbation method (from Point (1) to Point (4)) could be run multiple times during a series arc fault confirmation algorithm in order to reduce nuisance trips further.

The predicted arc quench time t_{quench} can be calculated in Equation (5.11), based on the theoretical arc quench time derived in Equation (5.6).

$$\begin{aligned} t_{quench} &= \frac{L_{dn} + L_l}{R_l} \ln \left[\frac{V_{src} - V_{arc}}{I_{quench} R_l} \right] \\ &= \frac{24 \times 10^{-6}}{135} \ln \left[\frac{270 - 15}{(600 \times 10^{-6}) \times 135} \right] = 14.3 \mu s \end{aligned} \tag{5.11}$$

The prediction correlates well with the experimental arc quench time of $t_{quench} = 14\mu$s for the 2A resistive load scenario with 24μH downstream / load inductance, as illustrated in Figure 5.9. The results depicted in Figure 5.9 were repeated for multiple test runs and were found to be consistent, therefore verifying the arc quench time predictions presented in Section 5.2.1. The major challenge for accurately predicting the arc quench time t_{quench} is estimating the arc quench current I_{quench} since this varies between different fault scenarios, where longer arcs lead to higher quench currents.

The proposed power interruption has an insignificant effect on power quality since RTCA DO-160G states that power quality requirements in 270VDC systems can support an interruption of 50ms, and the interruption time required for the arc fault perturbation scheme to function correctly is $\sim$100μs. Therefore providing that the repetition rate of the arc fault perturbation scheme algorithm is sufficiently long and the interruption time is short, this will minimise the impact of the arc fault perturbation scheme on the aircraft loads and the EMI generated.

Table 5.2 shows the arc times calculated from the results of the 2.5A to 20A resistive load tests presented in Figure 5.9. These values fall within the surface plot envelope given in Figure 5.3, thus confirming the SSPC off time analysis for resistive loads equal to or less than 7.5A. The arcs shown in Figure 5.3 quench at currents between 0.288A and 0.464A, again supporting the SSPC off time analysis. The arc quench times t_{quench} and quench currents measured during this experiment align with the predictions outlined in Section 5.2.1.

For currents greater than 7.5A it was determined that regardless of the interruption time the series arcs quench less readily. Both the downstream wiring inductance and the snubber capacitor have stored energy to discharge immediately after the switch opens. Initially the snubber capacitor continues to support the output voltage from the switch and hence the load current. However, as load currents are increased, the snubber capacitor rapidly discharges and the inductive energy creates a negative voltage on the switch output which allows loop current to be delivered through the flywheel diode. Equation (5.12) shows how the snubber networks are less dominant at higher load current levels since the energy Q_{s2} stored in the output snubber capacitor C_{s2} is a function of the line voltage V_{src}, which remains consistent regardless of load current I_{load}. Equation (5.13) describes the energy Q_{dn} stored in the downstream

wiring inductance L_{dn}, which is proportional to the square of the load current I_{load} and therefore as load current increases the downstream wiring inductance quickly becomes dominant.

$$Q_{s2} = \frac{1}{2}C_{s2}V_{src}^2 \tag{5.12}$$

$$Q_{dn} = \frac{1}{2}L_{dn}I_{load}^2 \tag{5.13}$$

The energy stored in the downstream wiring inductance is sufficient to maintain the arc down below the typical ∼500mA arc quenching current, and this is achieved by creating an arc voltage which can exceed the line voltage to the switch. This behaviour can be observed in Figure 5.9 and could be prevented by fitting a higher capacitance snubber to prevent flywheel diode conduction. The current snubber in the PEPDC / PEPSC designs was chosen to stabilise the upstream and downstream wiring inductances during linear current limit operation of the switching MOSFETs. A higher capacitance value improves stability of the current limit circuit and therefore there is little risk to the main switching and control function of the SSPC as a result of increasing the capacitance value to promote arc quenching during operation of the arc fault perturbation scheme. However, increasing the capacitance is not a trivial matter since 100nF 1000V rated surface mount capacitors are both large (typically an imperial 2220 package) and high cost components.

The load current created by the arc quench current discontinuity can be easily detected since the rate of change of current with respect to time is very fast and can be detected by the passive electrical series arc fault dI/dt detector developed in Section 4.3. Aircraft loads would typically not present a waveform with a fast current waveform since they feature input power filters which limit the rate of change of current with time in order to prevent EMC susceptibility / emission issues. Furthermore the rate of change of current is no longer limited by the system wiring loop inductance during series arc fault quench, and thus the rate of change of current during arc quench is several orders of magnitude greater than that encountered during normal operation. Figure 5.8 Channel C3 shows a positive going edge on the $\frac{dI_{loop}}{dt}$ detection logic signal during the arc quench current discontinuity at Point (6). This pulse was present during the testing of resistive loads up to 7.5A, thus verifying the predicted behaviour defined in the theoretical flowchart given in Section 5.2.1.

It was predicted from Figure 5.4 that in ∼90% of cases there would be a delay between re-closing the SSPC after the 100μs interruption and the corresponding rise in load current due to the presence of an air gap between the arc electrodes in the current path. Such a delay can be observed in Figure 5.8 between re-closing of the SSPC at Point (7) and the associated rise in load current. If this delay exists in an aircraft environment then there is either an open circuit within the downstream wiring network, or the load is expressing non-linear behaviour. Since RTCA DO-160G tests

electrical systems with power interruptions in the order of 50ms, it is unlikely that a 100μs interruption will cause a load to create a series arc-like discontinuity.

Finally Figure 5.10 illustrates the results of a SPICE simulation based on the arc model developed in Section 3.4, which implements the same schematic configuration used to gather the practical experimental results for a 2A resistive load shown in Figure 5.8. The results in Figure 5.10 show that the simulated loop current I_{loop} and SSPC output voltage $V_{sspcout}$ waveforms correlate well with the experimental waveforms in Figure 5.8. Note that the time scale on the SPICE simulation results in Figure 5.10 matches that of the practical experimental results in Figure 5.8, and the switch command signal is also directly correlated between the plots in order to further simplify the comparison exercise. The arc is enabled at time 86μs and the load current I_{load} in the simulation model shows consistent behaviour with the practical results, where the arc quench current is around 500mA. SSPC output voltage $V_{sspcout}$ also shows consistent behaviour, where the voltage falls only to 100V at the point of arc quenching, suggesting that this voltage is being maintained by the output snubber capacitor C_{s2}. Further to the experimental data, the simulation shows how the arc quench can be easily detected using the $\frac{dI_{loop}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ detector systems, because $\frac{dI_{loop}}{dt}$ during arc quench is 90A/μs which is significantly larger than the 1-2A/μs experienced during arc strike, and $\frac{dV_{sspcout}}{dt}$ is 600V/ns which again is greater than the 300V/ns which occurs during arc strike. The arc fault perturbation / confirmation system therefore generates an easily detectable pulse which does not require any additional hardware beyond the existing passive $\frac{dI_{loop}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ detection circuits. The results of this SPICE simulation support the experimental results outlined in this section including arc quench time t_{quench}, arc quench current I_{quench} and the sensitivity of the confirmation / perturbation scheme to the output snubber capacitance value. Furthermore the results presented in the SPICE simulation further validate the series arc fault model and overall electrical power distribution models developed during the wider modelling activity in Chapter 3.

5.3 Arc Fault Confirmation Using SSPC Leakage

5.3.1 Theory and Predictions

Unlike traditional electromechanical relays, contactors and circuit breakers, SSPCs feature unwanted leakage current when the SSPC is in the open state. The leakage current in the PEPDC / PEPSC designs is further exacerbated by a potential divider voltage monitor fitted between the input and output of the SSPC for the purposes of switch voltage measurement. The human safety aspect of SSPC leakage currents

has long been a cause for concern, and hence the SSPC leakage current is managed either passively with a discrete resistor or actively with a semiconductor pulldown device fitted between the SSPC output and chassis. The PEPDC and PEPSC designs manage leakage current with a resistive pulldown element which ensures that the SSPC output voltage cannot exceed ∼30VDC under no-load conditions.

The majority of the experimental work carried out during the series arc fault characterisation activity in Appendix A occurred with the SSPC in the closed state. It was unintentionally observed during the development of the arc fault perturbation scheme that when a loose terminal is present at the output of an open SSPC, the leakage current and corresponding developed SSPC output voltage is modulated, creating a pattern indicative of a loose terminal fault. An important feature in aircraft electrical power distribution systems is that the load is typically permanently connected during normal operation, unlike an equivalent domestic scenario. It is therefore envisioned that this technique could be used to confirm that a loose terminal or drawn series arc fault is present on an SSPC output prior to a series arc fault trip event. In similarity with the arc fault perturbation scheme in Section 5.2 this confirmation scheme is passive in that the SSPC output voltage is monitored for signals indicative of a loose terminal or drawn arc series arc fault, and also active since a small leakage current deliberately flows to the load when the SSPC is commanded open.

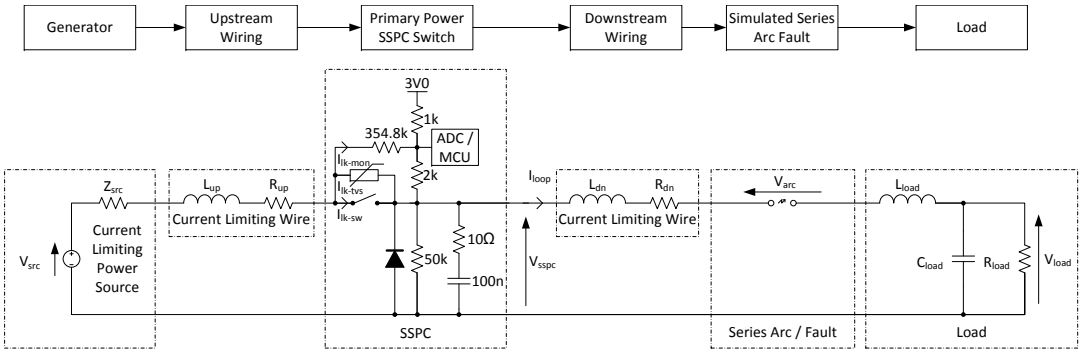


Figure 5.11: Schematic Configuration of the Open SSPC / Series Fault Scenario

Figure 5.11 shows a series fault scenario where the SSPC is in the open state. The leakage current through the SSPC is contributed from three parallel paths, the first path I_{lk-sw} is through the switch element which consists of $N_{fets} = 16$ parallel MOSFET devices, the second path I_{lk-mon} is through the resistive switch voltage monitor, and the final path I_{lk-tvs} is through the transient suppression component. The leakage current through the transient suppression component I_{lk-tvs} is very small compared with the other two paths and can therefore be neglected from the following analysis.

The leakage current through each MOSFET device I_{lk-fet} in the presence of a drain-source voltage of $V_{DS} = 1200$V at +25°C is 30nA, rising to 100μA at +175°C. The

worst-case total switch leakage current I_{lk-sw} at +25°C and +175°C at the RTCA DO-160G specified maximum 270VDC bus voltage of 285VDC can be calculated in accordance with Equations (5.14) and (5.15) respectively [49]. Lower temperatures are of less interest since this will result in lower leakage currents. The calculated leakage currents assume that there is a low impedance load attached to the SSPC output, however, if there was no load present the leakage current would be defined by the passive pulldown resistor(s) only. For modelling and simulation purposes it is simpler to deal with resistances, and thus an estimation of the switch leakage resistance R_{lk-sw} at +25°C and +175°C can be calculated assuming a linear relationship between leakage current and V_{DS} from the total switch leakage currents, and these are given in Equations (5.16) and (5.17) respectively.

$$I_{lk-sw(+25°C)} = \frac{V_{src}}{1200} N_{fets} I_{lk-fet} = \frac{285}{1200} \times 16 \times 30nA = 114nA \quad (5.14)$$

$$I_{lk-sw(+175°C)} = \frac{V_{src}}{1200} N_{fets} I_{lk-mosfet} = \frac{285}{1200} \times 16 \times 100\mu A = 380\mu A \quad (5.15)$$

$$R_{lk-sw(+25°C)} = \frac{V_{DS}}{N_{fets} I_{lk-fet(+25°C)}} = \frac{1200}{16 \times 30} = 2.5G\Omega \quad (5.16)$$

$$R_{lk-sw(+175°C)} = \frac{V_{DS}}{N_{fets} I_{lk-fet(+175°C)}} = \frac{1200}{16 \times 100} = 750k\Omega \quad (5.17)$$

The voltage monitor measures the voltage across the switch and feeds a signal into an Analogue-to-Digital Converter (ADC) and Microcontroller Unit (MCU) whose 3V0 power supply return is referenced to the SSPC output voltage, as illustrated in Figure 5.11. The leakage current I_{lk-mon} exists as a result of the additional resistance introduced across across the SSPC, and the leakage resistance due to this voltage monitor can be calculated in accordance with Equation (5.18). The resistors chosen for the voltage monitor have a 1% resistance tolerance with a resistance temperature coefficient of 50ppm/°C, and therefore the variation of the voltage monitor resistance is negligible compared with the variation of the MOSFET leakage resistance.

$$R_{lk-mon} = 354.8k + (1k \parallel 2k) = 355.5k\Omega \quad (5.18)$$

The total switch leakage resistance can therefore be calculated in accordance with Equations (5.19), (5.20) and (5.21).

$$R_{lk} = R_{lk-sw} \parallel R_{lk-mon} \quad (5.19)$$

$$R_{lk(+25°C)} = R_{lk-sw(+25°C)} \parallel R_{lk-mon} = 2.5G \parallel 355.5k = 311.24k\Omega \quad (5.20)$$

$$R_{lk(+175°C)} = R_{lk-sw(+175°C)} \parallel R_{lk-mon} = 355.5k \parallel 750k = 241.18k\Omega \quad (5.21)$$

Figure 5.12 shows a simplified schematic of the PEPDC and PEPSC SSPC module in the open state. The flywheel diode and transient suppressor can be neglected here since they exhibit minimal leakage current over the temperatures of interest. The total switch leakage resistances R_{lk} calculated in Equations (5.20) and (5.21) can be

directly substituted into the model. The PEPDC output snubber consists of resistor $R_s = 10\Omega$ and capacitor $C_s = 100\text{nF}$, and a passive pulldown resistor $R_p = 50\text{k}\Omega$ is used.

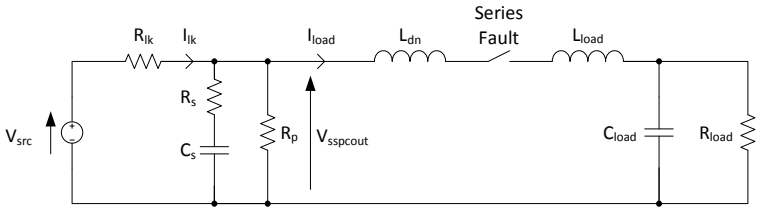


Figure 5.12: Simplified Schematic for SSPC Leakage Analysis

The downstream wiring inductance L_{dn}, load capacitance C_{load}, load inductance L_{load} and load resistance R_{load} with associated loop current I_{loop} are assumed to vary in the ranges specified in Table 5.3.

Parameter	**Minimum Value**	**Maximum Value**
$R_{load}(I_{loop})$	2.25Ω (120A)	270Ω (1A)
$L_{dn} + L_{load}$	10μH	100μH
C_{load}	0μF	500μF

Table 5.3: Parameter Range for SSPC Leakage Behaviour Analysis

Firstly consider the static case where the SSPC is open and there is a healthy load electrically connected to the SSPC output. It is important to consider the worst case steady state SSPC output voltage due to the total switch leakage current, and this occurs when the SSPC input voltage is at the maximum $V_{src} = 285\text{V}$, the load resistance is at the maximum $R_{load} = 270\Omega$ ($I_{loop} = 1\text{A}$ loop current), and the SSPC is at +175°C with a leakage resistance of $R_{lk(+175°C)} = 241.18\text{k}\Omega$. Equation (5.22) shows that this worst case voltage is 317mV, and therefore any SSPC output voltage exceeding 317mV when the SSPC is commanded open is indicative that either the SSPC module has failed or that there is a wire fault downstream from the SSPC. This result also assumes that loads such as switching power supplies do not become high impedance when their input voltages fall below the nominal 270VDC input voltage.

$$\begin{aligned} V_{sspcout} &= V_{src}\frac{R_p \parallel R_{load}}{R_{lk(+175°C)} + (R_p \parallel R_{load})} \\ \therefore V_{sspcout} &= 285 \times \frac{50k \parallel 270}{241.2k + (50k \parallel 270)} = 317mV \end{aligned} \tag{5.22}$$

Secondly consider the dynamic case where the SSPC is open and the electrical load becomes disconnected from the SSPC output. It can be assumed that since the leakage current reaching the load is minimal, the load disconnection is manifested as a step change in load impedance from the healthy load impedance to a high impedance. The

rise time characteristics of the SSPC output voltage waveform can be determined by analysing the simplified SSPC leakage schematic in Figure 5.12 and deriving the s-domain representation of SSPC output voltage $V_{sspcout}(s)$ in Equation (5.23), where the source voltage V_{src}(s) can be modelled as a unit step of magnitude V_{src} as given in Equation (5.24). Rather than beginning with a SPICE simulation, this simple analysis assists with the qualitative understanding of SSPC output voltage behaviour.

$$V_{sspcout}(s) = V_{src}(s)\frac{R_p \parallel \left(R_s + \frac{1}{sC_s}\right)}{R_{lk} + \left(R_p \parallel \left(R_s + \frac{1}{sC_s}\right)\right)} \tag{5.23}$$

$$V_{src}(s) = \frac{V_{src}}{s} \tag{5.24}$$

The expression for V_{out}(s) in Equation (5.23) can then be arranged in the form of Equation (5.26), with constants α, K_1 and K_2 given by Equations (5.26), (5.27) and (5.28) respectively.

$$V_{sspcout}(s) = V_{src}\left(K_1\frac{1}{s+\alpha} + K_2\frac{\alpha}{s\,(s+\alpha)}\right) \tag{5.25}$$

$$\alpha = \frac{R_{lk}+R_p}{C_s\left(R_{lk}R_p + R_{lk}R_s + R_pR_s\right)} \tag{5.26}$$

$$K_1 = \frac{R_pR_s}{R_{lk}R_p + R_{lk}R_s + R_pR_s} \tag{5.27}$$

$$K_2 = \frac{R_p}{R_{lk}+R_p} \tag{5.28}$$

Using the standard inverse LaPlace transforms given in Equations (5.29) and (5.30) it is possible to derive a first-order time domain expression for $V_{sspcout}$(t) in Equation (5.31).

$$\mathcal{L}^{-1}\left\{\frac{1}{s+\alpha}\right\} = e^{-\alpha t}u(t) \tag{5.29}$$

$$\mathcal{L}^{-1}\left\{\frac{\alpha}{s(s+\alpha)}\right\} = \left(1-e^{-\alpha t}\right)u(t) \tag{5.30}$$

$$V_{sspcout}(t) = \mathcal{L}^{-1}\left\{V_{sspcout}(s)\right\} = V_{src}\left(\left(K_1-K_2\right)e^{-\alpha t} + K_2\right)u(t) \tag{5.31}$$

With Equation (5.31) it is now possible to compute the range of possible SSPC output voltage step response waveforms when a series open fault occurs for the minimum, nominal and maximum SSPC input voltages of 255VDC, 270VDC and 285VDC respectively at both +25°C and +175°C. MATLAB® is used to plot the SSPC output voltage step response waveforms in Figure 5.13. When the SSPC output voltage reaches a threshold of 30V it can be assumed that the load is open circuit. Figure 5.13 shows that the slowest time for the SSPC voltage to reach 30V of 38.4ms occurs where the SSPC input voltage is at the minimum V_{src} = 255VDC at a temperature of +25°C, and the fastest time to reach 30V of 18.4ms occurs with the highest SSPC

input voltage V_{src} = 285VDC and highest temperature +175°C. The rise time will be slower with temperatures below +25°C, however, this scenario is unlikely to occur due to other heat sources around the SSPC module. SSPC output current waveforms for the six scenarios are also included for completeness, and these show a variation in SSPC output current between 0.8mA through 1.2mA.

Computing the SSPC output leakage voltage rise times is a relatively simple process since the load is disconnected from the SSPC output and can be disregarded in the LaPlace analysis, thus resulting in a first-order system. However, computing the SSPC output leakage voltage fall times for different load conditions is more troublesome since this requires analysis of a third-order system, and therefore a SPICE simulator is used to plot a range of different load scenarios. Figure 5.14 illustrates the SSPC output leakage voltage behaviour during closing of the series fault element under varying electrical load scenarios.

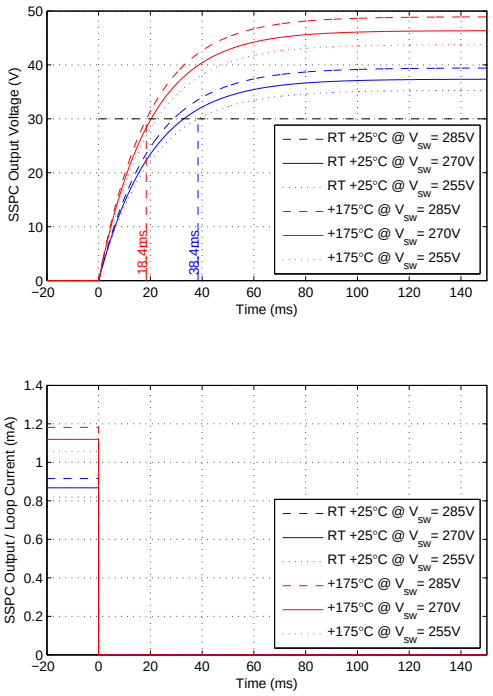


Figure 5.13: SSPC Output Leakage Voltage Step Responses (Transition to Series Fault Open)

The SSPC output leakage voltage fall times vary with temperature, SSPC input voltage and the electrical load. Fast SSPC output leakage voltage falling edges are trivial to detect, and thus to design the proposed arc fault confirmation system, the slowest fall time is a critical parameter which needs to be understood. The left hand plots in Figure 5.14 illustrate the effects of varying load on fall times under a nominal room temperature of 25°C and a nominal line voltage of 270VDC, where the fastest falling edge occurs with a 500μF capacitive load attached to the SSPC output because

a capacitive load exhibits very low impedance under changing load voltage conditions. The right hand plots in Figure 5.14 demonstrate that the slowest fall time is exhibited by the minimum 1A resistive load, where downstream and load inductance has very little impact on fall time since the load current level is low. The right hand plots also show that although temperature and SSPC input voltage influence the steady state SSPC output leakage voltage, the fall time between the load connection at time zero and the SSPC output leakage voltage reaching 0.5V is approximately 0.7ms. The worst case fall time is therefore two orders of magnitude faster than the worst case rise time of 38.4ms, which implies that detection of the transition from load connected to load open circuit is slower than that of the detection of the transition from load open circuit to load connected.

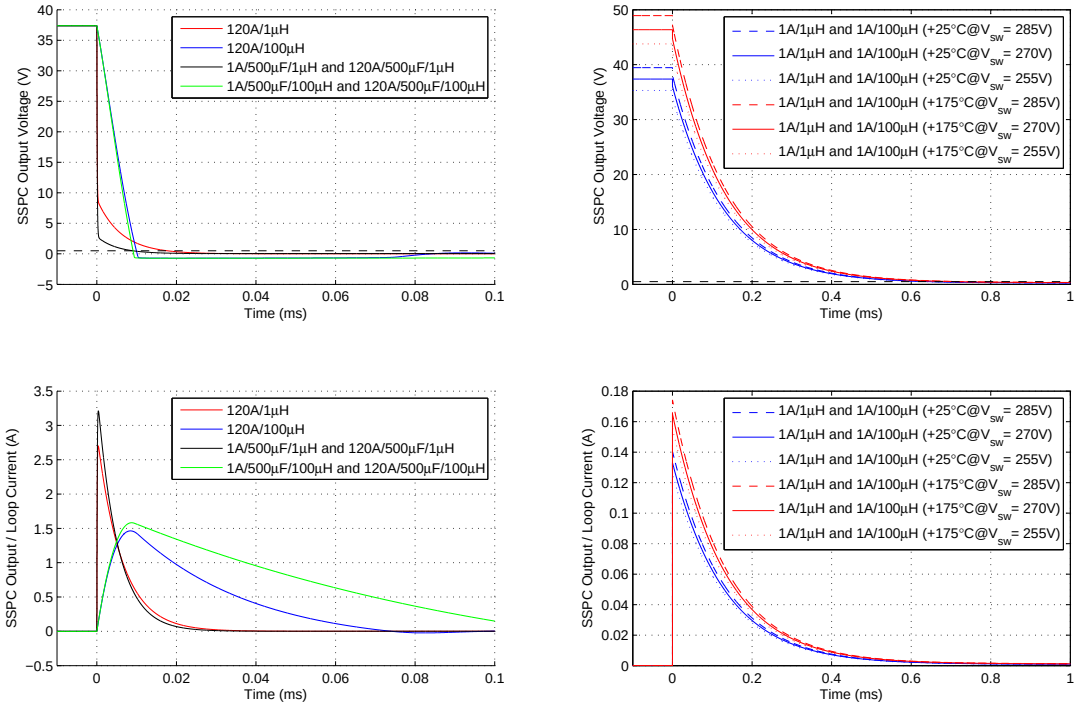
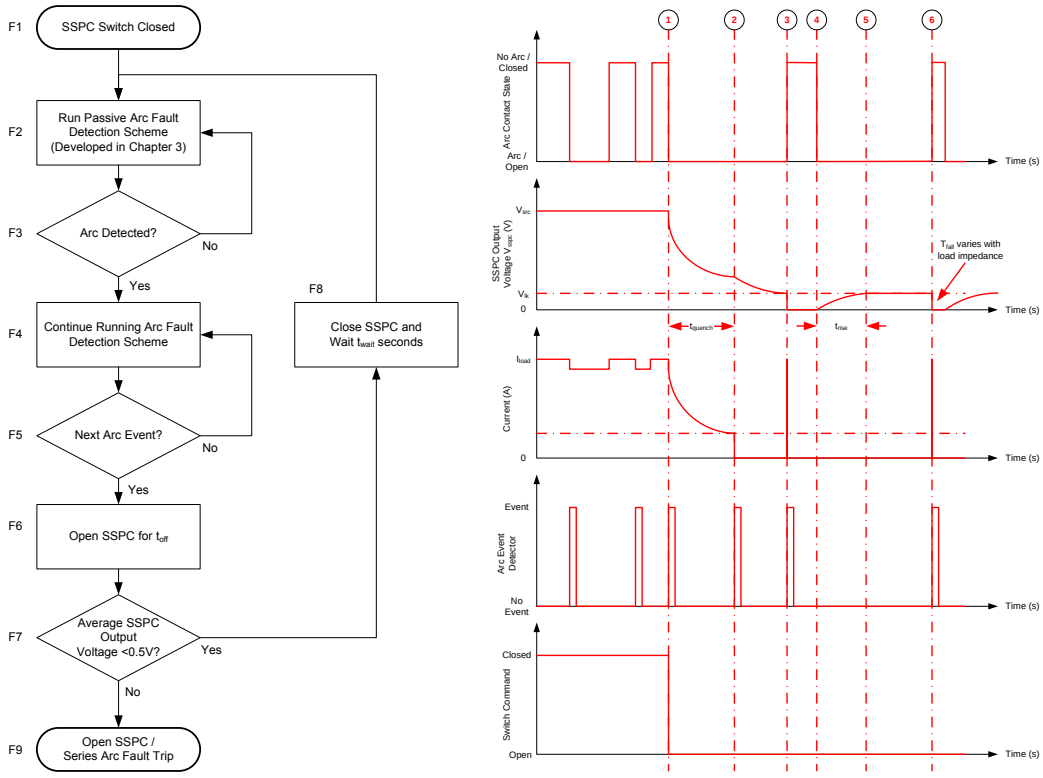


Figure 5.14: SSPC Output Leakage Voltage Responses (Transition to Series Fault Close)

The proposed series arc fault confirmation system flowchart based on SSPC output leakage voltage analysis is illustrated in Figure 5.15(a).

This system has been made possible by the inherent leakage current in the high voltage power MOSFET devices used in SSPC modules. The flowchart in Figure 5.15(a) was implemented in software within the SSPC PIC microcontroller. Figure 5.15(b) illustrates the concept waveforms for the SSPC output leakage voltage arc fault confirmation method. Similarly to the perturbation scheme in Section 5.2, the required interruption time is less than the 50ms allowed in RTCA DO-160G [49].



(a) Flowchart for SSPC Leakage Based Arc Fault Confirmation Scheme

(b) Concept Waveforms for SSPC Leakage Based Arc Fault Confirmation Scheme

Figure 5.15: Flowchart and Concept Waveforms for SSPC Output Leakage Voltage Based Arc Fault Confirmation

Figures 5.15(a) and 5.15(b) show how the proposed series arc fault confirmation scheme is similar to the arc fault perturbation scheme, where the SSPC is closed and a series arc fault is present in the system prior to Point (1). Elements F1 through F5 in the arc fault confirmation flowchart cover the arc fault detection process up to Point (1) in the concept waveforms. During this time the loose terminal series arc fault is detected by the passive series arc fault detection system developed in Chapter 4, and confirmed using the leaky integrator algorithm. At Point (1) the series arc fault detection system opens the SSPC in accordance with flowchart element F6, resulting in an exponentially reducing SSPC output current up to Point (2), where the series arc quenches and the SSPC output current falls to zero. It should be noted that this scheme would function equally well regardless of whether a series arc is present at Point (2). Following the arc quench at Point (2) the arc current falls to zero and the series arc becomes an open circuit. Between Points (2) and (3) the energy stored in snubber capacitor C_s is dissipated in pulldown resistor R_d and the SSPC output voltage reduces to the steady state leakage voltage. If a resistive load $R_{load} \leq 270\Omega$ is correctly electrically connected to the SSPC output, the SSPC output voltage would decay down to a voltage $V_{sspcout} \leq 317\text{mV}$. During this time, element F7 in the

flowchart process detects that the SSPC is commanded open, and that the average SSPC output voltage over time $t_{avg} = 100\mu$s exceeds 0.5V. In addition to the main SSPC output voltage monitoring system, the passive electrical series arc fault voltage monitoring hardware developed in Section 4.4 can be used to detect the fast reductions in SSPC output voltage due to the loose terminal between the SSPC output and the load impedance. After the criteria in flowchart element F7 is fulfilled a series arc fault trip is issued and the SSPC remains commanded open, otherwise the SSPC can be re-closed at F8 and normal operation can be resumed.

At Point (3) the series fault is closed and the SSPC output leakage voltage falls to ∼0V in accordance with the fall times calculated earlier in this section, which is accompanied with a short current spike as the energy stored in the snubber capacitor C_s is discharged into the load impedance and again this waveform feature can be detected by flowchart stage F7. At Point (4) the series fault is opened and the SSPC output leakage voltage rises over time t_{rise} between Points (4) and (5) up to the nominal static leakage voltage calculated earlier in this section, as the total switch leakage current charges the snubber capacitor C_s. At Point (6) the series fault is closed and, in the event of a "loose terminal fault, the cycle from Point (3) through (6) repeats until the fault ceases.

A further realisation during this research is that the SSPC software can be easily modified to provide a general health monitoring function, which can be run continuously when the SSPC is commanded open. This approach easily detects open and high impedance SSPC outputs, although care is needed to avoid the effects of electrical system transients such as lightning which may cause nuisance trips. Susceptibility to electrical transients can be mitigated by averaging SSPC output voltage over a few seconds to prevent nuisance trips. Alternatively the SSPC output leakage voltage and SSPC temperature can be monitored and processed to calculate the impedance of the attached load. The measured load impedance can be compared against a healthy load baseline then recorded and/or reported as a part of a Prognostics and Health Management (PHM) programme. Further work would be required to characterise typical aircraft loads over their operating envelopes.

5.3.2 Test Methodology

The purpose of the experimental testing in this section is to verify the time domain SSPC output leakage voltage behaviour against the theory and prediction when the SSPC is open.

Figure 5.16 shows the lab configuration used to validate the SSPC leakage series arc fault confirmation scheme. This test configuration is common with the other series arc fault experiments carried out in this thesis and the series fault is generated using the same SAE AS5692 loose terminal method outlined in Section 5.2.2. The main difference here is that the SSPC is open during all aspects of the testing carried out.

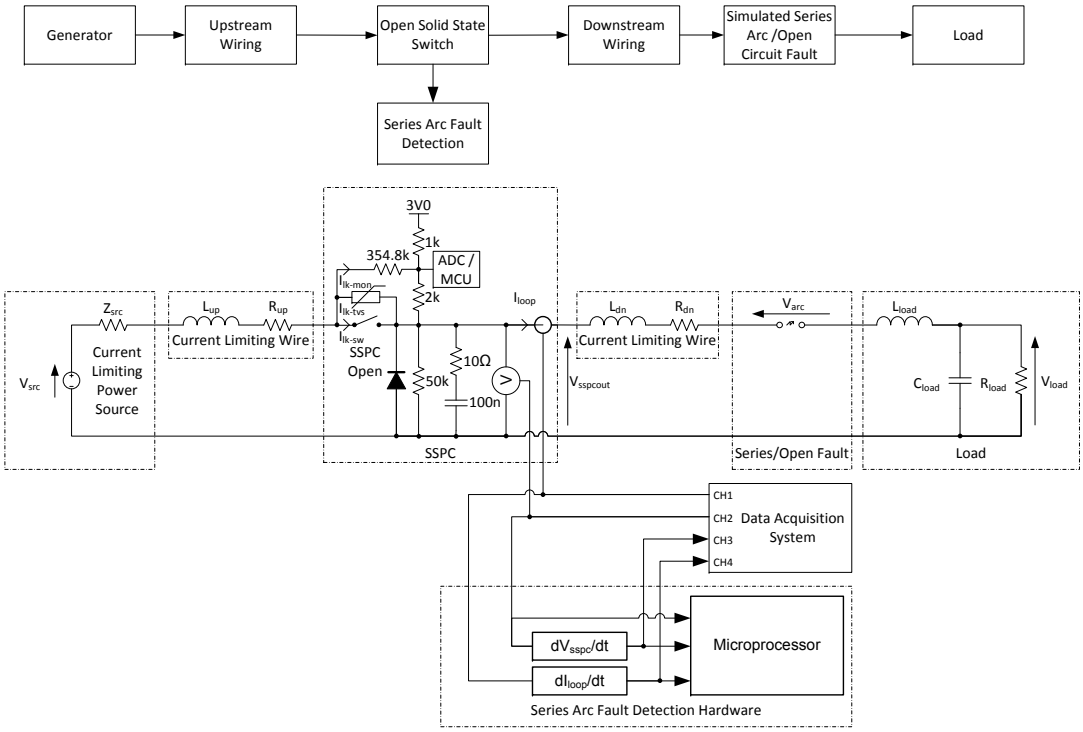


Figure 5.16: Experimental Test Schematic / Block Diagram for the SSPC Output Leakage Voltage Based Arc Fault Confirmation System

The SSPC output leakage voltage experiments were carried out with varying combinations of resistive R_{load}, capacitive C_{load} and inductive loads L_{load}, and inductive downstream wiring L_{dn} in the ranges specified in Table 5.4.

Parameter	**Minimum Value**	**Maximum Value**
$R_{load}(I_{loop})$	2.25Ω (120A)	270Ω (1A)
$L_{dn} + L_{load}$	10μH	100μH
C_{load}	0μF	380μF

Table 5.4: Parameter Range for SSPC Leakage Behaviour Experiment

For each experiment run an HBM Genesis 16t data acquisition system was configured to record at 100MSPS and was used to capture SSPC output voltage $V_{sspcout}$ using a isolated differential voltage probe, and SSPC output current / loop current I_{loop} using a Hall effect current probe such that the experimental SSPC output leakage voltage and current behaviour could be compared with the behaviour predicted in Section 5.3.1. The SSPC series arc fault voltage and current monitor analogue outputs were also recorded to enable evaluation of their series wire fault detection capability.

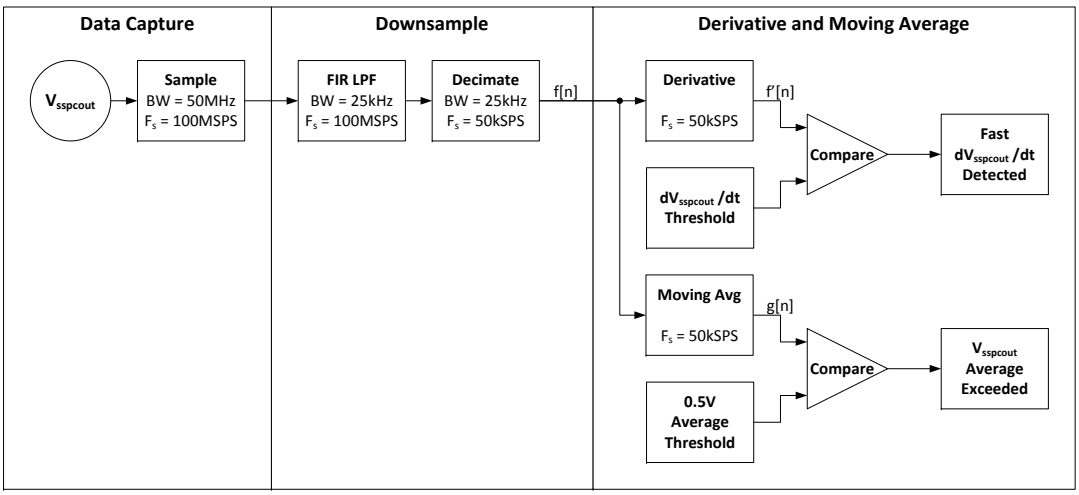


Figure 5.17: SSPC Leakage Voltage Signal Processing Block Diagram

Figure 5.17 shows how the captured data was processed in MATLAB®. The SSPC output leakage voltage signal is first decimated down to sampling rate $F_s = 50$kSPS and corresponding sample time $T_s = 20\mu$s, representing the sampling rate of the SSPC output voltage in the SSPC microcontroller. The backward difference derivative $f'[n]$ given in Equation (5.32) was computed from each sample n in the SSPC output leakage voltage signal $f[n]$ for sample time T_s as a means of detecting loose terminal reconnection events at the SSPC output [254]. Signal $g[n]$ was computed by applying a moving average filter to the SSPC output leakage voltage signal $f[n]$ to average the SSPC output leakage voltage over a 10ms window, allowing rejection of momentary SSPC output voltage transients. The number of samples N_{avg} required to provide averaging over 10ms is given in Equation (5.33), and the moving average signal $g[n]$ is calculated from Equation (5.34). The moving average signal was then thresholded to determine when an SSPC output leakage voltage event occurs.

$$f'[n] = \frac{f[n] - f[n-1]}{T_s} \tag{5.32}$$

$$N_{avg} = \frac{T_{avg}}{T_s} = \frac{10m}{20\mu} = 500 \tag{5.33}$$

$$g[n] = \frac{1}{N_{avg}} \sum_{k=0}^{N_{avg}-1} f[n-k] \tag{5.34}$$

5.3.3 Experimental Results

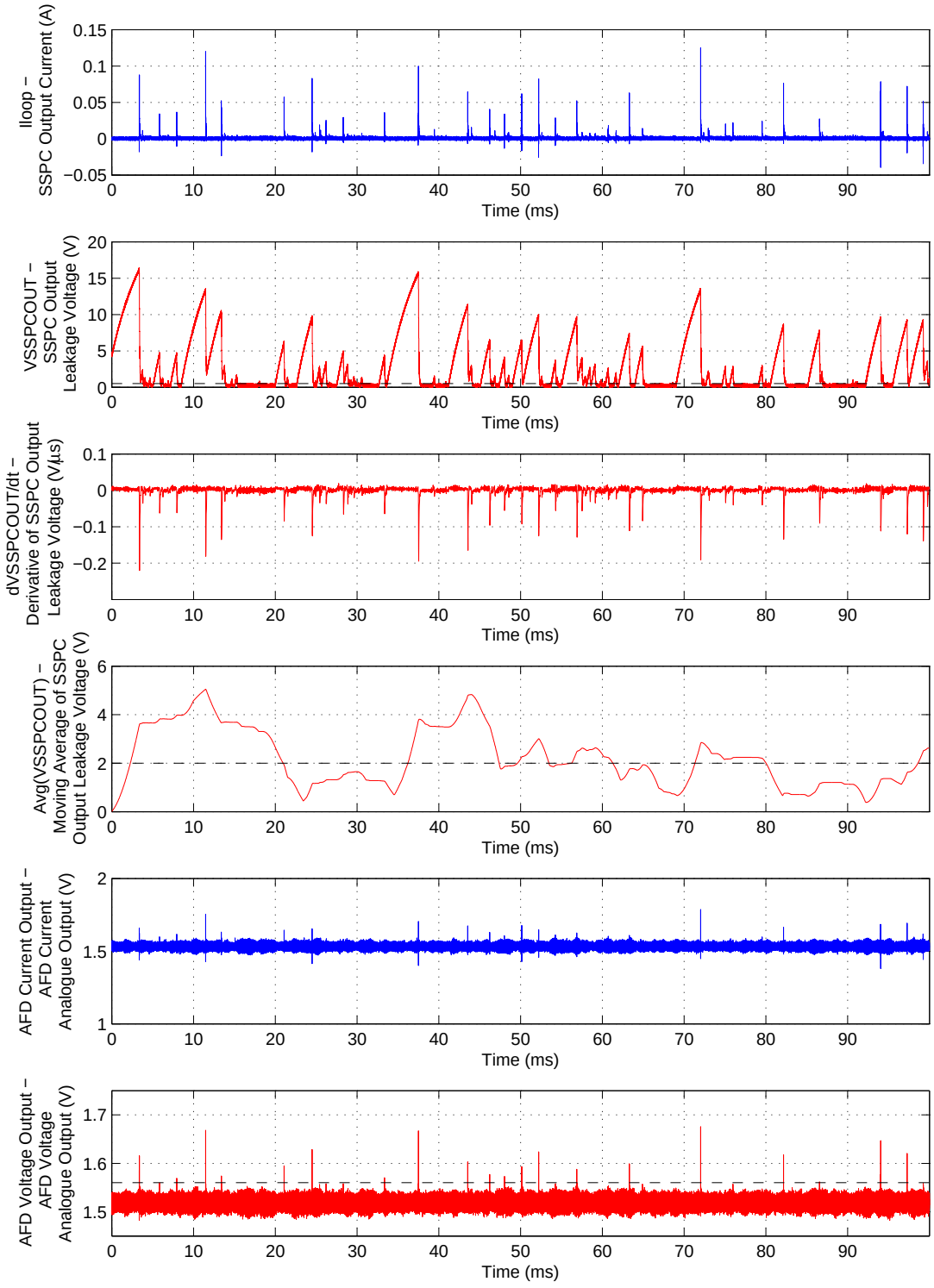


Figure 5.18: Experimental SSPC Output Leakage Voltage Behaviour ($V_{src} = 270$V, $R_{load} = 270\Omega(1\text{A})$)

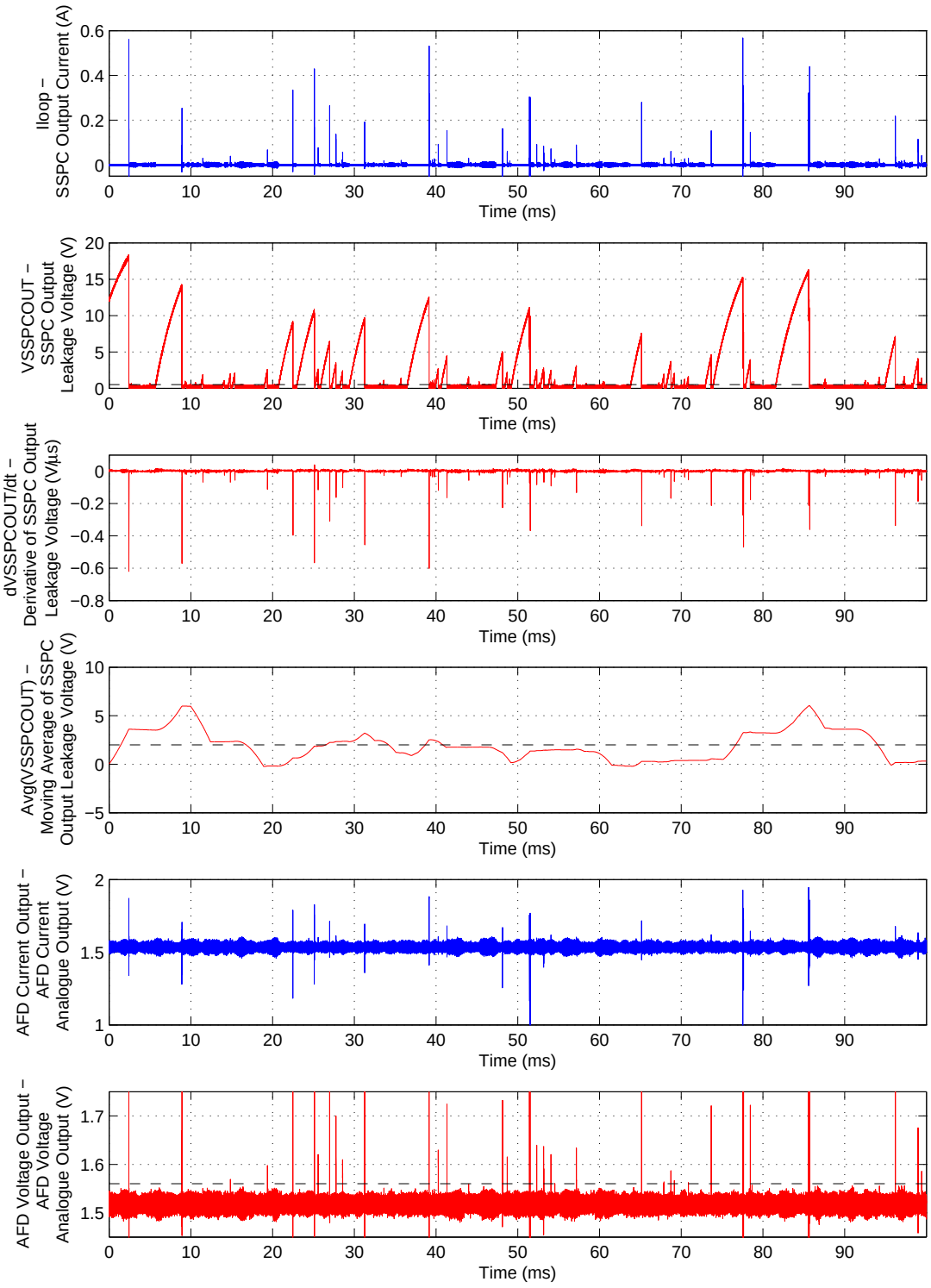


Figure 5.19: Experimental SSPC Output Leakage Voltage Behaviour ($V_{src} = 270$V, $R_{load} = 270\Omega(1\text{A})\| \; C_{load} = 500\mu$F)

5.3.4 Discussion

The results illustrated in Figures 5.18 and 5.19 show the measured SSPC output leakage voltages and SSPC output / loop currents for an SSPC input voltage of 270VDC and under the 270Ω(1A) and 270Ω(1A)‖500μF load conditions respectively. Many combinations of different loads were tested, but only the time domain waveforms in Figures 5.18 and 5.19 are presented since these illustrate the slowest and fastest falling edge scenarios respectively.

In contrast to the simulated SSPC output voltage rising edge, the experimental data does not rise up to the predicted steady state open circuit SSPC output leakage voltage and instead peaks at ∼20V. The SSPC output voltage does not reach the predicted values between 35 and 49V illustrated in Figure 5.13 because the loose terminal does not stay open long enough for the SSPC leakage current to charge up the snubber capacitor C_s. In the event of an open circuit at the SSPC output, the SSPC output leakage voltage would reach the predicted steady state value and this can be easily detected using a high threshold on the moving average filter output. The vibration characteristics in the mechanical domain have a significant impact on the SSPC output leakage voltage waveform, and since the SSPC leakage current is very low, there is insufficient energy to draw a significant arc across the series fault and thus interaction between the mechanical and electrical domains is minimal. This results in the higher frequency vibration seen during low current series arc faults, as observed during the characterisation activity in Section A.4. From Figures 5.12 and 5.16 it can be seen that to increase the SSPC output leakage voltage signal the rise time and time constant α of the SSPC leakage circuit would need to be reduced significantly by either reducing the value of snubber capacitor C_s, or increasing the leakage current by reducing the value of resistors R_p and R_{lk}, which is not practical due to thermal dissipation issues. The SSPC output snubber components are designed to provide optimal electrical performance when the system is functioning correctly, therefore value changes to aid fault detection should traded against the other SSPC functional requirements such as EMI susceptibility and current limit control stability.

The plot showing $\frac{dV_{sspcout}}{dt}$ for the slowest SSPC output leakage voltage falling edge scenario presented in Figure 5.18 shows that the use of the backward difference derivative at 50kSPS provides signals up to a peak of -0.22V/μs. Applying a threshold at 0.05V/μs to this signal provides simple confirmation of a loose terminal open circuit fault. The plot illustrating $\frac{dV_{sspcout}}{dt}$ for the fastest SSPC output leakage voltage falling edge scenario presented in Figure 5.19 provides a signal peaking at -0.6V/μs, which is somewhat easier to detect than that slower falling edge scenario. If the mechanical vibration excitation was at a particularly high frequency then the magnitude of the derivative signal may be reduced further since the SSPC output voltage would not have sufficient time to climb between reconnection events, thus resulting in a

lower change in voltage during reconnection. This demonstrates again that the performance of the $\frac{dV_{sspcout}}{dt}$ detector could be improved further by reducing the value of the snubber capacitor C_s to increase the SSPC output leakage voltage rise time.

The series arc fault detection voltage monitor developed in Section 4.4 is biased at 1.5V and is inverted such that fast negative rates of change of SSPC output voltage are expressed as a voltage peak greater than 1.5V. The voltage monitor threshold is placed at ∼1.55V for series arc fault detection purposes, and the experimental results in Figures 5.18 and 5.19 show that the this threshold is sufficient to detect load reconnection when the SSPC output voltage is ≥5V prior to reconnection. The series arc fault detection voltage monitor is thus an additional option for detecting loose terminal faults.

The corresponding SSPC output / loop currents measured during load reconnection peak at 0.12A for the slowest test scenario and 0.58A for the fastest test scenario. The current peak experienced during reconnection of the load is proportional to the SSPC output leakage voltage prior to reconnection. The current peaks are of comparable magnitude to the step changes in current seen during arc strike under the 270VDC series arc fault scenarios tested in Section A.4 and therefore the series arc fault detection current monitor is well equipped to detect these transients.

The series arc fault detection current monitor developed in Section 4.3 is biased at 1.5V and is inverted such that fast negative rates of change of SSPC output voltage are expressed as a voltage peak greater than 1.5V. The current monitor is capable of detecting reconnection events for SSPC output leakage voltages in excess of 10V, and thus the current sensor is less sensitive than the voltage monitor. Using a similar approach to the passive electrical series arc fault detection system developed in Chapter 4, the voltage and current monitors can be combined to detect negative going voltages and positive going currents, which may provide a degree of immunity to EMI which appears on one sensor but not the other.

The time required to confirm a series fault or open circuit is based on the averaging time T_{avg} required by the moving average filter to reach the confirmation voltage level. A longer averaging time T_{avg} yields a more robust confirmation scheme since it will be more resilient against normal electrical system transients. An averaging time of 10ms rejects a majority of transient threats which last for less than 1ms. In the event that the leakage scheme is operated immediately after a series arc fault trip, it is critical that the series arc fault / open circuit fault is confirmed within the allowable 50ms power interruption window permitted under the power quality requirements in RTCA DO-160G [49]. Assuming that detection begins at time 40μs, Figures 5.18 and 5.19 show that during a loose terminal series fault the moving average signal crosses the 2V threshold within 37ms thus meeting power quality requirements. Further testing

is required to explore the effects of EMI on an open circuit SSPC output to determine what level of filtering is required to avoid nuisance trips.

The confirmation scheme presented herein has been demonstrated to provide a reliable method of detecting series wire faults on SSPC outputs. Electromechanical relays and contactors typically feature very low leakage currents when the device is open due to the presence of an air gap between the conductors. This isolation is highly desirable from a human safety perspective, however, very little leakage current is required to implement the proposed arc fault confirmation concept and, although it could be perceived as counter-productive, a leakage path could be introduced across such a device for arc fault confirmation purposes. A simple resistor provides a thermally stable leakage path which results in a controlled leakage current and hence a more deterministic arc fault confirmation solution. The arc fault confirmation scheme could also be implemented in 28VDC electromechanical and solid state electrical power distribution systems where leakage current levels are likely to be smaller than the 270VDC scenario due to the lower voltage stress applied to the switching devices.

5.4 Initiated Built-In Test (IBIT) Scheme

5.4.1 Theory and Predictions

The schematic in Figure 5.20 illustrates the model developed in Chapter 3 which has been tailored to allow simulation of the series arc fault detection Initiated Built-In Test (IBIT) algorithm.

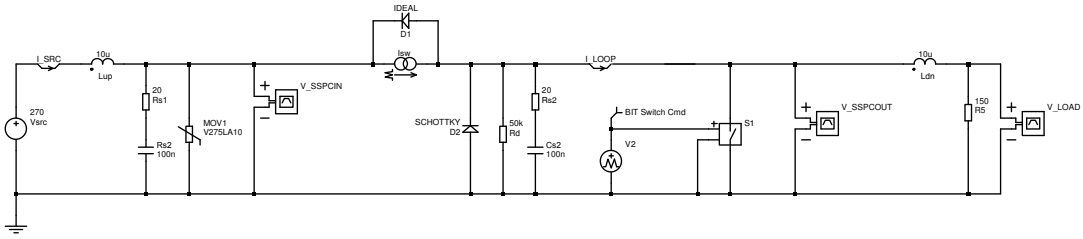


Figure 5.20: Schematic Illustrating the Initiated Built-In Test (IBIT) SPICE Model

The source voltage V_{src} was set to 270VDC and the SSPC has been simplified to behave as a simple current source I_{sw} with representative wire inductance values for the upstream L_{up} and downstream L_{dn} wire feeders, where it is assumed that wire resistance can be neglected. Transient suppression device MOV_1, input snubber $R_{s1} + C_{s1}$, output snubber $R_{s2} + C_{s2}$, flywheel diode D_2, anti-parallel diode D_1 and leakage discharge resistor R_d are fitted externally in order to allow flexible simulation. The "BIT Switch" S_1 is used to apply a low impedance to the output of the SSPC for test purposes. In order to simplify simulation, the model does not sense $\frac{dI_{loop}}{dt}$

and $\frac{dV_{sspcout}}{dt}$ to provide a closed-loop feedback to the IBIT system, but allows the author to prove that the $\frac{dI_{loop}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ signals are stimulated in accordance with the predictions. The results of this simulation are presented with the results of the physical experiment in Section 5.4.3.

Figure 5.21 shows a basic waveform representation for the series arc fault detection current/voltage monitor IBIT scheme.

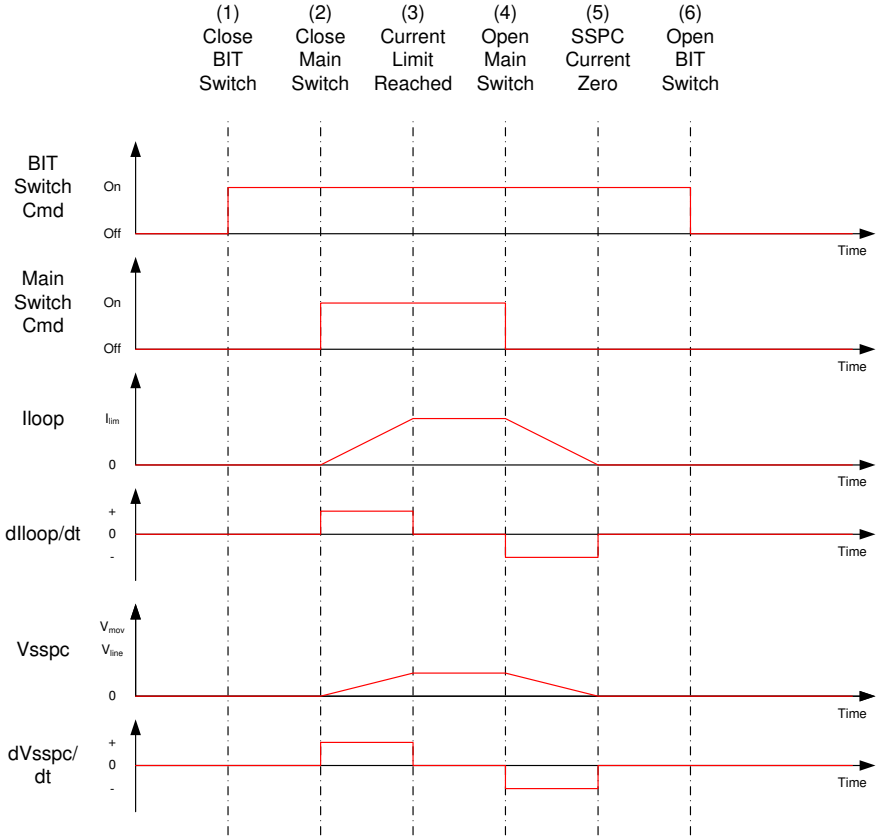


Figure 5.21: Series Arc Fault Detection Current/Voltage Monitor IBIT Sequence

To minimise nuisance trips due to manufacturing and installation errors it is important to monitor the two voltage and two current discrete input signals to ensure that no erroneous behaviour occurs prior to the start of the test at Point (1). At Point (1) the BIT switch is closed and a short time later, determined by the switching speed of the "BIT switch" and the cycle time of the microcontroller control software, at Point (2) the SSPC is closed thus triggering an increase in current at rate approximated by Equation (5.35).

$$\frac{dI_{loop}}{dt} = \frac{V_{src}}{L_{up}} \tag{5.35}$$

The increase in current creates a positive $\frac{dI_{loop}}{dt}$ event which is detected by the microprocessor and verifies operation of this positive current monitor function. In addition to this and somewhat less intuitively the current also creates a positive $\frac{dV_{sspcout}}{dt}$ event since in the PEPDC / PEPSC designs the minimum configurable current limit value for the 16 MOSFET SSPC is 250% of 120A rated current and for each MOSFET this gives a single MOSFET current limit $I_{limit,single}$ in accordance with Equation (5.37).

$$I_{limit} = 250\% \times 120 = 300A \tag{5.36}$$

$$I_{limit,single} = \frac{I_{limit}}{16} = \frac{300}{16} = 18.75A \tag{5.37}$$

The "BIT Switch" has non-zero on-resistance R_{bitsw} and in the case of the PEPDC / PEPSC design it is approximately $R_{bitsw} = 200\text{m}\Omega$. Equation (5.38) calculates the change in SSPC voltage $\Delta V_{sspcout}$ due to the increase in loop current up to the current limit.

$$\Delta V_{sspcout} = I_{limit,single} R_{bitsw} = 18.8 \times 0.20 = 3.8V \tag{5.38}$$

The 3.8V increase provides an ideal test case for the positive voltage monitor which is asserted between Points (2) and (3). Between Points (3) and (4) current limit is maintained until the SSPC is opened at Point (4). Opening the SSPC creates a decrease in loop current between Points (4) and (5) with a rate of change of current given by Equation (5.39), where V_f is the nominal forward voltage of flywheel diode D_2, and L_{pcb} is the parasitic loop inductance of the PCB tracking from the flywheel diode cathode to the "BIT switch" input, and from the flywheel diode anode to the "BIT switch" return.

$$\frac{dI_{loop}}{dt} = -\frac{V_f}{L_{pcb}} \tag{5.39}$$

The decrease in current asserts the negative current monitor between Points (4) and (5). The decrease in current also results in a decrease in voltage developed across the "BIT Switch" on resistance, thus causing assertion of the negative voltage monitor between Points (4) and (5).

At Point (6) the "BIT Switch" is opened to restore the SSPC to normal operation mode and the IBIT operation is complete. In the event that one of the four series arc fault detection current / voltage monitor logic signals is not asserted correctly during the test cycle, a series arc fault detection IBIT failure will be reported from the SSPC to the SSPM.

During the closed duration t_{bit} of the "BIT Switch" between Points (2) and (5), the power dissipation P_{bit} in the chosen device is given by Equation (5.40) and the energy transferred into the "BIT Switch" over the typical $t_{bit} = 60\mu$s is given by Equation

(5.41), assuming that the current rise and fall times are fast compared with the total IBIT cycle.

$$P_{bit} = I_{limit}^2 \times R_{bitsw} = 300^2 \times \left(200 \times 10^{-3}\right) = 18kW \tag{5.40}$$

$$Q_{bit} = P_{bit} t_{bit} = \left(18 \times 10^3\right) \times \left(60 \times 10^{-6}\right) = 1.08J \tag{5.41}$$

Since the PEPDC / PEPSC SSPCs perform a current limit during short circuit operation the main switching MOSFETs also undergo a temperature rise. Equation (5.42) describes the power dissipated in a single MOSFET P_{FET} out of N_{FET} total MOSFETs for a maximum power supply voltage $V_{src(max)}$ of 350V and a current limit at 250% of the 120A rated current given by I_{limit}. Based on a consistent IBIT test duration of $t_{bit} = 60\mu$s the energy dissipated in a single MOSFET can be calculated by Equation (5.43).

$$P_{FET} = \frac{V_{src(max)} I_{limit}}{N_{FET}} = \frac{350 \times 300}{16} = 6.562kW \tag{5.42}$$

$$Q_{FET} = P_{FET} t_{bit} = \left(6.562 \times 10^3\right) \times \left(60 \times 10^{-6}\right) = 393.7mJ \tag{5.43}$$

The temperature rise in the MOSFETs is limited by minimising pulse duration to 60μs which translates to a 50°C temperature rise, which is sufficient to ensure that each MOSFET does not exceed the maximum junction temperature based on maximum ambient temperature specifications.

5.4.2 Test Methodology for the Initiated Built-In Test (IBIT) Scheme

The electrical configuration of the Initiated Built-In Test (IBIT) scheme is given in Figure 5.22.

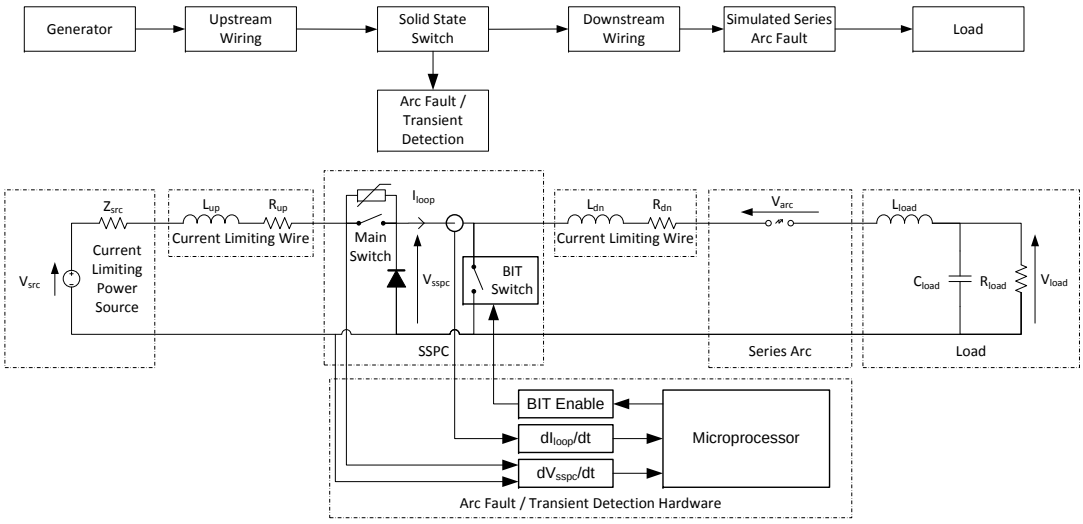


Figure 5.22: PEPDC/PEPSC Initiated Built-In Test (IBIT) Function

The block diagram in Figure 5.22 shows the configuration of a typical SSPC within a solid-state electrical power distribution system, and includes the arc fault detection capability developed in Chapter 4. The lower level schematic below the block diagram shows how a switch designated a "BIT Switch" can be switched in between the SSPC switch output and chassis return path by a microprocessor and associated software.

The "BIT Switch" first appeared in GE Aviation Systems Ltd Modular Power Tile (MPT) products as a method of testing the current limit function of SSPCs with multiple semiconductors fitted in parallel. This is achieved by shorting the "BIT Switch" and turning on each of the parallel semiconductors individually in sequence and verifying over a short time period that the semiconductor current does not exceed the preset limit. This scheme is implemented in the PEPDC and PEPSC products, and is covered by international patents [249; 250; 251; 252].

The scheme was later developed further to be used as a method of testing the presence and functionality of transient suppressors required for protection of SSPC hardware, such as the MOV connected across the SSPC / main switch depicted in Figure 5.22, where the SSPC is closed into a short circuit created by the "BIT Switch" thus charging the upstream cable inductance. When the SSPC is opened, shortly followed by the "BIT Switch", the upstream inductance is discharged into the transient suppressor, and the SSPC input / output voltage monitors are used to determine if the voltage across the transient suppressor is within the datasheet specification. This scheme is covered by international patents [245; 246; 247; 248].

Built-In Test was considered since the functionality of the passive electrical series arc fault detection current and voltage monitors, developed in Sections 4.3 and 4.4, is difficult to test unless a series arc fault is present in the system. To perform end-to-end testing of the planar current transformer circuit a real current has to flow through the SSPC busbar structure, and the opportunity to use the existing "BIT Switch" was identified. Similarly to perform end-to-end testing of the series arc fault voltage monitor circuit, a fast voltage variation has to be present at the input to the SSPC hardware. Voltage pulses can be injected into the voltage monitor resistor chains and current monitor amplifier stages for test purposes, but this requires significant additional hardware and does not verify operation of the complete detection system. The IBIT scheme therefore provides a simple and reliable method for end-to-end testing of the series arc fault detection current and voltage monitors in SSPCs without requiring a real series arc fault.

5.4.3 Experimental Results

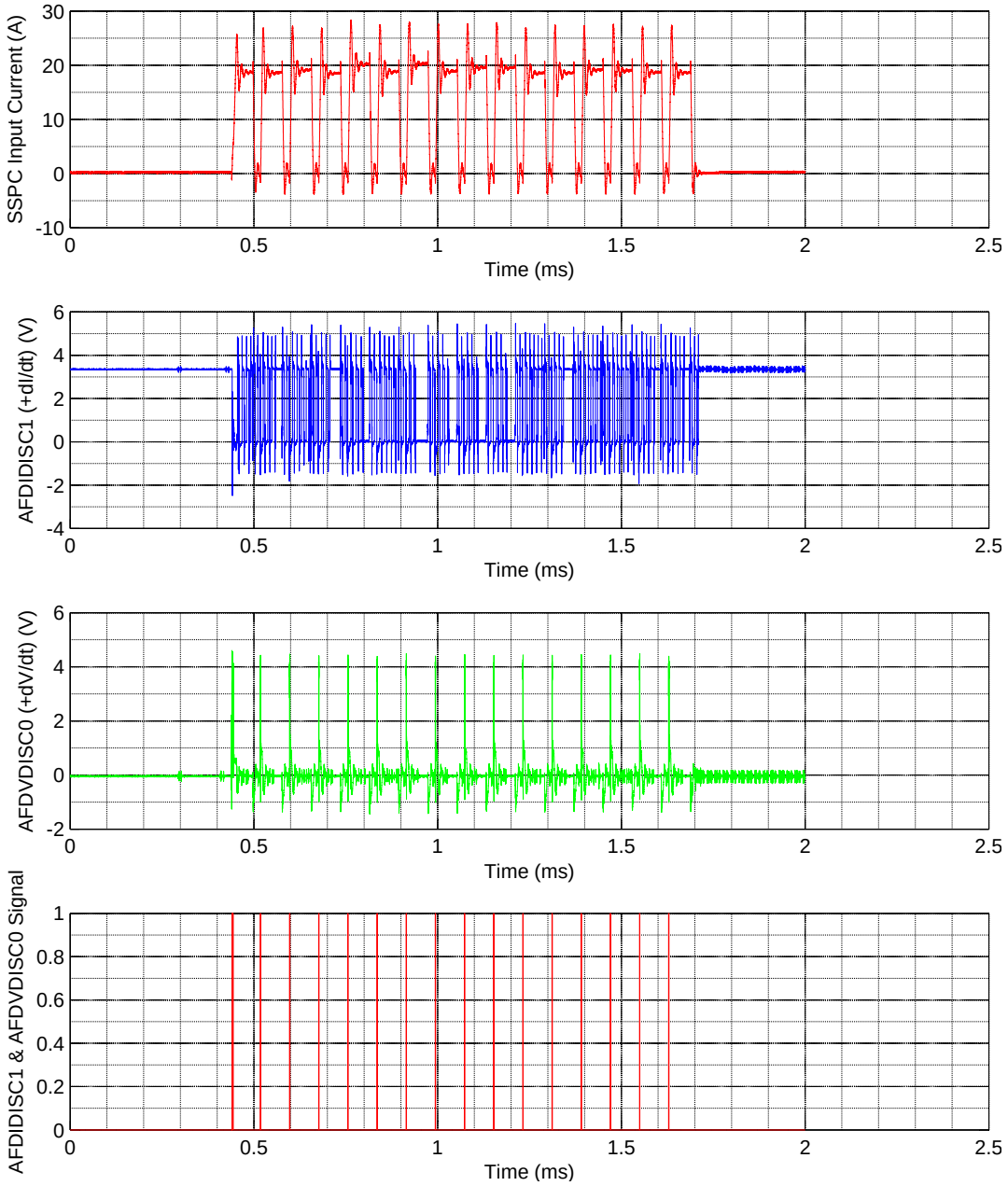


Figure 5.23: PEPDC / PEPSC IBIT Function Positive $\frac{dI_{loop}}{dt}$ / $\frac{dV_{sspcout}}{dt}$ Test Results

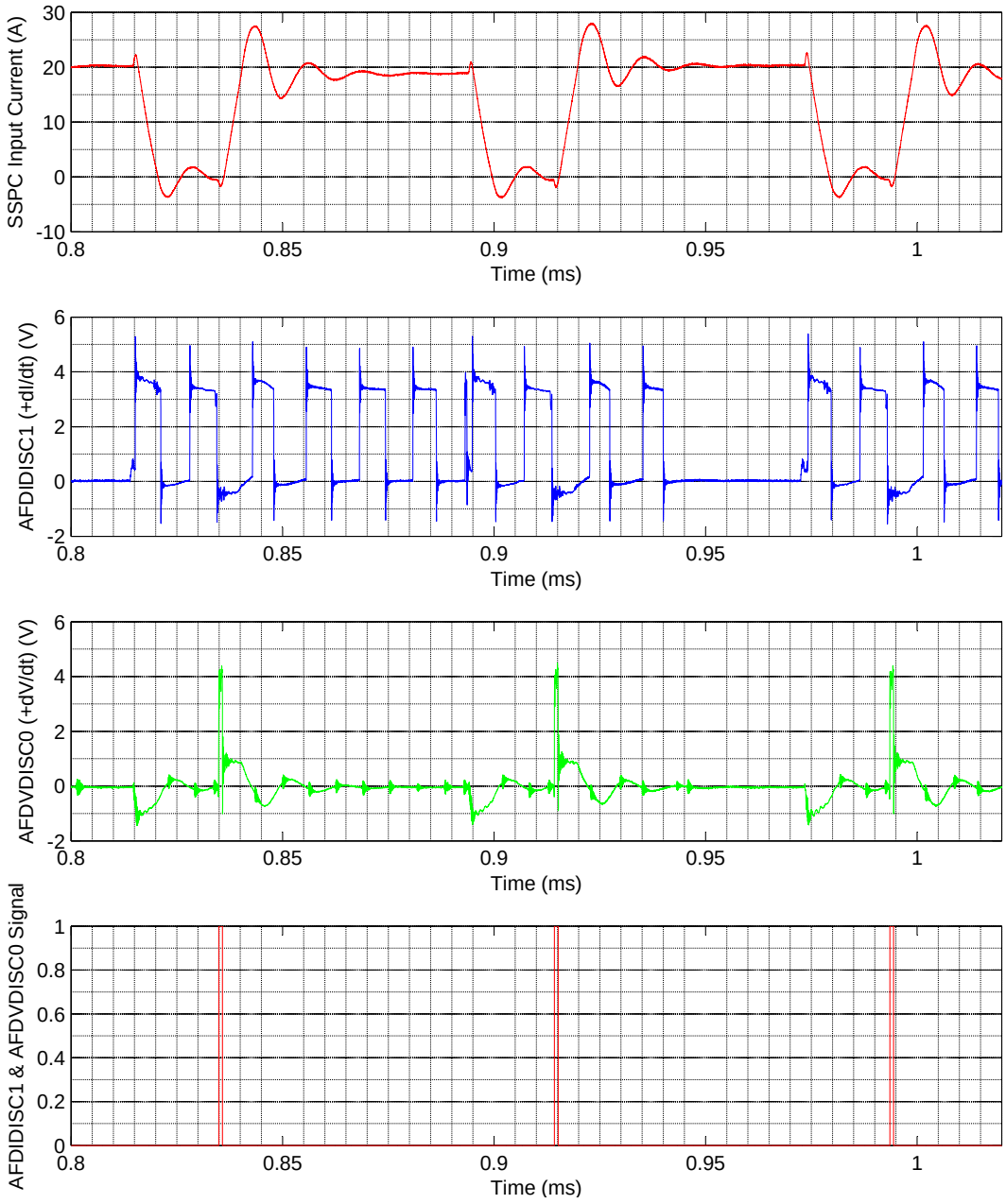


Figure 5.24: PEPDC / PEPSC IBIT Function Positive $\frac{dI_{loop}}{dt}$ / $\frac{dV_{sspcout}}{dt}$ Test Results (Detailed)

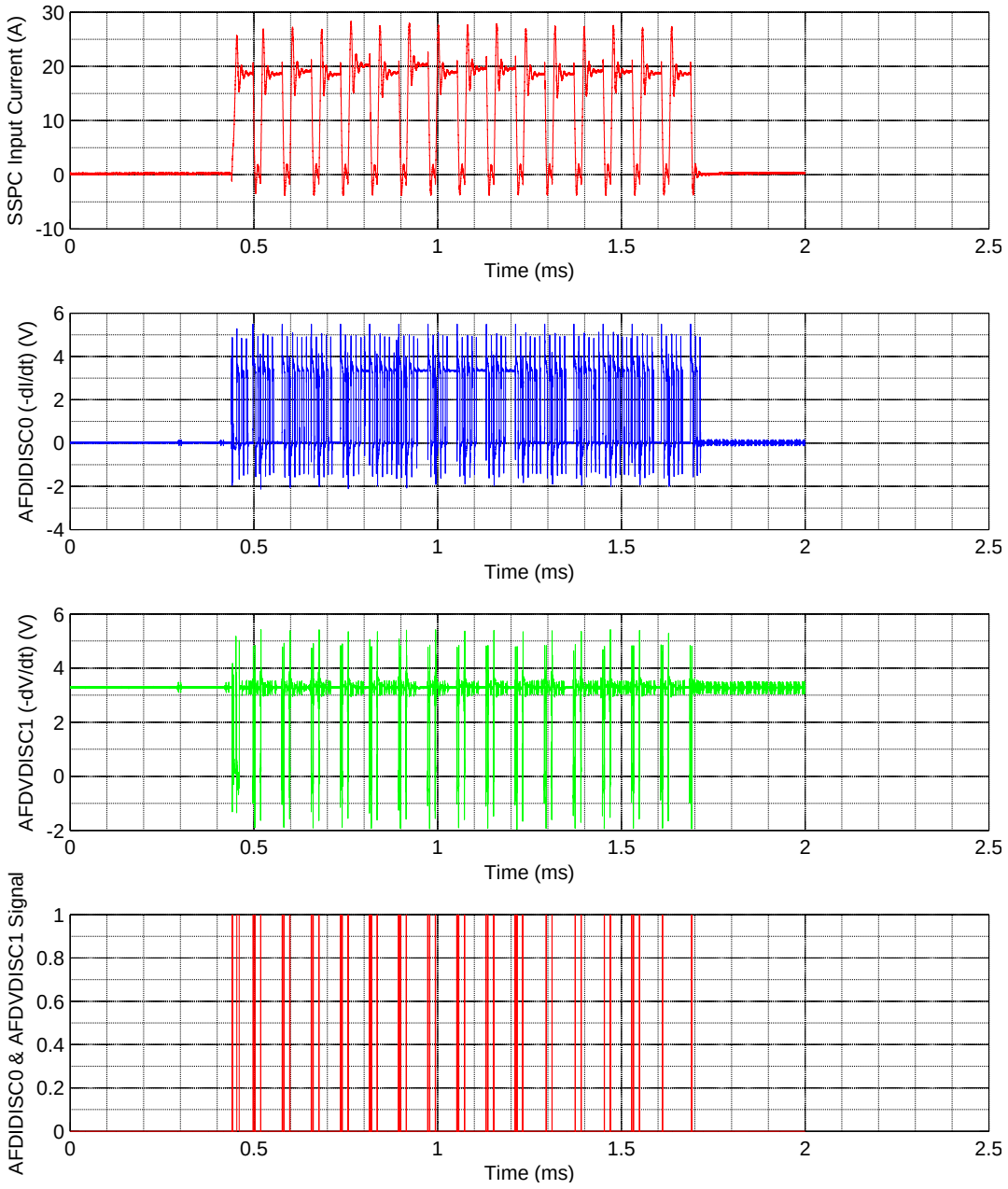


Figure 5.25: PEPDC / PEPSC IBIT Function Negative $\frac{dI_{loop}}{dt}$ / $\frac{dV_{sspcout}}{dt}$ Test Results

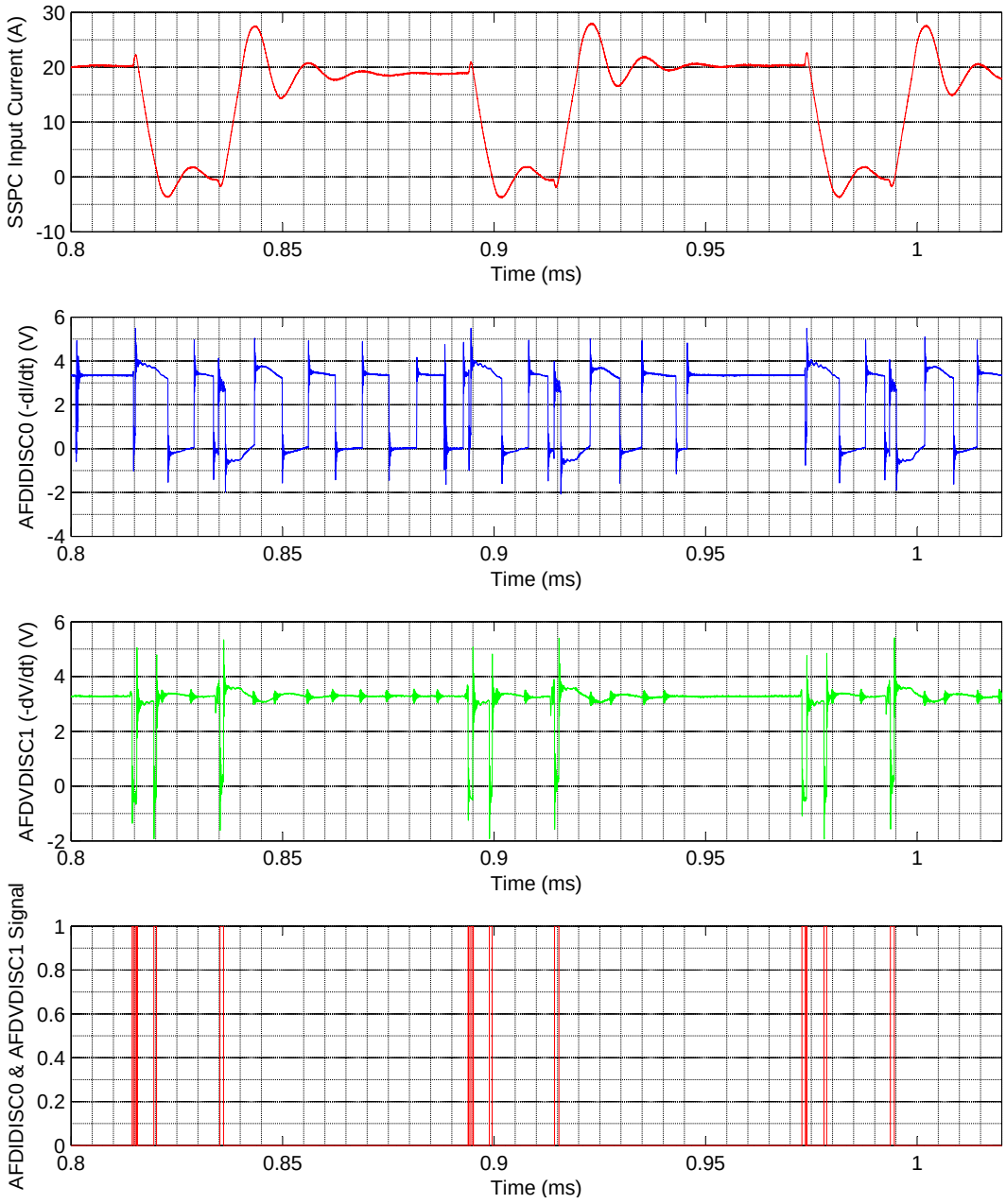


Figure 5.26: PEPDC / PEPSC IBIT Function Negative $\frac{dI_{loop}}{dt}$ / $\frac{dV_{sspcout}}{dt}$ Test Results (Detailed)

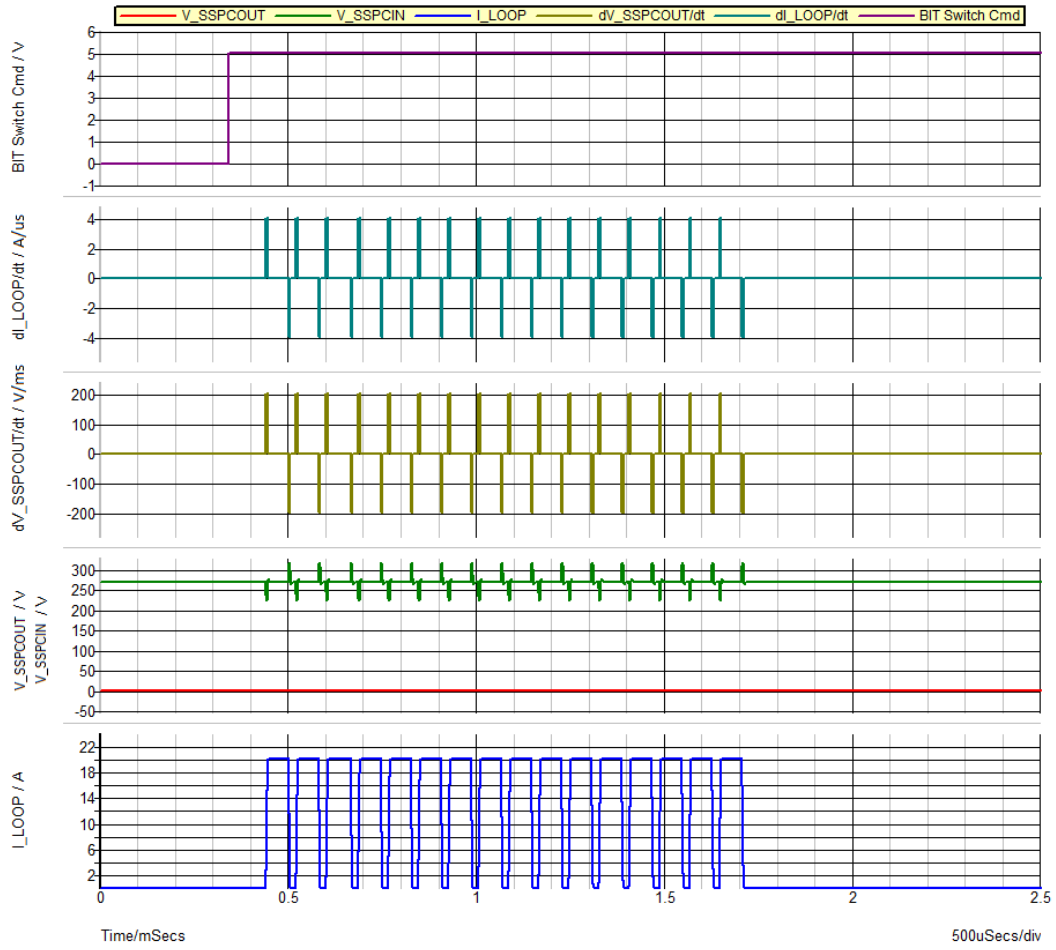


Figure 5.27: Plot Showing Results of the IBIT Function SPICE Simulation

5.4.4 Discussion

Figures 5.24 and 5.26 show the results of operating the IBIT scheme outlined in Section 5.4.2. It should be noted that both Figures 5.24 and 5.26 show three iterations of the IBIT scheme described in Section 5.4.2, but 16 iterations in total were completed as part of the standard PEPDC / PEPSC IBIT process in order to test each of the 16 parallel MOSFETs, where the full cycle of testing can be seen in Figures 5.23 and 5.25.

Prior to initiation of the IBIT scheme the series arc fault detection system is in steady-state, and the four discrete logic signals AFDVDISC0 (Positive $\frac{dV_{sspcout}}{dt}$ Event), AFDVDISC1 (Negative $\frac{dV_{sspcout}}{dt}$ Event), AFDIDISC0 (Negative $\frac{dI_{loop}}{dt}$ Event), and AFDIDISC1 (Positive $\frac{dI_{loop}}{dt}$ Event) are not asserted. For further clarification of signal names and the full current and voltage monitor configurations under test, please refer to Appendices C.7 and C.8 respectively. The absence of signals during this time

can be monitored by the microprocessor to ensure that there is no instability in the current and/or voltage monitor hardware, and that the steady-state active low states for the four signals are correct. Erroneous steady-state behaviour leads to nuisance trips during normal operation.

Figure 5.24 shows how the AFDIDISC1 (Positive $\frac{dI_{loop}}{dt}$ Event) and AFDVDISC0 (Positive $\frac{dV_{sspcout}}{dt}$ Event) discrete logic signals are asserted in response to a positive going $\frac{dV_{sspcout}}{dt}$ event during the rising edge of the SSPC input current waveform at times 0.835ms, 0.915ms and 0.995ms, and this result aligns with the predicted operation of the IBIT scheme presented in Section 5.4.1. At these times the AFDIDISC1 (Negative $\frac{dI_{loop}}{dt}$ Event) discrete logic signal indicating a positive-going $\frac{dI_{sspcout}}{dt}$ event is also asserted in error. This occurs because the 18.8A current switched during operation of the IBIT scheme is significantly higher than the maximum change in loop current $\Delta I_{loop(max)}$ seen in a 270VDC system during a series arc strike event. The maximum change in loop current $\Delta I_{loop(max)}$ during a series arc strike event can be calculated in Equation (5.44), assuming the SSPC is supplying the full rated load current $I_{load(max)} = 120$A and the arc voltage is $V_{arc} = 15$V .

$$\Delta I_{loop(max)} = \frac{V_{arc}}{V_{sspcout}} I_{load(max)} = \frac{15}{270} \times 120 = 6.7A \tag{5.44}$$

The high current during IBIT causes the planar current transformer to resonate, leading to the erroneous detection of both positive and negative $\frac{dI_{loop}}{dt}$ events. This issue is also compounded by the low threshold setting of the comparator which thresholds the analogue signal from the current transformer circuit. This is not an issue for IBIT testing purposes because only the instantaneous response around the rising edge of input current is of interest and all other pulses can be ignored.

Figure 5.24 also shows the result of a boolean AND operation between AFDVDISC0 (Positive $\frac{dV_{sspcout}}{dt}$ Event) and AFDIDISC1 (Negative $\frac{dI_{loop}}{dt}$ Event) which provides a pulse during each of the three rising edges in the SSPC input current waveform. The first part of the IBIT test operation is classified as successful if each rising edge in the IBIT current waveform results in an output pulse from the AND operation, thus verifying the functionality of the AFDIDISC1 and AFDVDISC0 signals. The outcome of the test depicted in Figure 5.24 is therefore successful.

Figure 5.26 illustrates how the AFDIDISC0 (Negative $\frac{dI_{loop}}{dt}$ Event) and AFDVDISC1 (Negative $\frac{dV_{sspcout}}{dt}$ Event) active low discrete logic signals are asserted in response to a negative-going $\frac{dV_{sspcout}}{dt}$ event during the falling edge of the SSPC input current waveform at times 0.815ms, 0.895ms and 0.975ms, and this result verifies the predicted operation of the IBIT scheme presented in Section 5.4.1. At these times the

AFDIDISC0 (Positive $\frac{dI_{loop}}{dt}$ Event) active low discrete logic signal is also asserted due to resonance in the planar current transformer, as discussed previously. Figure 5.26 also shows the result of a boolean AND operation between NOT AFDVDISC0 (Negative $\frac{dV_{sspcout}}{dt}$ Event) and NOT AFDIDISC1 (Negative $\frac{dI_{loop}}{dt}$ Event), which is asserted during each of the three rising edges of the SSPC input current signal. The second part of the IBIT test operation is classified as successful if each falling edge in the IBIT current waveform results in an output pulse from the AND operation, thus verifying the functionality of the AFDIDISC0 and AFDVDISC1 signals. The outcome of the test depicted in Figure 5.26 is therefore successful.

The results of the IBIT scheme SPICE simulation are presented in Figure 5.27 and show the result of testing each of the 16 MOSFETs fitted to both the PEPDC and PEPSC designs, where the current limit for each MOSFET is set to 18.8A. In similarity with the experimental data, the rising edges of the IBIT current waveform result in positive $\frac{dI_{loop}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ events, and conversely the falling edges of the IBIT current waveform result in negative $\frac{dI_{loop}}{dt}$ and $\frac{dV_{sspcout}}{dt}$ events. These results show an ideal $\frac{dI_{loop}}{dt}$ response, where the high magnitude IBIT current pulses do not excite resonances in the planar current transformer, and therefore the model could be improved further by modelling the resonant behaviour of the planar current transformer in SPICE.

The results show that the IBIT scheme functions in accordance with the concept waveforms in Figure 5.21. However, the peak current limit of 18.8A causes a resonance in the current monitor circuit which could lead to erroneous results, and therefore a lower current limit should be investigated for stable IBIT testing, where ideal test waveforms have been simulated in Figure 5.27. This work has successfully demonstrated a proof-of-concept for the IBIT scheme which can be incorporated into the final PEPDC / PEPSC SSPC hardware.

5.5 Chapter Summary

5.5.1 Series Arc Fault Perturbation/Confirmation Scheme

The work described in Section 5.2 has demonstrated that recent developments in fast switching SSPC technology for aircraft can provide fast power supply modulation that may be used for series arc fault detection and/or confirmation. The approach was initially devised using a theoretical approach, simulated using MATLAB® and SPICE, and finally demonstrated by practical implementation of the arc fault perturbation scheme in an SSPC, where testing was carried out with a loose terminal series arc fault.

It has been shown that turning off the SSPC during a series arc fault and monitoring arc quenching behaviour in the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ can be used as a method of detecting or confirming the presence of series arc faults in high voltage DC systems. The initial analysis and simulation predicted that an interruption time of 57μs would cause series arcs to quench for load currents up to 25A with total downstream inductances up to 150μH. A software controlled SSPC was programmed to open the SSPC for 100μs on detection of a possible arc series fault, and the feasibility of this approach was tested with loads in the range 2.5A through 7.5A.

Experimental and simulation data showed that the arc quench event created a fast $\frac{dI_{loop}}{dt}$ event, and this was detected by the series arc fault series arc fault current sensor and reported the the SSPC. Series arcs did not quench until current zero for load currents over 7.5A because the SSPC output flywheel diode commutates the switch-off current, indicating that the energy stored in the output inductance dominates the energy stored in the SSPC output snubber selected for the trial. The snubber capacitance could be increased to maintain consistent arc quench behaviour at higher current and inductance levels. However, increased snubber capacitance may detriment SSPC current limit performance, and result in higher power dissipation due to typical ripple voltages at the SSPC input.

A controlled 100μs SSPC interruption time was chosen for the perturbation scheme, and the period between interruptions was maximised to prevent impact on the power quality seen by aircraft loads and the EMC emissions created by the system. If the duration of a series arc in the loose terminal scenario is less than the 100μs SSPC interrupt time then this results in a missed detection. It was shown that there is a $\sim$10% probability that the duration of a series arc in the loose terminal scenario is less than the 100μs SSPC interrupt time, therefore the arc fault confirmation sequence should be run multiple times to minimise missed detections.

It has been shown that monitoring the delay between re-closing the SSPC and load current rising can be used to determine whether an arc was present between the SSPC and load. For load currents between 2.5A and 25A this technique was more reliable than observation of the arc current discontinuity encountered during arc quench.

A perturbation / confirmation scheme was demonstrated which can be used as a primary or secondary method of series arc fault detection / confirmation in high voltage DC electrical power distribution systems. A further area to explore is a polling scheme whereby the perturbation scheme is run periodically, since each 100μs interruption has little effect on the power quality specified in RTCA DO-160G [49], providing that the repetition rate is kept low. Unlike the repetitive transients seen during a loose terminal fault, it was shown in Section 3.3 that drawn arcs feature

fast arc voltage and loop current transients only during arc strike, thus making them difficult to detect reliably. Running the perturbation scheme periodically would allow drawn arcs to be detected and quenched in addition to those created in a loose terminal scenario, thus reducing the reliance on detecting fast voltage/current transients alone. Non-linear and active loads such as switched mode power supply loads should also be investigated since these behave similarly to series arc fault near current zero, and could result in nuisance trips.

5.5.2 Series Arc Fault Confirmation Using SSPC Leakage Scheme

The work described in Section 5.3 identified that SSPCs suffer with undesirable leakage currents, unlike traditional electromechanical devices which feature air gap isolation. It was predicted that SSPC leakage current could be used as a method of detecting series wire faults. An equivalent schematic and mathematical model were developed for the SSPC leakage current and SSPC output leakage voltages to predict the interaction with series wire faults.

The step response characteristics of the SSPC output leakage voltage waveform were derived, which allowed a series arc fault confirmation algorithm to be realised. The SSPC output voltage step responses were modelled as a first order time domain equation, where faster SSPC output voltage rise times were found be achieved by increasing the SSPC leakage current or by reducing the size of the SSPC output snubber capacitor C_s. SSPC output voltage fall times presented a more complex problem when considering reactive loads, and a SPICE simulator was used to simulate this behaviour. It was shown that the slowest SSPC output voltage fall time between the load connection at time zero and the SSPC output leakage voltage reaching a 0.5V threshold is approximately 0.7ms under a 1A resistive load scenario. The worst case fall time is two orders of magnitude faster than the worst case rise time of 38.4ms. The rise time is heavily dependent on SSPC temperature and input voltage where lower SSPC temperatures and input voltages reduce the SSPC leakage current, which prevents the SSPC output snubber capacitor from being charged quickly.

The series arc fault confirmation scheme was experimentally demonstrated using a PEPDC SSPC and loose terminal series fault. It was demonstrated by monitoring and thresholding a moving average of the SSPC output leakage voltage that a series wire fault could be easily detected. A moving average filter was required to avoid nuisance fault detection as a result of normal electrical system voltage transients. The scheme was demonstrated in the time domain with the lightest (1A resistive load) and heaviest (500μF$\|$1A resistive) load scenarios, which allowed the effectiveness of the $\frac{dV_{sspcout}}{dt}$ detector to be evaluated. A simple backward difference derivative was sufficient to detect $\geq$ 5V SSPC output leakage voltage reconnection events in the main SSPC voltage monitor. It was also shown that the passive electrical series arc fault detection

voltage monitor developed in Section 4.4 was capable of detecting the $\geq$ 5V SSPC output leakage voltage reconnection events, and could be used as an alternative to the backward difference derivative calculation, thus removing computational load from the SSPC microcontroller. The results revealed that the passive electrical series arc fault detection current monitor developed in Section 4.3 was less effective at detecting reconnection events, where SSPC output leakage voltages $\geq$ 10V were required.

This study has a major impact where the leakage monitoring scheme can be expanded to run continuously when the SSPC is open. This allows detection of series wire faults prior to closing of the SSPC, thus providing series arc fault prevention and improved health monitoring capability.

5.5.3 Series Arc Fault Detection BIT Scheme

The literature showed that there is a need to perform Built-In Testing (BIT) to verify functionality of each semiconductor in a given SSPC. One method to achieve this is to short circuit the output of the SSPC with another semiconductor, and then switch on each semiconductor in the SSPC into the short circuit for a short duration. It was predicted that the current and voltage signals generated by this testing could be used to test the series arc fault current and voltage monitors developed in Section 4.3 and 4.4 respectively during aircraft installation, thus increasing reliability and availability of the system, and reducing nuisance trips caused by faulty hardware.

The theory behind the scheme was outlined in Section 5.4.1 in the form of a sequence diagram. The model developed in Section 3.4 was then modified to include the BIT hardware, and was used to simulate the proposed IBIT scheme. The simulation results in Section 5.4.3 showed that the rising and falling edges of the IBIT current waveform could be used to stimulate the series arc fault current and voltage monitors.

The IBIT scheme was then demonstrated with the physical PEPDC SSPC hardware, where test results are given in Section 5.4.3. The results showed that the passive electrical series arc fault current and voltage sensors were triggered during the test in accordance with the theoretical prediction and simulation results. It was found that the large magnitude of the current test signal caused the current monitor signals to oscillate after the initial pulse was received, and while this oscillation behaviour was not ideal, this behaviour did not affect the outcome of the IBIT test.

The IBIT scheme outlined in this chapter has been successfully demonstrated to provide an Initiated Built-In Test (IBIT) solution for the series arc fault detection scheme presented and tested in Chapter 4. The scheme also provides a new avenue of further work to explore IBIT functionality for series and parallel arc fault detection in both AC and DC electrical power distribution systems.

Chapter 6

Conclusions and Further Work

6.1 Conclusions

The main goal of this thesis is "The characterisation, modelling, simulation and detection of series arc faults in aircraft electrical power distribution systems featuring Solid State Power Controllers (SSPCs)". To satisfy the main thesis goal ten objectives were identified in Section 1.8, where each objective was fulfilled throughout the thesis as discussed below.

During the introduction of this thesis series arc faults in the Electrical Wiring Interconnect System (EWIS) were highlighted as a particular threat to high voltage electrical power distribution systems because series arc fault currents fall within the normal operating range of typical aircraft thermal circuit breakers with I^2t overcurrent protection. Series arc faults are also more difficult to detect than parallel arc faults since they create a lesser impact on the signals in a given electrical power distribution system. From these findings it was concluded that without series arc fault detection capability, series arc faults could continue unabated causing damage to the aircraft wiring and structure, thus providing a significant motivation for this work.

The review of literature highlighted that there are many and various series arc fault test and detection methods available. The SAE5692/SAE6087 loose terminal test method was found to be the preferred series arc fault detection method for aerospace due to its simple and repeatable nature [8; 255].

The arc fault detection methods from the literature were broadly split into passive and active methods where active detection methods were considered prohibitive due to their high cost, weight, volume and complexity. Although active reflectometry techniques such as SSTDR [178] have been successful in detecting 28VDC and 115VAC series arc faults, these systems rely on arc quench to develop a sufficient impedance discontinuity for the reflectometry system to detect and locate the offending fault.

Since 270VDC series arc faults do not quench readily, these active reflectometry techniques were neglected from study.

Passive series arc fault detection methods such as acoustic [86; 87; 88; 89; 90; 91; 92; 93], visible light [97], ultraviolet light [96], and ionisation methods [98; 99] were also deemed unsuitable or difficult to implement for aerospace applications since they are neither modular, scalable nor cost effective. It was concluded that passive electrical schemes provided simple, modular, scalable and low cost series arc fault detection solutions. However, these were found to be susceptible to nuisance trips because they were either too sensitive, or the authors had not reviewed the fundamental arc physics and behaviour prior to definition of the detection method.

The use of passive electrical frequency domain detection methods such as FFT [134; 136; 137; 139; 140; 142; 144], STFT [68; 145; 146] and wavelet analysis [147; 148; 149; 150; 151; 152; 153; 154; 155; 156; 157; 158] for series arc fault detection was widespread in the literature. These methods all focussed on implementing complex pattern recognition without relating the arc physics or the wider system configuration to the series arc fault waveforms under scrutiny. Failure to consider the qualitative aspects of series arc fault detection systems results in the inability to produce a verifiable and aerospace certifiable engineering solution. It can be concluded that to develop a considered series arc fault detection system, the fundamental arc physics and interaction of the series arc fault with the wider electrical power distribution system must be understood.

By studying arc physics literature it was determined that the striking and quenching of the series arc fault manifested transient arc current behaviour that the many passive electrical time domain detection methods in the literature were capable of detecting. It was concluded that passive electrical time domain methods offered the most scalable, modular and cost effective solution to loose terminal series arc fault detection, but these were limited to 28VDC [103; 121; 126] and 115VAC [106; 107; 108; 113; 115; 118; 128] operation only and did not consider the interaction of the series arc fault with the SSPC electronics present in modern solid state electrical power distribution systems. It was therefore necessary to characterise 270VDC series arc fault current behaviour in solid state electrical power distribution systems such that a 270VDC passive electrical time domain series arc fault detection solution could be realised for the PEPDC and PEPSC SSPC hardware modules.

During the characterisation activity a loose terminal 270VDC series arc fault simulator was built and the arc voltages, loop currents, SSPC output voltages and load voltages for each scenario were analysed in Section A.5. It was demonstrated that arc voltage is line voltage invariant, and thus in 28VDC and 270VDC systems with a 15V arc voltage, the load voltages are reduced to 13V and 255V respectively during a

series arc fault. It was concluded from these findings that in contrast to the 28VDC case, the 270VDC load voltage falls within the RTCA DO-160 Section 16 power quality specification for normal operation during the series arc fault. The impact of the series arc fault on load operation is therefore minimal, and the fault will continue to cause damage to the EWIS and aircraft structure unabated [49].

The results also highlighted that the rate of change of loop current during series arc strike is proportional to the arc voltage to total loop inductance ratio, and since arc voltage is line voltage invariant, the rate of change of current during series arc strike is comparable for both 28VDC and 270VDC faults. However, the change in loop current during typical 28VDC and 270VDC series arc strike events is 54% and 5.6% respectively, assuming an arc voltage of 15V. It was concluded that development of a series arc fault current monitor capable of detecting ∼5.6% changes in SSPC loop current down to load current levels of 5A is a challenging task because existing SSPC current monitors do not provide the dynamic range required for series arc fault detection, and thus a dedicated current sensor was required.

It was found that a voltage pulse appears on the SSPC output voltage during arc strike, and that this voltage is proportional to the arc voltage multiplied by the ratio of upstream inductance to total loop inductance. Since arc voltage is line voltage invariant, it was concluded that the magnitude of the voltage pulse is similar for both 28VDC and 270VDC systems, therefore a common series arc fault voltage monitor can be used. The rise time of the SSPC output voltage pulse was measured at ∼1μs and the pulse duration was found to be a similar order of magnitude, therefore the existing SSPC voltage monitors were unable to provide a sufficient bandwidth and sampling rate to detect this feature and thus a dedicated voltage sensor was required.

Although the effect of inductive and capacitive loads on series arc fault behaviour had been studied by Müller et al in AC systems, Strobl and Meckler highlighted that there was little literature available regarding the effect of such loads in DC systems [80; 68]. The analysis of the effect of reactive load behaviour in Section A.5 revealed that series arc faults in both 28VDC and 270VDC circuits are unstable when the total system loop inductance is low, and in conclusion the introduction of load inductance and additional SSPC upstream and downstream wiring improves arc stability and allows arcs to continue burning unabated. The impact of this discovery is that series arc faults in both 28VDC and 270VDC systems are of concern and not just the perceived worst case in 270VDC systems. Conversely, it was concluded that the introduction of a capacitive load causes series arcs to quench immediately after arc strike in both 28VDC and 270VDC systems due to the inability of the total loop inductance to maintain a sufficient arc voltage across the arc electrodes to sustain a stable arc. The capacitance level required to achieve this is modest with 40μF being sufficient to enable arc quenching at 270VDC with resistive load currents up to 25A.

While this feature makes series arc faults in 270VDC systems much easier to detect, there is an industry trend to reduce the capacitance of electrical loads because this can drive a requirement for larger generators capable of withstanding high inrush currents, and can cause electromagnetic interference issues during power on. However, it is likely that future aircraft loads will retain some level of input capacitance due to the requirement for hold-up energy during power interruptions, and thus the use of a minimum capacitance for such loads should be considered as an aid to passive electrical series arc fault detection.

The distribution of arc periods and arc durations were analysed in each test scenario during the characterisation activity, along with the arc strike, quench and reconnection voltage distributions. Capacitive loads were found to reduce both the arc durations and periods due to spot welding of the arc electrodes during contact reconnection. It was also found that the loose terminal test method limited loop currents to $\leq$25A since higher currents caused spot welding of the arc electrodes and therefore experimental testing up to 25A was carried out. It was concluded that the distribution of arc duration and period data can vary wildly for different fault types, mechanical / electrode configurations, and electrical load configurations, thus creating a complex detection problem. The impact of this finding is that series arc fault detection designers must consider the corner cases for the overall electrical system before selecting the appropriate arc fault classifier.

The investigation into modelling of the series arc fault scenario determined that a SPICE model was most appropriate since this facilitated simple integration with the existing top-level SSPC hardware model. It was found that electric arc behaviour could be easily modelled in SPICE using a simple modified Nottingham static V-I arc model [9], where energy balance equations such as those of Cassie and Mayr were rejected since they did not accurately model arc quench behaviour [212; 213]. Since the standard Nottingham model exhibits asymptotic arc voltage behaviour as arc current tends to zero, a maximum arc voltage and minimum arc leakage current was assumed to allow convergence of the SPICE simulation. This assumption implies that the simulation is not accurate for very small currents, but this was not an issue for the test scenarios presented in this thesis since load currents of less than 1mA are of little interest. The simulation results of the SSPC-based distribution system presented in Section 3.5 correlated well with the experimental results from the characterisation activity, and in conclusion the bottom-up analysis of the series arc fault physics and wider electrical system yielded a good quantitative model of loose terminal series arc fault behaviour. The implication of this result is that requirements for current / voltage based series arc fault detection systems can be derived from simulations of the corner cases for a given application, and such simulation results were used to develop the voltage invariant arc fault detection system presented in Chapter 4.

It was suggested in the literature that passive series arc fault detection methods suffer from nuisance trips, and it was also found that a 270VDC passive series arc fault detection system had not been attempted. The author therefore decided to explore the limitations of a novel passive electrical 270VDC series arc fault detection system before attempting to minimise nuisance trips using other techniques. The system requirements for a passive electrical line voltage invariant series arc fault detection system, presented in Section 4.2, were synthesised from the characterisation activity results discussed in Section A.5. The system requirements highlighted that dedicated series arc fault current and voltage monitors are required to realise a passive electrical 270VDC series arc fault detection system based on SSPC loop current and SSPC output voltage behaviour.

A trade study was conducted on a range of possible series arc fault current monitors where cost, weight, volume, sensitivity and high DC current withstand requirements were analysed, and it was concluded that a Rogowski coil implementation was most favourable. A multi-layer PCB-instantiated Rogowski coil was developed and tested where it was found that the sensitivity of the structure was sufficient to detect series arc faults down to loop current levels of 5A, and the air cored nature of the coil was not susceptible to the SSPC maximum steady state current capability. The discussion in Section 4.8 observed that series arc fault strike caused the current sensor to resonate. The impact of this resonance is that the current sensor is susceptible to radiated EMI, and in conclusion the interlayer capacitance of future multi-layer PCB current sensor designs should be minimised further to increase resonant frequency and thus measurement bandwidth.

A simple RC differentiator circuit was developed to provide SSPC output voltage pulse detection and to minimise the cost and complexity of the series arc fault voltage monitor. The results showed that the voltage sensor was capable of detecting series arc faults in systems with loop currents down to 5A, and a minimum upstream-to-total inductance ratio of $\sim$30%. The implication of using SSPC output voltage monitoring for series arc fault detection is that the physical positioning of the SSPC module within the aircraft affects the detection performance of the voltage monitor, and suggests that the SSPC cannot be mounted close to the generator or other power source since there may be insufficient upstream inductance and thus SSPC output voltage signal to enable detection.

The outputs from the developed series arc fault current and voltage monitors were fed into the existing PEPDC and PEPSC microcontrollers, where a software confirmation algorithm enabled series arc faults to be confirmed. Both leaky integrator and statistical profiling schemes were proposed as candidate software confirmation algorithms. It was decided that the leaky integrator approach was most appropriate due to the simple, configurable and easily verifiable functional operation. In conclusion it

is possible to detect and confirm series arc faults in 270VDC systems under a range of different source, resistive load, reactive load and wiring configurations within 2.5s using passive current / voltage monitoring and simple leaky integrator confirmation, thus allowing fault isolation before significant damage to aircraft wiring and structure can occur. This result implies that series arc faults can be detected in 270VDC systems without the need for complex and high cost active detection technologies.

The majority of available active series arc fault detection schemes highlighted in the literature focussed on the use of reflectometry schemes such as the highly robust Spread Spectrum Time Domain Reflectometry (SSTDR), where pulses of energy are transmitted through the wire under test and any faults cause reflections proportional to the associated impedance discontinuity, which are captured and processed by the reflectometry equipment, thus enabling fault presence and location to be determined. It was concluded that reflectometry techniques rely on high impedance discontinuities (i.e. open or short circuits) for wire fault detection and, based on the characterisation activity discussion in Section A.5, these were found not to exist during 270VDC series arc faults. Typical active arc fault detection methods are also comparably expensive compared with their passive counterparts due to the requirement for additional expensive and power hungry hardware. The implication of this conclusion is that active methods only provide benefit where they have the opportunity to minimise nuisance trips and/or improve detection sensitivity compared with the passive electrical series arc fault detection scheme developed in Chapter 4.

Nuisance trip behaviour was discussed during the literature review in Section 2.9, where it was concluded that it is not possible to achieve a nuisance trip rate of zero in abstract passive or active series arc fault detection systems. In the case of passive series arc fault detection systems it was proposed that to achieve a zero nuisance trip rate the series arc fault detection system would need to perfectly classify series arc fault behaviour over the full electrical system operating range, where this is unlikely since series arc fault behaviour has been demonstrated to be inherently chaotic and unrepeatable [6; 33; 65; 164]. Since it is not known when a series arc fault will occur, the series arc fault detection system needs to monitor the electrical system under test continuously, which increases the probability of a nuisance trip event. Similarly active detection systems cannot achieve a zero nuisance trip rate due to the same issue of series arc fault classification. However, it is proposed that the correlation of action and response in an active system reduces the probability of nuisance trips significantly because continuous asynchronous system monitoring is not required.

It was concluded from the literature that nuisance trips are a risk regardless of the chosen series arc fault detection method, and that active detection techniques held the key to minimising nuisance trips. Many researchers demonstrated sensor fusion to reduce nuisance trips, where multiple passive and/or active detection methods are

combined to realise a more reliable detection system [194; 195; 196; 197; 198; 199]. Nemir et al proposed an active method of reducing nuisance trips where a tripped circuit is re-closed after a short delay in order to provide power to the load between intermittent arc fault interruptions [65]. This research inspired the author to develop the novel arc fault confirmation and perturbation scheme presented in Section 5.2, which uses SSPC modulation as an active method of arc fault detection.

The proposed series arc fault perturbation scheme makes use of solid state switching speed, which is several orders of magnitude faster than that of historical electromechanical switching. Building on the known active arc fault detection schemes, the author developed a series arc fault perturbation scheme which firstly uses the passive electrical series arc fault detection technique discussed in Section 4.8 to detect the presence of a series arc fault. After a loose terminal series arc fault is passively detected, on the next arc strike the SSPC is subsequently opened in order to interrupt the arc prior to arc electrode reconnection. By interrupting the burning arc it was demonstrated that the arc could be artificially quenched, where the resultant SSPC loop current waveform exhibited the normal characteristic exponential decay followed by a step reduction in current due to arc quench at a rate that far exceeds the natural electrical system response. This step reduction in current occurred at the quench current of approximately 400mA regardless of the load resistance. The series arc fault perturbation scheme underwent integration testing on the PEPDC SSPC, where the step reduction in current during arc quench was found to be registered by the series arc fault current monitor developed in Section 4.3, thus giving confirmation that a series arc fault was present. In conclusion interrupting a burning series arc by opening the SSPC provides an effective method for confirmation and perturbation of loose terminal series arc faults in systems, where series arcs do not quench under typical fault conditions, thus resulting in reduced nuisance trips and improved system availability without adding any further hardware to the SSPC.

The series arc fault and wider electrical system models developed in Section 3.4 were configured to operate the theoretical arc fault perturbation algorithm developed in Section 5.2.1, and a simulation of the series arc fault perturbation scheme was run, where the simulation results were found to correlate with the experimental results. In conclusion the series arc fault SPICE model provides a simple tool for validating future series arc fault detection, confirmation and perturbation methods before committing them to physical hardware. The impact of this finding is a reduction in development time for future arc fault detection systems.

During development of the series arc fault perturbation scheme it was observed that the SSPC output voltage did not decay to zero following arc quench as expected, and this anomaly prompted a study into the interaction of the series arc fault and the inherent SSPC leakage current present when the SSPC is open. It was concluded

that series arc faults could be identified by monitoring the SSPC output voltage both during operation of the arc fault perturbation scheme, and also continuously while the SSPC is commanded open. This enables the detection of open circuit load and open circuit downstream feeder faults which can propagate into series arc faults when the SSPC is subsequently closed. The finding implies that, in addition to confirmation of series arc faults, series arc faults can be prevented by detecting high impedance SSPC loads, which are characteristic of an open circuit downstream feeder or open circuit load. This was achieved by monitoring SSPC output voltage using the existing SSPC output voltage monitor hardware, thus providing a simple, reliable and cost effective method of series arc fault detection, confirmation and/or prevention.

The review of nuisance trip literature in Section 2.9 highlighted an additional area for study where malfunction or failure of the series arc fault detection current and voltage monitor hardware, developed in Sections 4.3 and 4.4 respectively, due to manufacturing, assembly or installation errors could lead to nuisance trips. To protect against this type of failure an Initiated Built-In Test (IBIT) function was developed to allow maintenance staff to quickly and easily test the series arc fault detection current and voltage monitors after the solid state electrical power distribution panel has been installed on the aircraft. The IBIT scheme was experimentally validated on the PEPDC SSPC hardware and uses the existing BIT pulldown MOSFET used for main semiconductor testing [249; 250; 251; 252] to create series arc-like current and voltage transients to trigger the arc fault detection system, therefore no additional hardware was required to implement this function. It was concluded that the functionality of the series arc fault detection system can be quickly confirmed in the end user's application, thus eradicating the possibility of nuisance trips due to manufacturing, assembly or aircraft installation errors.

In conclusion the findings of the loose terminal series arc fault characterisation, modelling, simulation and detection in aircraft electrical power distribution systems featuring SSPCs have been presented and discussed herein, thus meeting the thesis aim and objectives. The author hopes that the work provided in this thesis will contribute to the delivery of a safe high voltage DC solid state electrical power distribution system for the next MEA/AEA, which is protected from the hazardous electrical arcing that resulted in the losses of many aircraft as described in Section 1.6.1.

6.2 Novel Contributions

The doctoral work presented in this thesis contains seven novel contributions to knowledge which are discussed below. While the author was unable to publish academic papers in these areas due to commercial sensitivity, patents were filed to secure Intellectual Property (IP) rights on five of these topics in accordance with Section 1.10, thus demonstrating both the originality and value of this work.

1. Reactive Load Behaviour With 270VDC Series Arc Faults

The literature review identified that there was a gap in knowledge where 270VDC series arc fault behaviour was not fully understood. Strobl and Meckler similarly identified that the effect of reactive loads on series arc faults in both 28VDC and 270VDC systems was not fully understood [68]. The interaction of SSPC electronics with series arc faults was similarly not documented. This thesis characterises the behaviour of 28VDC and 270VDC series arc faults in representative aircraft electrical power distribution systems, and perhaps more importantly their interaction with the typical solid state SSPC. In addition to this the impact of inductive and capacitive loads and system wiring on series arc fault behaviour in 28VDC and 270VDC systems has been presented. A full summary of the findings can be found in Section A.6.

2. Series Arc Fault Modelling and Simulation

Limited literature on arc fault modelling was found where Andrea et al presented the main reference in this area regarding AC arc fault modelling in MATLAB using energy balance arc models [32]. Andrea et al performed experimental validation of their model using a non-aerospace test method and therefore additional work was required. The author identified a gap in knowledge, where modelling the interaction of SSPC electronics with series arc faults as part of the wider electrical system model provides the ability to determine the impact of series arc fault behaviour more accurately and also the ability to validate series arc fault detection systems prior to realising physical hardware. In this thesis a novel series arc fault model was developed and integrated with an SSPC and wider electrical power distribution system model. The associated simulation results correlate well with the experimental results gathered in the thesis. This model enables future simulation work on both high voltage AC and DC arc faults in solid state electrical power systems, and also enables different passive electrical time domain series arc fault detection, confirmation and perturbation schemes to be trialled. A full summary of the findings can be found in Section 3.7.

3. 270VDC Series AFD Using PCB-Instantiated Rogowski Coil

Existing literature showed that toroidal Rogowski coils had been used for a passive electrical time domain series arc fault detection application in 28VDC and 115VAC systems, and that glass wafer based micro-fabricated current sensors had been used with some success for partial discharge detection in aircraft wiring [256]. Existing PCB-instantiated Rogowski coils were found to be complex and bulky since they contained multiple separate PCBs arranged radially [257]. To produce a low cost, high sensitivity solution capable of simple integration with existing SSPC hardware, the author developed a multi-layer PCB-instantiated Rogowski coil which was implemented and tested under varying 270VDC series arc fault scenarios with great success. A full summary of the findings can be found in Section 4.9 of this thesis. Patents have been published for the novel PCB-implemented coil design in Canada,

China, Germany and the United States under CA 2,813,933 A1, CN 103,384,446 A, DE 102,013,104,286 A1 and US 8,842,398 B2 respectively [50; 51; 52; 53].

4. Series Arc Fault Confirmation/Perturbation Using SSPC Modulation
Building on the work of Nemir and Beck who presented an arc fault management strategy based on switch modulation in their 2004 paper [65], the author developed and experimentally validated a series arc fault perturbation technique that allows confirmation of series arc faults by interrupting the series arc after arc strike and observing the subsequent arc current characteristics for a negative rate of change of current faster than that of the natural system response. This technique is particularly novel and is an area which has not received a great deal of research since the majority of work on arc fault detection has been carried out on AC electromechanical AFCB / AFCI devices, where the switching speed is insufficient to realise such a perturbation scheme. A full summary of the findings can be found in Section 5.5 of this thesis. A patent has been filed for the series arc fault confirmation / perturbation scheme under GE Disclosure: 33811 / Docket Number: 268868.

5. Series Arc Fault Confirmation Using SSPC Leakage Current
A novel and undocumented field of series arc fault prevention was identified which exploits the use of SSPC leakage current and corresponding SSPC output voltage for identification of high impedance loads at the output of the SSPC, which are indicative of loose terminal faults that can lead to series arc faults when the SSPC is closed. A series arc fault confirmation scheme using SSPC leakage current and monitoring SSPC output voltage was proposed and experimentally validated, where a full summary of the findings can be found in Section 5.5. A patent has been filed for the series arc fault confirmation / perturbation scheme under GE Disclosure: 62939 / Docket Number: 282149.

6. Series Arc Fault Initiated Built-In Test (IBIT) Scheme
Tyler and Collins presented a method of testing the health and functionality of semiconductor devices in multi-semiconductor SSPCs by firstly using an additional semiconductor switch to short the output of the SSPC to chassis, and secondly turning on each of the main semiconductor switching devices in turn into the low impedance circuit, thus enabling the semiconductor devices to be tested [249; 250; 251; 252]. The author built on this method by observing that turning on the semiconductor devices causes a well-defined transient current to flow through the SSPC, as well as a corresponding voltage transient on the SSPC output which provides an ideal test signal for the passive electrical time domain series arc fault detection system. The novel Initiated Built-In Test (IBIT) scheme was experimentally validated and a full summary of the findings can be found in Section 5.5. A patent has been filed for the Built-in-Test Method for Arc Fault Detection Hardware scheme under GE Disclosure: 44999 / Docket Number: 265352.

7. Bifurcated Method of Arc Fault Detection and Location, Using Series Arc Fault Perturbation Technique and TDR/FDR/STDR/SSTDR
Following on from the development of the arc fault perturbation scheme a bifurcated method of arc fault detection and location was conceived which enables active reflectometry-based arc fault location schemes to detect the location of series arc faults in high voltage systems by artificially increasing the impedance discontinuity at the series arc fault location by quenching the arc. This scheme has not been experimentally validated due to resource limitations and has been recommended as a future work activity and outlined in Section 6.3. A patent has been filed for the bifurcated method of arc fault detection and location, using arc fault perturbation technique and TDR/FDR/STDR/SSTDR under GE Disclosure: 55075 / Docket Number: 274954.

6.3 Limitations and Areas for Further Work

During the course of this research a number of limitations were identified, where the areas of future work to address these are presented below. The further work commences with incremental improvements to the concepts proposed in this thesis, and concludes with further work in the wider field of arc fault detection.

1. Develop High Current Series Arc Fault Test Equipment
The first and perhaps most fundamental limitation in the doctoral work is that the SAE AS5692 compliant loose terminal series arc fault scenario used for experimental characterisation of series arc faults did not provide series arcing above arc current levels of 25A due to spot welding which prevented the arc electrodes from vibrating and producing the desired arc phenomena. It was assumed during development of the passive electrical series arc fault detection system that if a series arc fault detection system functions correctly at 25A, the signal levels produced by 120A series arcing would be proportionally greater and thus easier to detect. An area for future work is therefore the development of a 120A capable series arc fault simulator, which would enable the series arc fault detection, confirmation and perturbation schemes developed in Chapters 4 and 5 of this thesis to be fully tested in a laboratory environment.

The analysis phase of the series arc fault characterisation activity was limited by the isolated differential voltage probe, used for measuring the voltage across the arc electrodes, which influenced arc behaviour by providing an alternative path for arc current through the probe impedance. The isolated differential probe introduced a differential impedance of 10MΩ in parallel with 10pF across the arc electrodes. The isolated differential voltage probe and data acquisition system were electrically decoupled from mains earth to minimise the impact of the common-mode probe impedance on the arc and this approach worked successfully. In conclusion during arc quench the high arc voltage and low arc current led to inconsistent and inaccurate arc quench

voltage measurements due to the differential mode probe impedance. Arc voltage inaccuracy was further exacerbated during arc quench by aliasing due to the short duration of the arc quench phenomena and the relatively low sample rate. A data sampling rate of 100MSPS was selected since this was the fastest sampling rate that allowed continuous recording, and thus in future work a higher sampling rate should be considered for arc quench voltage monitoring.

Characterisation of the SSPC output voltage transient encountered during arc strike indicated that the magnitude of the transient was proportional to the ratio of upstream-to-total system inductance, and a limitation was identified here where it was not possible to provide a sufficiently low aircraft-representative inductance between the power source and the SSPC, and between the SSPC and the load due to the baseline laboratory inductances which are constrained by the physical positioning of equipment within the facility. Hence another limitation of this work is that it was carried out in an aircraft systems integration laboratory and not on a representative aircraft platform, therefore further work is required to address this.

2. Explore Series Arc Fault Progression Over Time

A further limitation of the characterisation activity was that data captured for each test scenario was limited to three seconds due to the storage and processing overheads of large data sets, which exceeded one TeraByte. More than two hundred series arc events were captured during each test scenario, with the exception of the extreme 100μH / 380μF resonant / capacitive load scenario, and this was an acceptable test duration. However, the test duration could be increased further to determine how series arc faults change over time as localised wiring damage occurs.

3. Exploit Arc Fault Model for Simulation of Parallel Arc Faults

Modification of the series arc fault SPICE model to simulate parallel arc faults would be beneficial since parallel arc faults represent very high energy events which cause instantaneous damage to the mechanical environment. This activity would require further work on characterising the interaction between the mechanical and electrical domains.

A limitation of the series arc fault model developed in this thesis is that it is not capable of representing the near-infinite arc voltage encountered as arc current tends to zero during arc quench. Similarly the model is unsuitable for simulation of very low arc currents below 100mA due to the assumption regarding a minimum arc current. While these features are not a problem for the research carried out in this thesis, the assumption of a minimum arc current and maximum arc voltage must be considered when taking this model forward into future work.

4. Optimise SSPC Snubber Networks for Series Arc Fault Detection
The primary requirement of the snubber networks at the input and output of the PEPDC and PEPSC SSPCs is that of line and load feeder impedance stabilisation during SSPC switching. Additional conflicting requirements for the snubber networks were identified in this thesis since snubber components limit the rate of change of SSPC output voltage during arc strike, thus making arc strike more difficult to detect. Later during the arc fault perturbation scheme development it was identified that higher capacitance snubber networks allowed series arcs to quench more readily when the SSPC is opened thus allowing confirmation of the fault. Further work is therefore required in order to optimise snubber networks to fulfil these three requirements, while considering that the snubber networks are also dependent on the nominal SSPC current rating.

A complimentary area of future work is the opportunity to dynamically switch the input / output snubber networks in and out during SSPC operation. The snubber networks are only required for open / close of the given SSPC during normal operation, operation of protective trip functions such as I^2t, and operation of the series arc fault perturbation scheme. During the remaining time the input / output snubber networks could be switched out of circuit, allowing a larger voltage to be developed at the SSPC output in response to a downstream series arc fault, thus making series arc faults easier to detect.

5. Optimise the Passive Series Arc Fault Detection System
The novel series arc fault current monitor multi-layer PCB-implemented Rogowski coil design developed in Section 4.3 provides excellent detection of series arc strike events. However, there is a limitation that inter-winding capacitance between every other PCB layer reduces the self-resonant frequency of the coil structure, thus reducing the self-resonant frequency, reducing bandwidth and preventing positive and negative $\frac{dI_{loop}}{dt}$ events from being discriminated. Future work would seek to minimise inter-winding capacitance further by increasing PCB thickness to allow such discrimination.

The series arc fault voltage monitor design developed in Section 4.4 functions well, and despite optimising the bandwidth of the series arc fault voltage monitor for series arc fault detection, the voltage monitor is limited by its susceptibility to noise on the aircraft bus. This is further aggravated by the presence of the SSPC snubber components which limit the $\frac{dV_{sspcout}}{dt}$ experienced on the SSPC output voltage during arc strike, thus preventing the series arc fault voltage monitor high-pass cut-off frequency from being increased to avoid such noise. Further work is therefore required to test with aircraft representative power sources to determine if this behaviour is caused by the laboratory testing configuration.

Nuisance trip robustness of the developed series arc fault detection, confirmation

and perturbation techniques has not been explored since it is impractical to test this negative requirement, and thus nuisance trips have been discussed purely theoretically in Section 2.9. An important area of further work is characterising the crosstalk behaviour between an arcing conductor and non-arcing conductor(s), to prevent this from causing nuisance trips across multiple switched outputs.

6. Evaluate Fluxgate Current Sensor Technology for Series AFD
Following the development of the series arc fault current sensor presented in Section 4.3.3 and shortly after the time of writing, Mohat and Hopper of Texas Instruments demonstrated a fluxgate current monitor device formed as a semiconductor wafer fabrication that can be mounted into a slotted busbar [258]. Due to the simple method of fabrication this is a physically small and cost effective current monitoring technique which may be useful for providing current monitoring in future series arc fault detection schemes, and thus requires further investigation.

7. Explore Bifurcated Method of Arc Fault Detection/Location, With Series Arc Fault Perturbation and SSTDR
The series arc fault perturbation scheme allows series arc fault events to be identified by opening the SSPC when the series arc is burning. Based on this invention a bifurcated method of series arc fault detection and location was conceived which enables active reflectometry-based arc fault location schemes to detect the location of series arc faults in high voltage systems by artificially increasing the impedance discontinuity at the series arc fault location by quenching the arc. Further work is required to evaluate the capability of existing reflectometry schemes, and in particular to investigate the maximum achievable arc fault location distance based on the maximum round-trip time of the reflectometry system constrained by the nominal 100μs SSPC power interruption window.

8. Explore Polling Using the Series Arc Fault Perturbation Technique
The arc fault perturbation scheme is limited by an assumption that the minimum series arc duration is 100μs, which was estimated from the characterisation activity in Appendix A. The experimental results for the series arc fault perturbation / confirmation scheme were limited to a resistive load study due to limited resources, and therefore the interaction between the capacitive load arc quench behaviour observed during the characterisation activity and the series arc fault perturbation / confirmation system has not been fully explored.

A further area to explore is a system where the series arc fault perturbation scheme is run periodically using a polling scheme. This is possible since each interruption has little impact on the power quality specified in RTCA DO-160G [49]. Running this scheme periodically would also allow drawn arcs to be detected and quenched as well as those created in a loose terminal scenario, thus removing the need for detection

of fast voltage / current transients. Further input would be required from airframers regarding the acceptability of transient EMC emissions created by such a scheme.

9. Complete Qualification, Certification and Aircraft Testing

Due to the military nature of existing 270VDC electrical systems, there were no non-ITAR fully aircraft-representative generators or active / passive loads that could be compliantly tested during this research. Following the successful integration testing presented in this thesis, which has been carried out in a laboratory environment, there is a desire to complete full qualification and certification of the proposed series arc fault detection system to realise a commercially exploitable product. This would further allow the series arc fault detection, confirmation and perturbation schemes to be tested on a flight test platform with representative generators, power converters, wiring and loads, thus providing further validation of the work carried out in this thesis. Furthermore the arc fault perturbation scheme in particular requires approval from the aircraft systems integrators and airframers before deliberate power interruptions can be introduced for series arc fault perturbation / confirmation purposes.

10. Develop a +/-270VDC Series Arc Fault Detection System

The main body of this thesis has focussed on providing a solution to 270VDC series arc fault detection since there is an immediate requirement for a robust solution in this area. The thesis introduction identified that future aircraft electrical power systems are likely to feature high voltage +/-270VDC electrical power distribution, and looking to the future further research is required in order to apply the analysis, modelling, simulation, detection, perturbation and confirmation techniques developed in this thesis to the development of a robust +/-270VDC series arc fault detection system for the More Electric and All Electric Aircraft (MEA/AEA).

11. Explore Series Arc Fault Detection, Perturbation and Confirmation / Leakage Schemes in AC Systems

The final area of further work covers a wide spectrum and it is thus proposed that the passive series arc fault detection, perturbation and confirmation schemes developed in this thesis are applied to the problem of high voltage series arc fault detection in AC electrical power distribution systems such as the 230VAC system currently deployed on the Boeing 787 platform [13]. It is envisioned that this future work would form a similar doctoral thesis to that provided herein and would cover series arc fault characterisation, modelling, detection, perturbation and confirmation, along with an analysis of the effects of SSPC leakage currents on series arc faults in AC systems.

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Appendix A

Electrical Characterisation of Series Arc Faults in Aircraft Electrical Power Distribution Systems

A.1 Introduction

A.1.1 Background

From the literature review it was determined that wire faults are of great concern in aircraft electrical power distribution systems and have undergone significant research where NASA in particular delivered the vitally important "ageing aircraft" study. This research revealed that there are a number of possible wiring failure modes including damaged connectors, chaffed wires, cut wires, connector pin failures, corroded wires, shorted wires, splice failures and terminal lug failures [259]. These wire faults could go undetected until a failure occurs and could lead to series arcing resulting in localised damage, or propagation into the more destructive parallel arc fault. It was concluded that passive arc fault detection systems can cause nuisance trips, and that one possible reason for this is that the arc physics are not fully understood during selection of the series arc fault classifier. Development of an active detection scheme was recommended to resolve this, but before engaging in this expensive task it is necessary to fully characterise 270VDC series arc fault electrical behaviour in a typical aircraft power distribution system to explore the possibility of passive detection.

Strobl and Meckler described the behaviour of drawn electric arcs in aircraft DC power networks, where the research presented covers drawn arc behaviour and not the repetitive "loose terminal" scenario covered by SAE AS5692 and SAE AS6019 [68]. These studies investigated arc current, arc voltage, arc power and arc energy

for drawn arcs under varying source voltage conditions, where higher voltage DC arcs were found to burn more stably at lower current levels [68]. Strobl and Meckler identified that further work is required on 270VDC systems since distribution voltage levels in aerospace, automotive and industrial applications are set to climb as electrical power demand increases. This chapter aims to build on the work of Strobl and Meckler by investigating the behaviour of 270VDC loose terminal induced series arc faults.

When considering the effect of series arc faults on aircraft electrical distribution systems it is also important to understand the interaction between reactive loads and the system under test. Müller et al analyse the effect of inductive and capacitive loads on arc faults in aircraft AC power networks [80], however neither the effect of these loads on DC systems nor the loose terminal scenario are considered. Whilst these results are interesting, the papers cover a small subset of possible supply and load conditions and are not explicitly taken from representative systems using Solid State Power Controllers (SSPCs) which will influence system arcing behaviour. The research presented in their first paper covers drawn arc behaviour and not the repetitive loose terminal arcing covered in this chapter, and the test conditions vary between tests. The work presented in this chapter aims to expand on the work of Müller et al by considering the effect and interaction of inductive and capacitive loads on 270VDC electrical power distribution systems.

A.1.2 Hypothesis

The hypothesis underpinning this experiment is that if a series arc is introduced into a representative aircraft electrical power system, the SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ will be deflected such that these parameters can be employed in a method of passive electrical arc fault detection, and as a basis for the validation of a series arc fault electrical model.

A.1.3 Aims and Objectives

The aims of this chapter are firstly to determine whether SSPC loop current I_{loop} and SSPC output voltage $V_{sspcout}$ can be used in order to detect series arc faults downstream from a given SSPC within solid state aircraft electrical power distribution systems, and secondly to build a quantitative understanding of the effect of series arc faults on solid state aircraft electrical power distribution systems in the presence of varying resistive, inductive and capacitive load conditions.

The main objectives of this chapter are therefore firstly to emulate a representative "loose terminal' series arc fault scenario, secondly to capture loop current I_{loop} and SSPC output voltage $V_{sspcout}$ under varying source voltage, resistive/reactive loads and wiring configurations, and finally to characterise the system electrical behaviour so that a passive series arc fault detection system can later be derived in Chapter 4.

A.2 Theory and Predictions

A.2.1 Review of Static Arc Characteristics

In order to predict and understand series arc fault behaviour the electric arc models should be reviewed. The static V-I (Voltage-Current) equations which characterise electric arcs have been the subject research over many years, beginning with the work of Ayrton and Steinmetz in the late 19$^{\text{th}}$ and early 20$^{\text{th}}$ century [67; 95]. Ayrton presented Equation (A.1):

$$V_{arc} = A + B\ell + \frac{C + D\ell}{I_{arc}} \tag{A.1}$$

where V_{arc} is the arc voltage, I_{arc} is the arc current, ℓ is the arc length and A, B, C and D are constants. Constant A represents the cathode and anode fall voltages, $B\ell$ the voltage drop in the arc column, and $(C + D\ell)/I_{arc}$ the inverse characteristic of the arc. Nottingham demonstrated that Ayrton's equation was valid for constant arc lengths up to 15mm, and produced a new equation, given by Equation (A.2).

$$V_{arc} = A + \frac{B}{I_{arc}^{n}} \tag{A.2}$$

where A and B are constants dependent upon the arc length and electrode materials, and n was demonstrated to be directly proportional to the absolute temperature of the boiling point of the anode material [224]. Nottingham also shows that for longer arcs the Ayrton equation, Equation (A.1) can be modified to give Equation (A.3)

$$V_{arc} = A + B\ell + \frac{C + D\ell}{I_{arc}^{n}} \tag{A.3}$$

Peelo studies the history of arc equations and illustrates how many researchers developed this basic equation and extracted the parameters A, B, C, D and n in an attempt to validate their experimental data for a range of application specific scenarios [224]. A graphical representation of electric arc characteristics between copper electrodes in open air is presented by Sölver and is given in Figure A.1 [3].

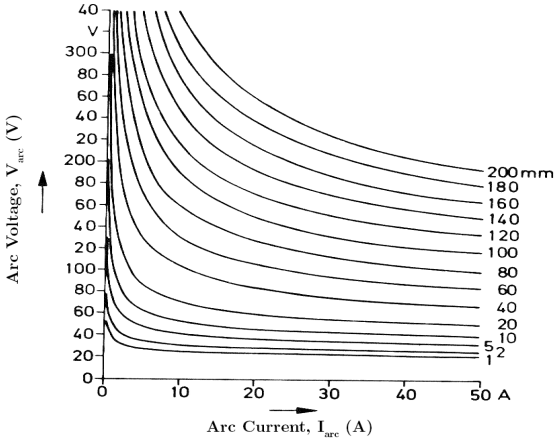


Figure A.1: V-I Characteristics of Open-Air Arc with Copper Electrodes [3]

To understand the behaviour of series arc faults in aircraft electrical power systems it is important to note in Figure A.1 that for a constant arc current I_{arc} when arc length ℓ increases, the arc voltage V_{arc} increases.

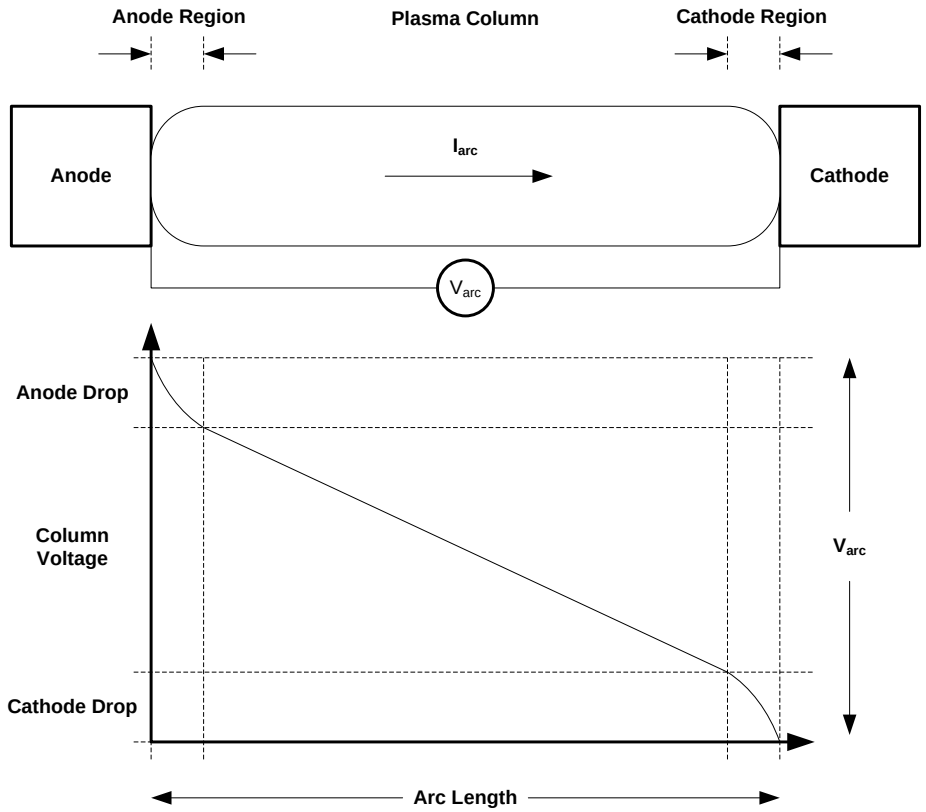


Figure A.2: An Illustration of the Distribution of Arc Column Voltage Drop [3; 4; 5; 6]

It is well understood that a typical arc column voltage is comprised of the anode drop, column voltage and cathode drop as indicated in Figure A.2 [3; 4; 5; 6]. As an arc increases and decreases in the length the arc column voltage increases and decreases respectively, but for short arcs the arc column voltage is negligible and the arc voltage V_{arc} consists of the anode and cathode voltage drops only. This is further illustrated in Figure A.1 where for short arcs of length less than ∼1mm and arc currents I_{arc} above 5A the arc voltage becomes invariant with respect to arc current and tends to a value near the sum of the anode and cathode voltage drops.

As arc current I_{arc} decreases the arc voltage V_{arc} increases in order to maintain the arc. The graph in Figure A.1 is valid for stable arcs burning in open air and demonstrates the negative differential impedance behaviour of electric arcs, but for arcs in representative aircraft electrical power systems it is likely that arc current will vary due to both load behaviour and the effect of reactive circuit elements within the system. The graph also does not show the point at which the arc strikes or quenches and instead shows an asymptote at zero arc current.

A.2.2 Typical DC Solid State Power Distribution Schematic

In order to predict the behaviour of the loose terminal series arc fault the typical DC SSPC test schematic in Figure A.3 must first be considered. This test schematic was derived by the author as a simple and configurable schematic which can be used for experimentation purposes.

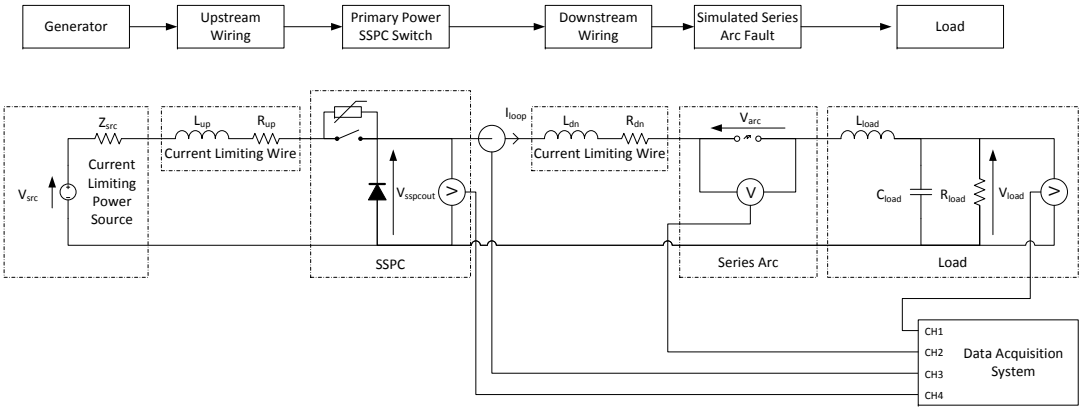


Figure A.3: Schematic Configuration of the Loose Terminal Scenario

Power is sourced from power supply V_{src} through source impedance Z_{src}, through the upstream wire feeder modelled by a series LR network $L_{up} + R_{up}$ to the SSPC input. From here power is switched out from the SSPC through the downstream wire feeder modelled by $L_{dn} + R_{dn}$, through the series arc fault to the load represented by R_{load}, C_{load} and L_{load}.

A.2.3 Predicted Loop Current I_{loop} Behaviour

The author has determined that understanding loop current I_{loop} behaviour mathematically is critical to the design of a passive arc fault detection system since if the current deviation during a series arc is small as a proportion of the normal load current then the fault will be difficult to identify from current alone. From the literature review in Chapter 2 it was determined that Naidu et al made the observation that during a series arc where the voltage seen at the load drops by the arc voltage, the corresponding reduction in current can be calculated from Equation (A.4) [69].

$$I_{arc} = \frac{V_{src} - V_{arc}}{Z_{load}} < I_{load} = \frac{V_{src}}{Z_{load}} \tag{A.4}$$

where I_{arc} is the current through the series arc fault, V_{src} is the source voltage, V_{arc} is the arc voltage, Z_{load} is the load impedance and I_{load} is the normal load current.

Based on this work the author analysed the test circuit illustrated in Figure A.3 and proposed the concept of the current reduction ratio r which represents the reduction in loop current level during a series arc fault as a proportion of the normal load current

I_{load} and this relationship is given in Equation (A.5). Applying simple circuit analysis in Equation (A.5) a simple expression for current reduction ratio r can be derived in the form of Equation (A.6). The review of Sölver's arc characteristics in Section A.2.1 identified that for short arcs (∼1mm), since arc voltage is current invariant, it can be assumed that arc voltage is constant at ∼15V, and it is therefore predicted that the current reduction ratio r will decrease with higher power supply voltages. Taking the two existing DC aerospace electrical distribution system voltages 28VDC and 270VDC, current reduction ratios can be calculated as per Equations (A.7) and (A.8) giving 54% and 5.6% respectively.

$$r = \frac{I_{load} - I_{arc}}{I_{load}} = \frac{\frac{V_{line}}{R_{load}} - \frac{V_{line} - V_{arc}}{R_{load}}}{\frac{V_{line}}{R_{load}}} \tag{A.5}$$

$$r = \frac{V_{arc}}{V_{src}} \tag{A.6}$$

$$r_{28V} = \frac{V_{arc}}{V_{src}} = \frac{15}{28} = 0.54 \equiv 54\% \tag{A.7}$$

$$r_{270V} = \frac{V_{arc}}{V_{src}} = \frac{15}{270} = 0.056 \equiv 5.6\% \tag{A.8}$$

The rate of change of loop current is an important factor in the design of a passive arc fault detection system since a given passive arc fault detection system must be capable of detecting the rate of change of current associated with a series arcing event. The rate of change of loop current I_{loop} is determined by the total loop inductance L_{total}, where Equation (A.9) shows how the loop inductance is calculated.

$$L_{total} = L_{up} + L_{dn}\,[+L_{load} + L_{src}] \tag{A.9}$$

where L_{up} represents the upstream inductance from generator to SSPC, L_{dn} represents the downstream inductance between SSPC and load, L_{load} represents load inductance, and L_{src} represents source inductance.

Now using Equation (A.10), which describes the electrical behaviour of an inductor, the rate of change of loop current I_{loop} with respect to time can be determined in Equation (A.11), based on a step change in arc voltage V_{arc} from 0 to 15V and arbitrary total loop inductance L_{total} of 50μH.

$$V_{arc} = L_{total}\frac{dI_{loop}}{dt} \tag{A.10}$$

$$\frac{dI_{loop}}{dt} = \frac{V_{arc}}{L_{total}} = \frac{15}{50 \times 10^{-6}} = 0.3 \times 10^{6} A/s \tag{A.11}$$

Given that arc voltage V_{arc} is source voltage invariant and broadly loop current invariant, the rate of change of loop current I_{loop} is determined from the total loop inductance L_{total} alone.

A.2.4 Predicted SSPC Output Voltage $V_{sspcout}$ Behaviour

The literature review did not present a mathematical description of peak SSPC or circuit breaker output voltage $V_{sspcout}$ as a function of arc voltage V_{arc}. The author therefore analysed the test schematic in Figure A.3 and determined that since arc voltage V_{arc} is broadly current invariant, the voltage spike appearing at the SSPC output during arc strike is given approximately by the arc voltage V_{arc} multiplied by the ratio of source inductance L_{src} and upstream wire feeder inductance L_{up} to the total loop inductance L_{total}. Assuming that source inductance L_{src} is negligible, the peak SSPC output voltage $\hat{V}_{sspcout}$ can be determined by Equation (A.12).

$$\hat{V}_{sspcout} \quad = \quad V_{src} + V_{arc}\left[\frac{L_{up}}{L_{dn} + L_{up} + L_{load}}\right] \tag{A.12}$$

The significance of this prediction is that for low inductance loads the peak SSPC output voltage created by a series arc fault event is determined mainly by the ratio of upstream and downstream wire feeders, and thus the physical positioning of the SSPC between the power supply and the load which is being fed.

A.2.5 Predicted Load Voltage V_{load} Behaviour

Predicting the load voltage V_{load} during a series arc fault is simple assuming that voltage drops caused by resistive losses in the wire feeders and SSPC are negligible. In this case the load voltage drops by the arc voltage during a series arc fault in accordance with Equation (A.13).

$$V_{load} \quad = \quad V_{src} - V_{arc} \tag{A.13}$$

Given again that arc voltage V_{arc} is broadly loop current invariant and is in the order of ∼15V, then for higher voltage 270VDC systems, the load will not register the arc voltage drop as a power interruption since this is within the acceptable level of power quality within the system.

A.2.6 Predicted Arc Power P_{arc} and Arc Energy Q_{arc} Behaviour

Arc power P_{arc} can be calculated by assuming again that arc voltage V_{arc} is loop current invariant which means that arc power P_{arc} is proportional to arc current I_{arc} and can be calculated in accordance with Equation (A.14).

$$P_{arc} \quad = \quad V_{arc}I_{arc} = V_{arc}(1-r)I_{load} \tag{A.14}$$

Equation (A.14) shows that arc power P_{arc} is not a function of source voltage V_{src}. Therefore, for a given load current I_{loop} in a range of different voltage systems the series arc power for short arc lengths is approximately equal. The arc energy Q_{arc} is defined by the author as the energy imparted into an arc of a given power P_{arc} with

a given arc duration determined by the arc strike time t_{strike} and arc quench time t_{quench}. Arc energy Q_{arc} can be calculated in accordance with Equation (A.15).

$$Q_{arc} = \int_{t_{strike}}^{t_{quench}} P_{arc} dt \tag{A.15}$$

The significance of arc power P_{arc} and arc energy Q_{arc} is that these figures allow the damage threat of a given arc fault to be estimated, where higher current arcs result in higher arc power dissipation, and longer duration arcs dissipate more energy, which can result in higher levels of damage.

A.2.7 Predicted Loose Terminal Behaviour

Although the effect of individual arcs can be calculated as presented earlier in this section, it is predicted that the effect of the loose terminal configuration detailed in SAE AS5692 [8] and SAE AS6087 [255] will result in chaotic arc events. Since the mechanical configuration of the experimental method detailed in Section A.3.2 is only one example of a physical electrical wiring configuration, which is subjected to one random vibration power spectral density profile, it is not worthy of numerical analysis, and therefore for completeness a statistical analysis method is presented in Section A.3.3.

A.3 Methodology of Loose Terminal Series Arc Fault Experiment

A.3.1 Electrical Configuration of Loose Terminal Series Arc Fault

This series of experiments uses a common top level schematic illustrated in Figure A.4, where a block diagram shows how the schematic emulates a typical solid state aircraft DC electrical power distribution system. Power was supplied by V_{src}, which in these experiments was provided by a California Instruments MX45 power supply [253]. The power supply was connected through the upstream cabling to a Solid State Power Controller (SSPC), which is shown with a simple equivalent schematic. The SSPC then provided power through a loose terminal to a configurable RLC load. Instrumentation was provided by an HBM Genesis 16t data acquisition system, which allowed continuous recording of four channels at up to 100MSPS. The instrumentation monitored and recorded the output voltage of the SSPC $V_{sspcout}$, the arc voltage V_{arc} and the load voltage V_{load} using three 100:1 isolated differential voltage probes. The instrumentation also monitored and recorded the loop current I_{loop} using a single Hall effect current probe / clamp.

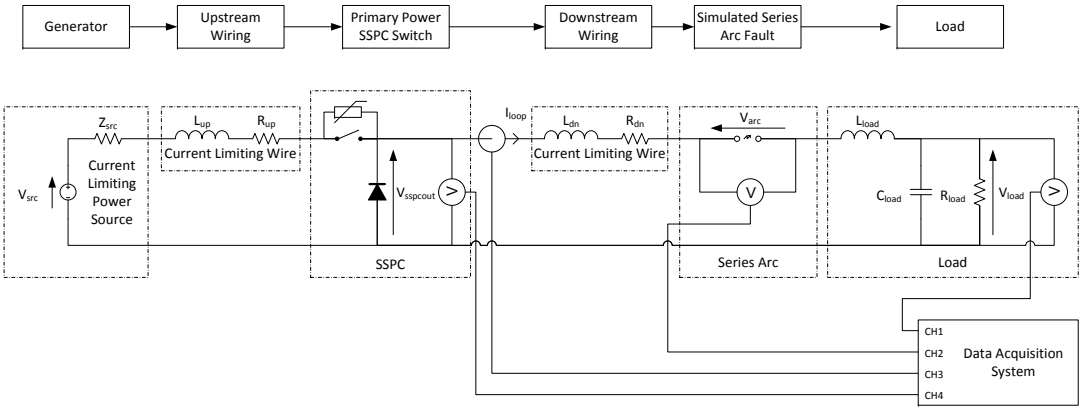


Figure A.4: Schematic Configuration of the Loose Terminal Scenario

Table A.1 shows the range over which the parameters illustrated in Figure A.4 were varied during the experimental process. The supply voltage V_{src} was fixed, while the other combinations of parameters were varied. One circuit parameter was varied at a time such that a correlation between arc/circuit behaviour could be analysed.

Parameter	**Tested Range**
V_{src}	28V and 270V
R_{load}	2.5A to 30A (at supply voltage V_{src}, thus giving a resistance)
L_{load}	0 to 100μH
C_{load}	0 to 380μF
L_{up}	0 to 100μH
L_{down}	0 to 100μH

Table A.1: Tested Parameter Range for Loose Terminal Testing Scenario

It is assumed that the position of the series arc is near the load. Whilst it is not realistic to assume that every series arc in an aircraft power distribution system occurs near the load, the effect of repositioning the arc closer to the SSPC output can be likened to the introduction of load inductance, and therefore no valuable laboratory time was spent on varying arc position.

A.3.2 Mechanical Configuration of Loose Terminal Series Arc Fault

A common mechanical configuration illustrated in Figure A.5 was used for all experiments. Mechanical parameters were kept constant for all experiments and arcing components were replaced after each test, since the primary purpose of this series of experiments was to investigate the effect of series arc faults on electrical power distribution systems with different electrical parameters. The representative mechanical configuration given in SAE AS5692 [8] limits the arc length substantially to the order of millimetres, and therefore allows a relationship between the mechanical system and electrical system to be determined based on Section A.2.1, where for short arcs with load currents above a given minimum current threshold, the arc voltage is invariant with respect to current.

The loose terminal mechanical configuration is illustrated in context in Figure A.5.

The random vibration profile used for the loose terminal scenario is given in Figure A.6. This profile is taken from SAE AS5692 [8] and was originally derived from the environmental qualification requirements given in RTCA DO-160G [49], which are representative of a typical fixed wing commercial jet aircraft.

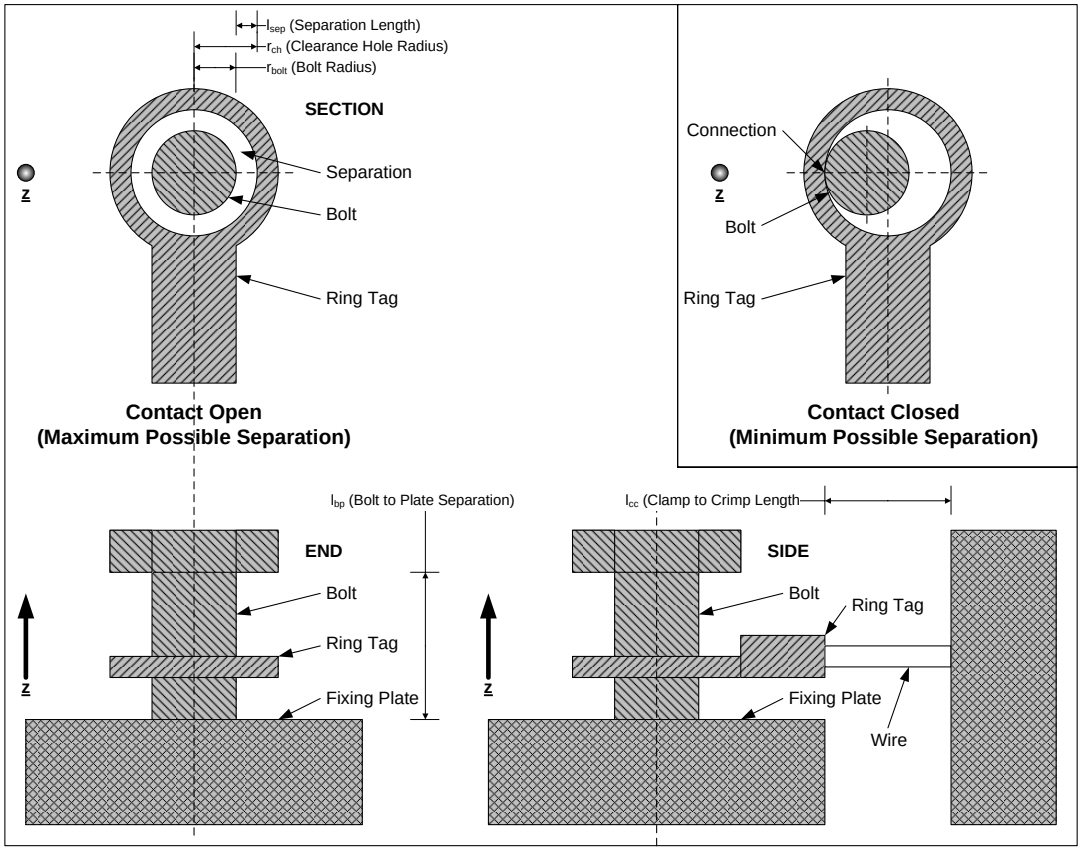
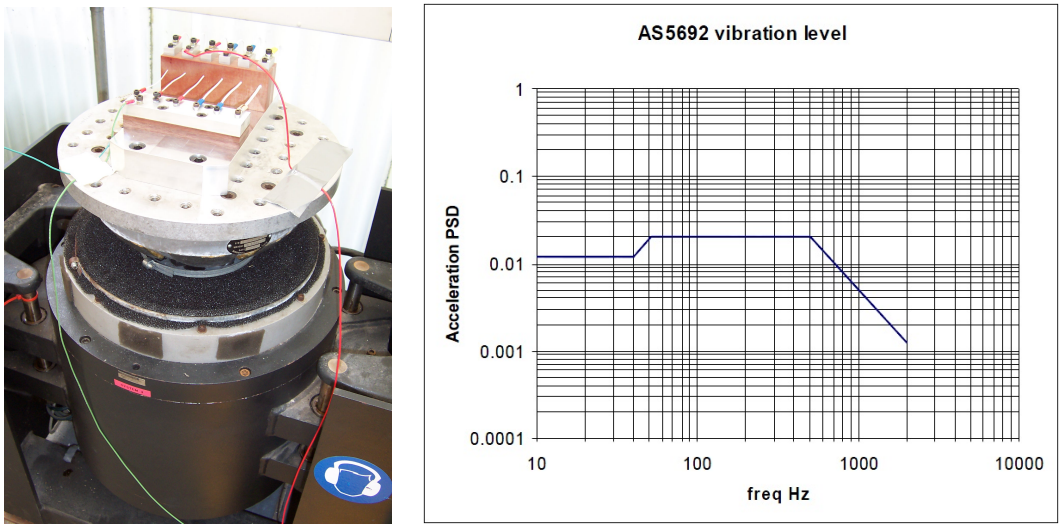


Figure A.5: Experimental Configuration of the Loose Terminal Scenario

Parameter	Description	Value
r_{bolt}	Bolt Radius	1.92mm
r_{ch}	Clearance Hole Radius	2.7mm
l_{sep}	Maximum Electrode Separation Length	1.4mm
l_{bp}	Bolt to Plate Separation	2mm
l_{cc}	Clamp to Crimp Length	80mm
d_{wire}	Wire Diameter	3.3mm

Table A.2: Mechanical Parameters for All Tests



(a) An Illustration of the Loose Terminal Block Mounted on a Vibration Table

(b) Vibration Profile for Loose Terminal Scenario Given in AS5692 [8] and RTCA DO-160G [49]

Figure A.6: Vibration Table and Vibration Profile Illustrations

A.3.3 Feature Detection and Automated Series Arc Fault Analysis

Following the data capture for each test scenario, it was necessary to extract the arc period and arc duration data. To achieve this a feature extraction activity was executed in MATLAB® to extract arc events from the loop current I_{loop} and arc voltage V_{arc} waveforms. This is akin to series arc fault detection and therefore poses a number of similar challenges.

Szeliski defines "feature detection" as the detection of a known "feature" in another image or data set [260]. Cyganek and Siebert suggest that feature detection can be accomplished using: "convolution", "filtering", "mask separability" and "discrete differentiation"; "Gaussian" and "binomial" filters are also discussed [261]. An important consideration during "feature detection" activities is the concept of scale-space

and multiresolution analysis. Lindeberg defines the problem of "scale" thus [262].

> *"...objects in the world and details in images, only exist as meaningful entities over limited ranges of scale, in contrast to certain ideal mathematical entities like "point", "line", "step edge", or "linear slope", which appear in the same way at all scales of observation."*

Lindeberg provides an example that a tree branch only makes sense at a scale from a few centimetres to a few meters at most, where considering a tree branch at the nanometre scale is meaningless [262]. Scale-space is an important concept when considering "feature detection" techniques where Heijmans describes scale space thus.

> *"In our view a scale-space is the mathematical construct that describes the scale-dependent observation (probing) of images."*

During the representative arc characterisation exercise, data was captured at a rate of 100MSPS for the purposes of archival and is noisy in nature, even when using a comparatively clean synthesised lab power supply with respect to the relatively noisy output from an aircraft generator. In contrast to the sampling rate, the edges created in the loop current I_{loop} waveform are comparatively slow, and therefore a macroscopic view of the sampled waveform is more useful than the microscopic view where "edge detection", a subset of "feature detection", is of great interest for this application. Basu reviews the problems encountered with edge detection methods and provides a summary of the issues which include noise, edge localisation, smoothing and scale [263]. Noise can corrupt the rapid transition between samples, making edges harder to identify. Edge localisation is an issue because noise added to an image or signal can cause the position of the detected edge to be shifted from its true location. Smoothing of edges caused by noise filtering removes high frequency content from the original image or signal, which also removes the fast changes between data samples that define a given edge. Finally scale is an issue since small scale analysis detects fine detail from an image or signal but is sensitive to noise, and a larger scale extracts coarser changes but edges can suffer further from localisation error.

Figure A.7 illustrates series arc fault behaviour in a 270VDC system with a 2A resistive load where five discrete arcs labelled "Arc 1" through "Arc 5" are visually identified. Taking "Arc 4" as an example it can be seen that the arc strikes at point (1), and this can be detected by computing and thresholding $-\frac{dI_{loop}}{dt}$ and $+\frac{dV_{arc}}{dt}$. The arc burns throughout (2) until a reconnection occurs at point (3), which can be detected by computing and thresholding $+\frac{dI_{loop}}{dt}$ and $-\frac{dV_{arc}}{dt}$. Arc duration $t_{duration}$ can be defined as the time between arc strike at point (1) and arc reconnection at point (3). Arc period t_{period} can be defined as the period between arc strike events, for example the period between "Arc 4" strike at point (1) and "Arc 5" strike at point (4).

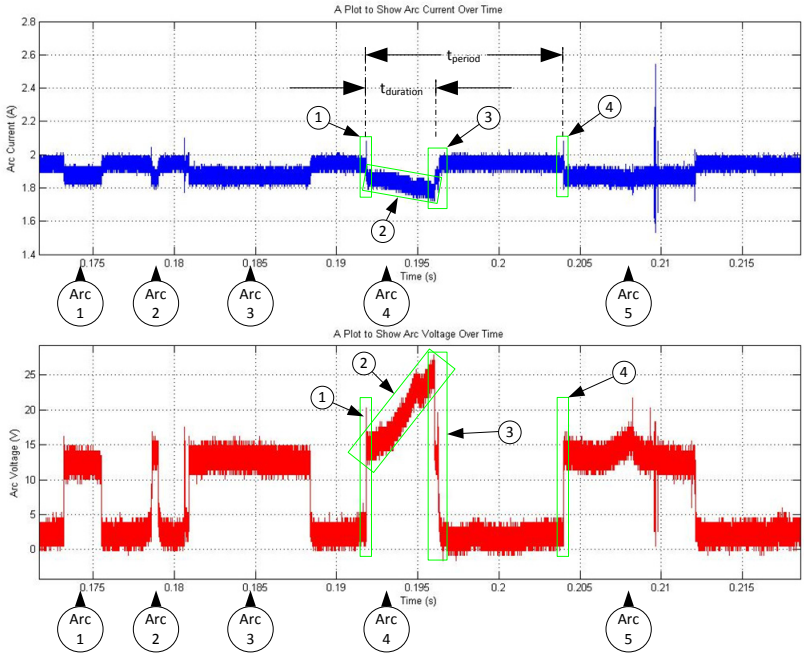


Figure A.7: Series Arc Fault Feature Extraction Waveform Example

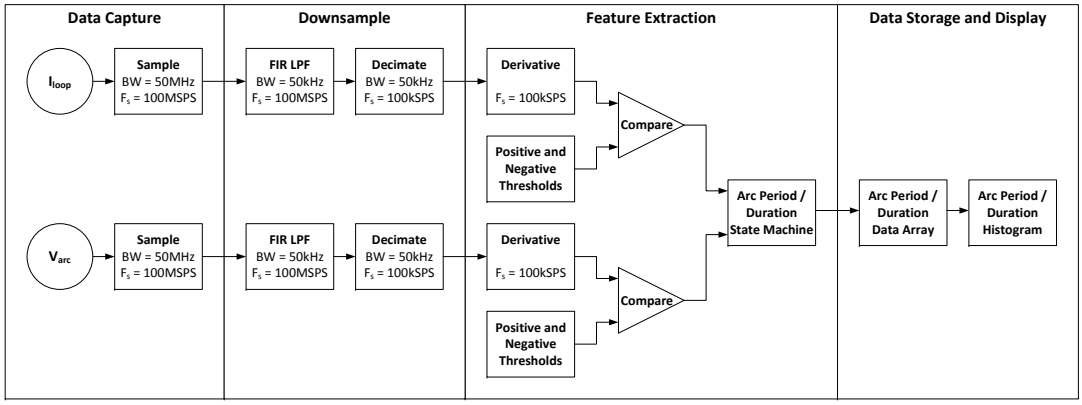


Figure A.8: Signal Processing Block Diagram

Figure A.8 illustrates how the I_{loop} and V_{arc} signals are processed in order to extract arc periods and durations. For this project it was determined that a process of down-sampling by firstly low pass filtering at 50kHz to provide anti-aliasing and secondly decimating by a factor of 1000 from a sampling frequency of 100MSPS to 100kSPS provided accurate feature detection, thus giving a sampling period of $10\mu s$, which retained the arc $\frac{dI_{loop}}{dt}$ and $\frac{dV_{arc}}{dt}$ features, but removed the high frequency (100kHz) noise generated by the lab power supply unit. Whilst Gaussian convolution techniques for edge detection were trialled, the author opted for the simplest approach in order to improve edge localisation and reduce processing time, given the large data set which runs to one gigabyte per experiment run. From the downsampled 100kSPS

signal a discrete sampled derivative is implemented to compute the $\frac{dI_{loop}}{dt}$ and $\frac{dV_{arc}}{dt}$ signals. The discrete sampled derivative is based on Newton's difference quotient, where Farid and Simoncelli remark that dropping the limit in the continuous definition of the differential operator given in Equation (A.16) in favour of a fixed sampling period where $\epsilon = T_s$ gives Equation (A.17).

$$D\{f(x)\} \equiv \lim_{\epsilon \to 0} \frac{f(x+\epsilon) - f(x)}{\epsilon} \tag{A.16}$$

$$f'[n] = \frac{f[n+1] - f[n]}{T_s} \tag{A.17}$$

The approach where the current sample and next sample are considered is called the forward difference derivative, and conversely when the current sample and previous sample are considered this is called the backward difference derivative [254]. The backward difference derivative was implemented for calculation of $\frac{dI_{loop}}{dt}$ and $\frac{dV_{arc}}{dt}$.

Following extraction of the edges from the input waveforms, the state machine in Figure A.9 was implemented in a MATLAB® script, and was used to determine whether arcs quench or whether arcs are maintained until contact reconnection following the initial arc strike.

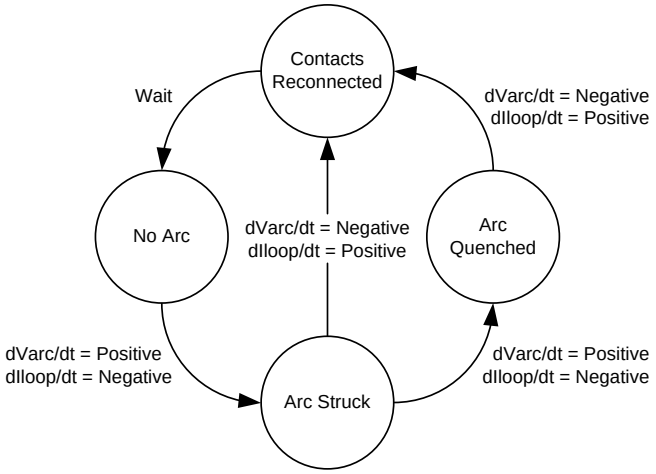


Figure A.9: State Diagram for Arc Waveform Analysis

This state machine was used in order to extract arc periods t_{period} and arc durations $t_{duration}$ from the time domain data. The arc periods and durations were plotted in histograms to determine the effect of the electrical parameters on the mechanical behaviour of the system. In addition to the extraction of timing data, when arc strike, quench, or reconnection events were encountered, the instantaneous peak arc voltages were captured, and histograms were plotted to allow analysis of arc voltage behaviour for each test conducted. The final MATLAB® feature extraction and graphing script is provided in Appendix A.7.

A.3.4 Assumptions and Experimental Controls

For each experiment the SSPC output voltage $V_{sspcout}$, arc voltage V_{arc}, loop current I_{loop} and load voltage V_{load} data was captured for three seconds at a rate of 100MSPS for each channel. Multiple test runs were carried out exhaustively for each scenario to ensure that the captured data was valid, and the presented electronic and mechanical parameters were carefully controlled during testing. Arc faults are chaotic in nature due to the random vibration excitation and the electrode interactions, and therefore no practical number of experiment repetitions will result in identical data.

The California Instruments power supply used for testing here has high output capacitance and is not explicitly representative of a real aircraft system, which would derive DC electrical power from a generator and Transformer Rectifier Unit (TRU) with limited output capacitance. This resulted in reduced low frequency voltage ripple in the recorded data due to increased power supply output smoothing and regulation. Furthermore the lab power supply used for this experiment is a switching power supply which produces higher levels of high frequency noise measured at typically $3V_{p-p}$, which is more noticeable when operating at the lower load current levels of 2.5A.

The electrical loads used were all resistance / inductance / capacitance combinations since it was assumed that specific loads would provide too much variability for initial testing. A discrete cable configuration was used for power feeders and power returns, whereas in aircraft power feeders are used to provide current to the load, and current returns through the aircraft chassis. The inductances of all cables used were recorded to address this dissimilarity, and it was assumed that the results gathered can be compared to the inductance of the proposed EWIS in a given aircraft design.

A.3.5 Presentation of Data

For each experiment a 100ms window of arcing is given along with a separate ∼4ms subset single arc view, which allows a single arc to be observed more clearly. Understanding arc faults is a multiscale problem which must be considered on both the macroscopic and microscopic scales. The final plots for each experiment are a histogram showing the period between arc strikes and the total number of arcs, and a histogram showing the duration of arc events. The histograms provide a simple way of understanding the affect of the mechanical system on electrical arc behaviour. All data was prepared and presented with bespoke MATLAB® scripts, and the results in this document show the effect of testing with the extremes of each parameter.

The analysis exercise consumed many months due to the safety requirements working with high voltages and currents, necessitating the requirement for two-man working. In addition to this 1 Terabyte of data was gathered during these experiments, and storing / processing each waveform required huge computational effort.

A.4 Experimental Results

A.4.1 Test Parameters

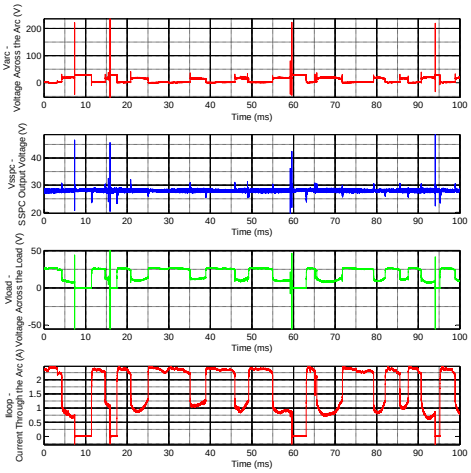
The parameters used for Tests 1 through 12 are recorded in Table A.3. The table maps each test performed to the appropriate figures showing processed results in the main body of this section, and as such these tables should be used as an index to the results section. In addition to the Figures referenced in Table A.3, Tables A.4 and A.5 in Section A.4.4 provide statistical data regarding the arcs observed in each test.

Test	V_{src} (V)	R_{load} $(A(\Omega))$	L_{load} (μH)	C_{load} (μF)	L_{up} (μH)	L_{dn} (μH)	**100ms Figure**	**Single Arc Figure**	**Histogram Figure**
1	28	2.5 (11.2)	12	0	4.25	12	A.10(a)	A.10(c)	A.10(e)
2	270	2.5 (108)	12	0	4.25	12	A.10(b)	A.10(d)	A.10(f)
3	28	20 (1.40)	12	0	4.25	12	A.11(a)	A.11(c)	A.11(e)
4	270	25 (10.8)	12	0	4.25	12	A.11(b)	A.11(d)	A.11(f)
5	28	2.5 (11.2)	62	0	4.25	12	A.12(a)	A.12(c)	A.12(e)
6	270	2.5 (108)	62	0	4.25	12	A.12(b)	A.12(d)	A.12(f)
7	28	2.5 (11.2)	12	380	4.25	12	A.13(a)	A.13(c)	A.13(e)
8	270	2.5 (108)	12	380	4.25	12	A.13(b)	A.13(d)	A.13(f)
9	28	10 (2.80)	112	380	4.25	12	A.14(a)	A.14(c)	A.14(e)
10	270	10 (27.0)	112	380	4.25	12	A.14(b)	A.14(d)	A.14(f)
11	28	10 (2.80)	12	0	54.25	12	A.15(a)	A.15(c)	A.15(e)
12	270	10 (27.0)	12	0	54.25	12	A.15(b)	A.15(d)	A.15(f)

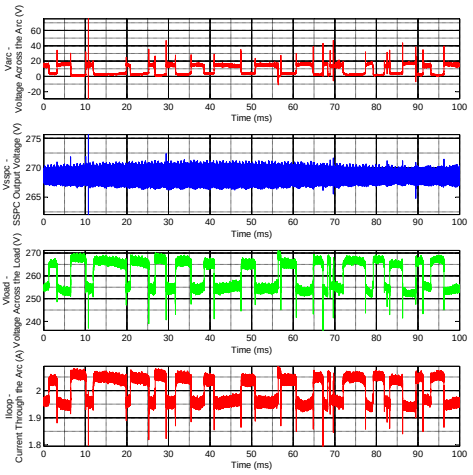
Table A.3: Experimental Parameters For Tests 1 Through 12

Given the imperfections in the lab environment, there are minimum system inductances present due to the self inductance of interconnecting cables and load banks and these are recorded in Table A.3 for completeness. The minimum downstream wiring inductance L_{dn} is 12μH due to cable inductance between the loose terminal and the resistive load bank. The minimum load inductance L_{load} is 12μH due to inherent inductance of the wire-wound resistive load bank. The minimum upstream wire inductance L_{up} is 4.25μH due to the cable inductance between the power supply and the SSPC switch.

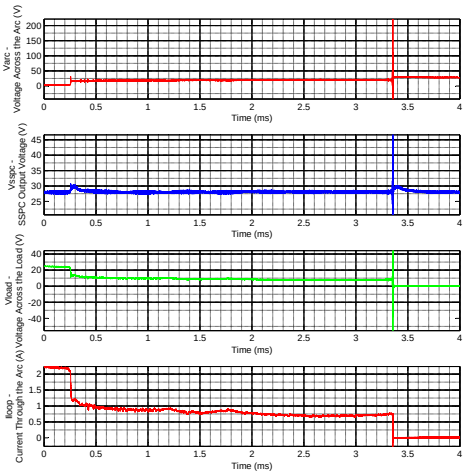
A.4.2 Arc Waveforms With Arc Period/Duration Histograms



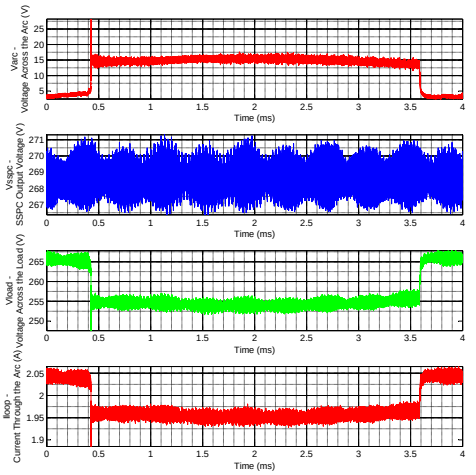
(a) 28VDC 2.5A Load - 100ms



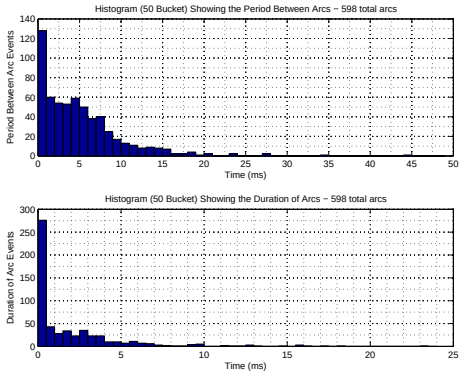
(b) 270VDC 2.5A Load - 100ms



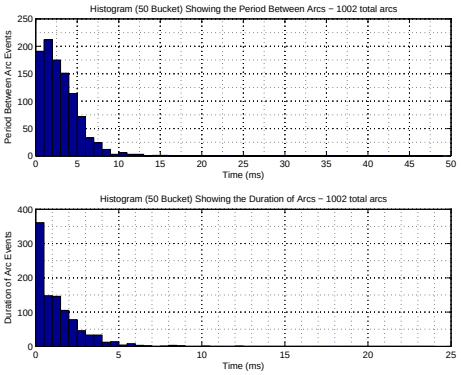
(c) 28VDC 2.5A Load - Single Arc



(d) 270VDC 2.5A Load - Single Arc

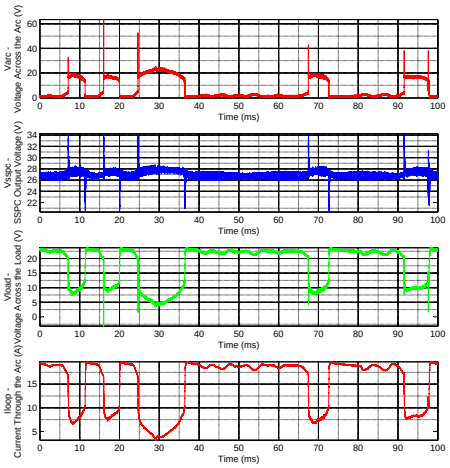


(e) 28VDC 2.5A Load - Histogram

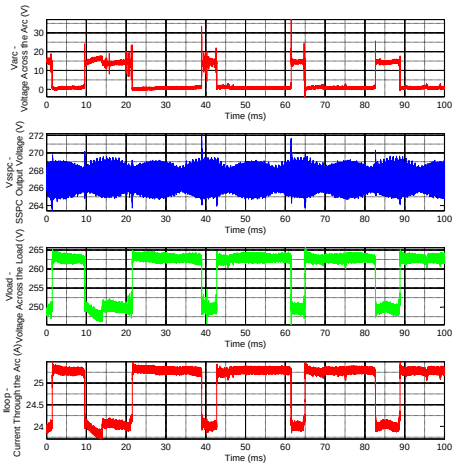


(f) 270VDC 2.5A Load - Histogram

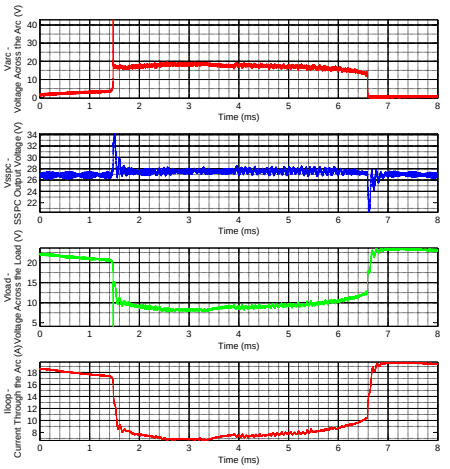
Figure A.10: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 1 and 2



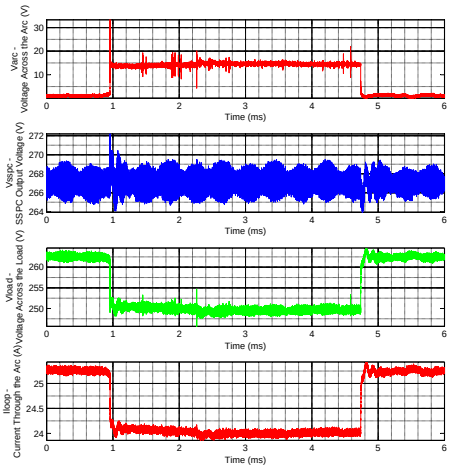
(a) 28VDC 20A Load - 100ms



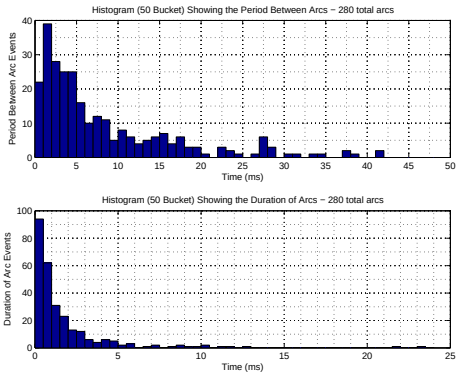
(b) 270VDC 25A Load - 100ms



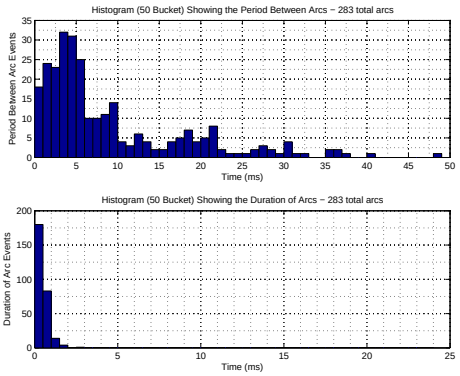
(c) 28VDC 20A Load - Single



(d) 270VDC 25A Load - Single

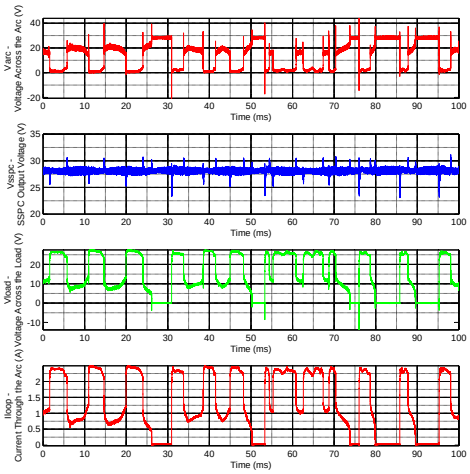


(e) 28VDC 20A Load - Histogram

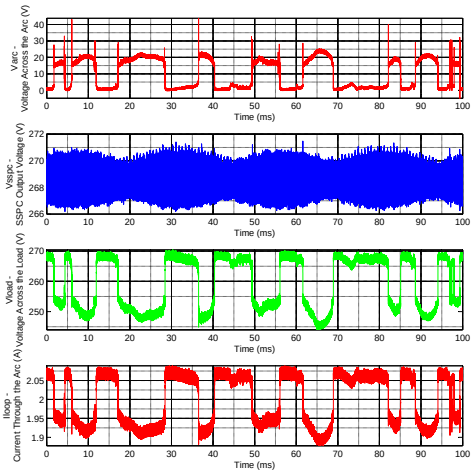


(f) 270VDC 25A Load - Histogram

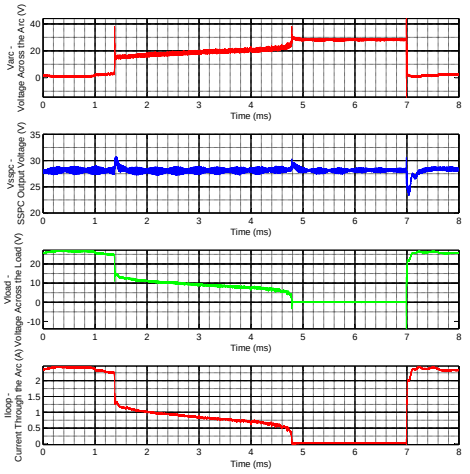
Figure A.11: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 3 and 4



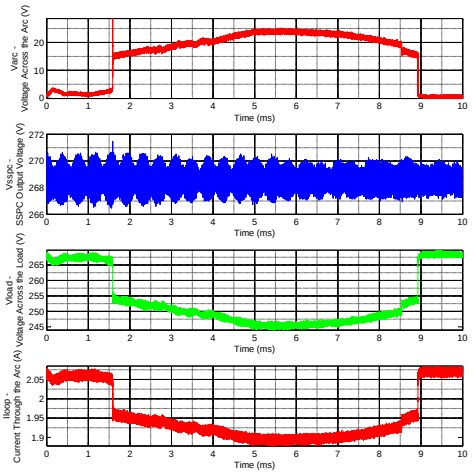
(a) 28VDC 2.5A//50μH Load - 100ms



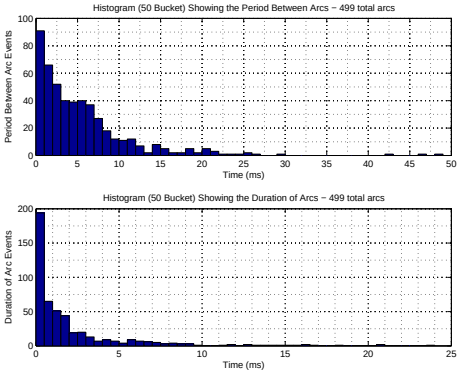
(b) 270VDC 2.5A//50μH Load - 100ms



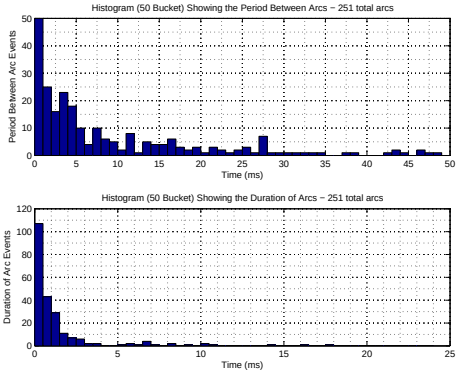
(c) 28VDC 2.5A//50μH Load - Single



(d) 270VDC 2.5A//50μH Load - Single

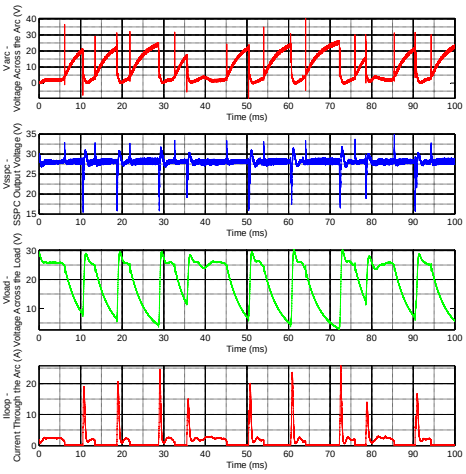


(e) 28VDC 2.5A//50μH Load - Histogram

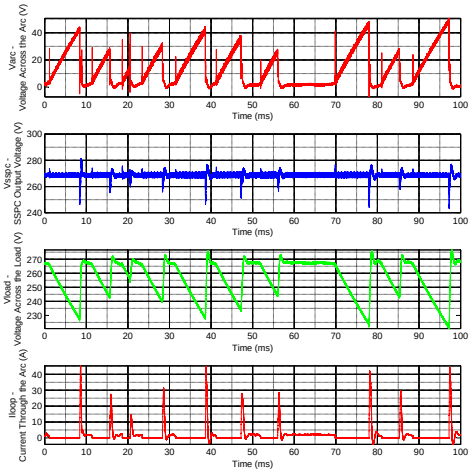


(f) 270VDC 2.5A//50μH Load - Histogram

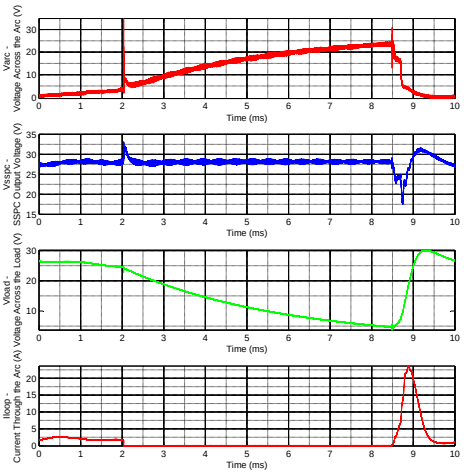
Figure A.12: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 5 and 6



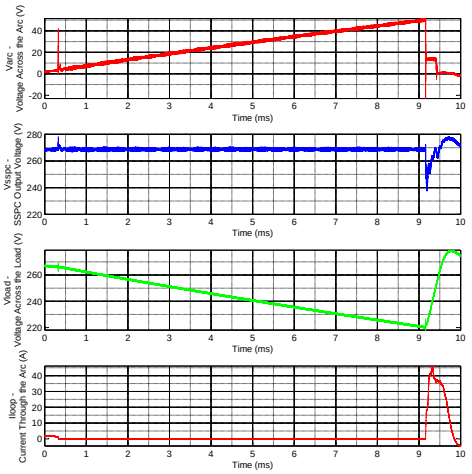
(a) 28VDC 2.5A//380μF Load - 100ms



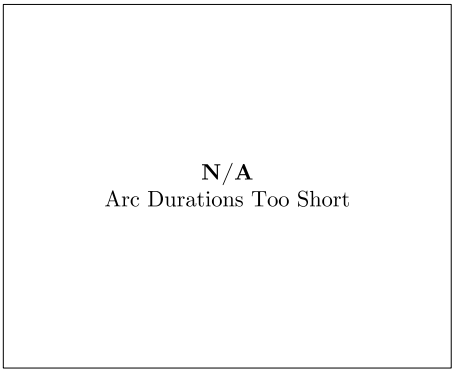
(b) 270VDC 2.5A//380μF Load - 100ms



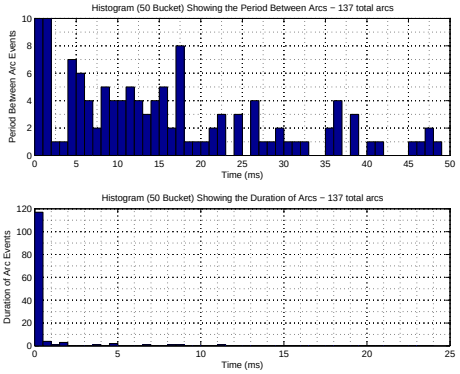
(c) 28VDC 2.5A//380μF Load - Single



(d) 270VDC 2.5A//380μF Load - Single

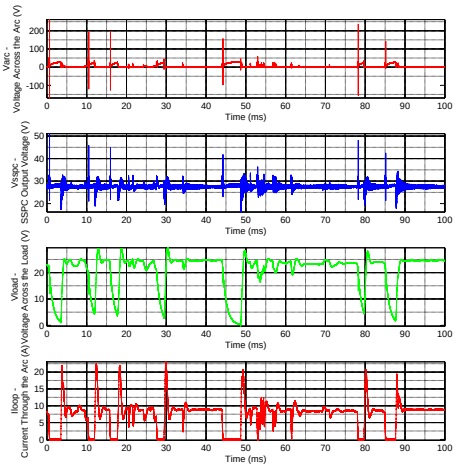


(e) 28VDC 2.5A//380μF Load - Histogram

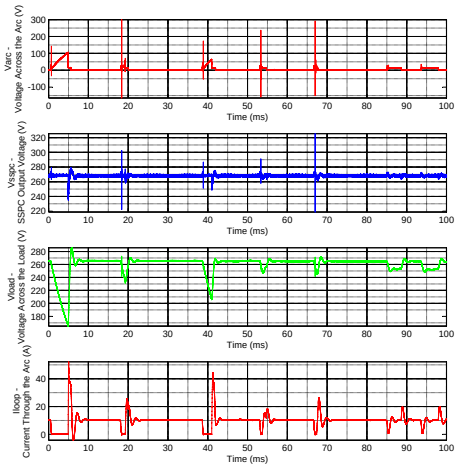


(f) 270VDC 2.5A//380μF Load - Histogram

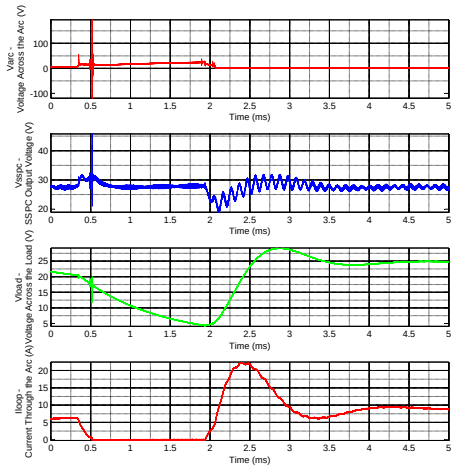
Figure A.13: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 7 and 8



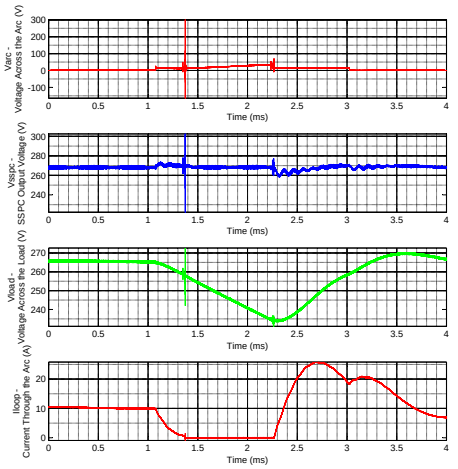
(a) 28VDC 2.5A//380μF//100μH Load - 100ms



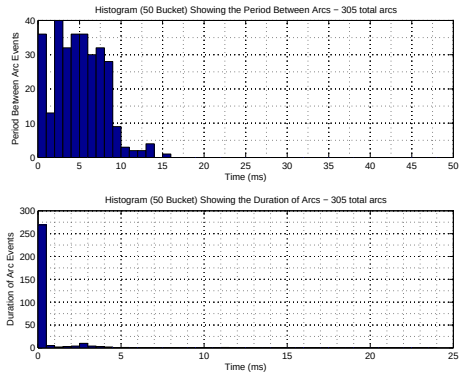
(b) 270VDC 2.5A//380μF//100μH Load - 100ms



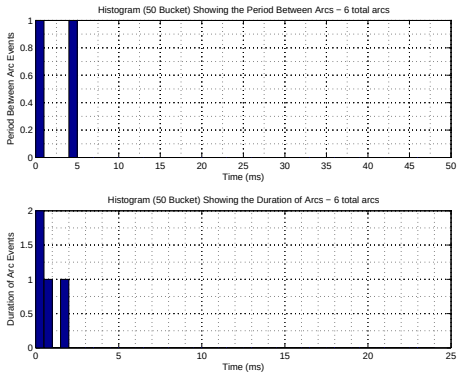
(c) 28VDC 2.5A//380μF//100μH Load - Single



(d) 270VDC 2.5A//380μF//100μH Load - Single

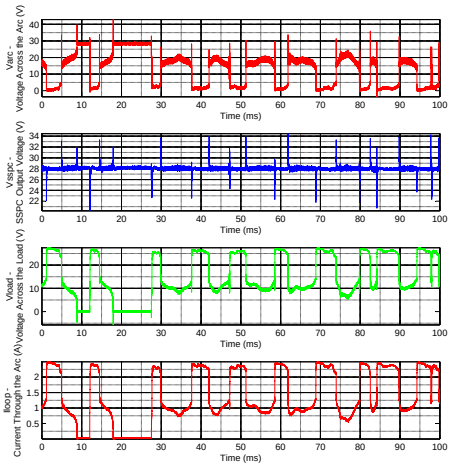


(e) 28VDC 2.5A//380μF//100μH Load - Histogram

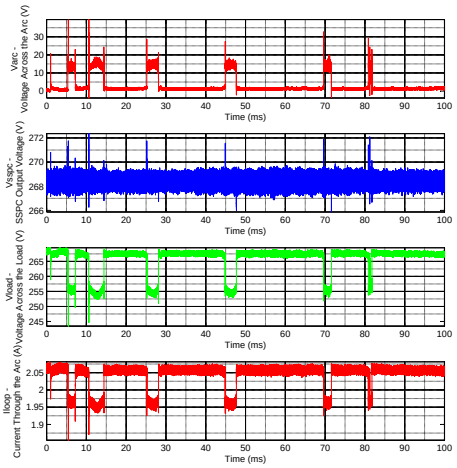


(f) 270VDC 2.5A//380μF//100μH Load - Histogram

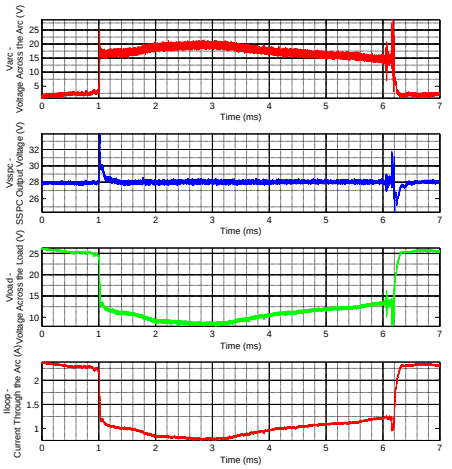
Figure A.14: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 9 and 10



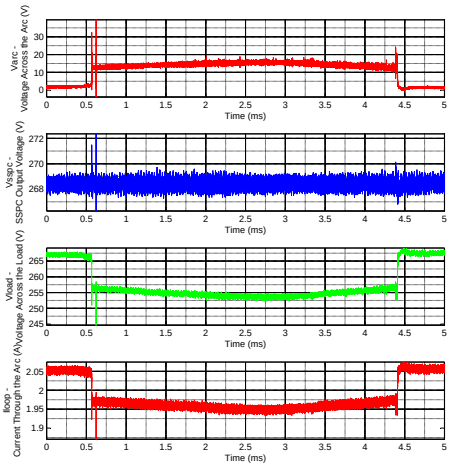
(a) 28VDC 2.5A w/50μH Upstream - 100ms



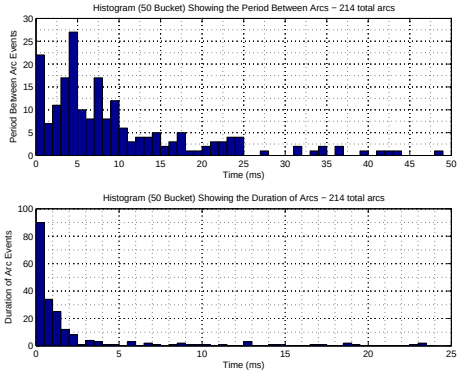
(b) 270VDC 2.5A w/50μH Upstream - 100ms



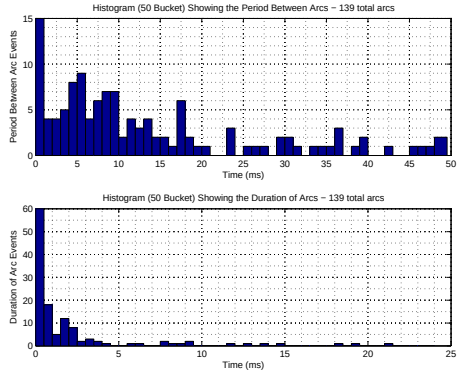
(c) 28VDC 2.5A w/50μH Upstream - Single



(d) 270VDC 2.5A w/50μH Upstream - Single



(e) 28VDC 2.5A w/50μH Upstream - Histogram



(f) 270VDC 2.5A w/50μH Upstream - Histogram

Figure A.15: Plots showing V_{arc}, $V_{sspcout}$, V_{load} and I_{loop} Signals Under the Loose Terminal Scenario for Tests 11 and 12

A.4.3 Arc Strike, Quench and Reconnect Voltage Histograms

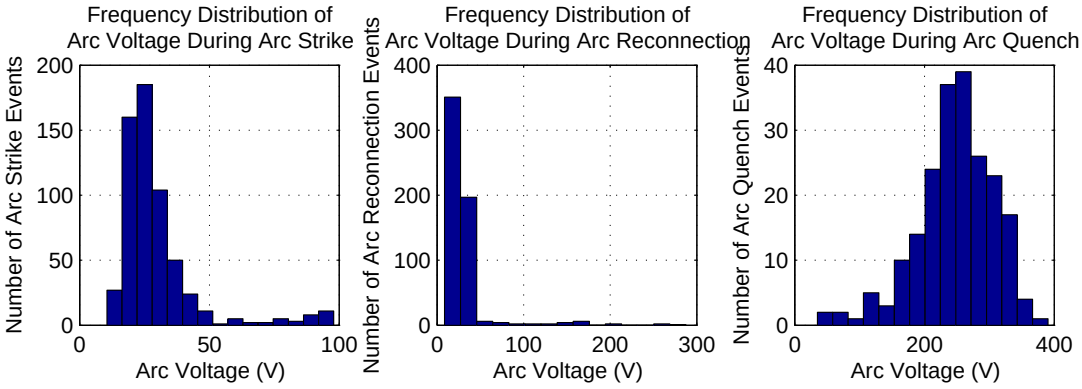


Figure A.16: Histogram Showing Strike, Quench and Reconnect Voltages for Test 1 (28VDC 2.5A Resistive Load)

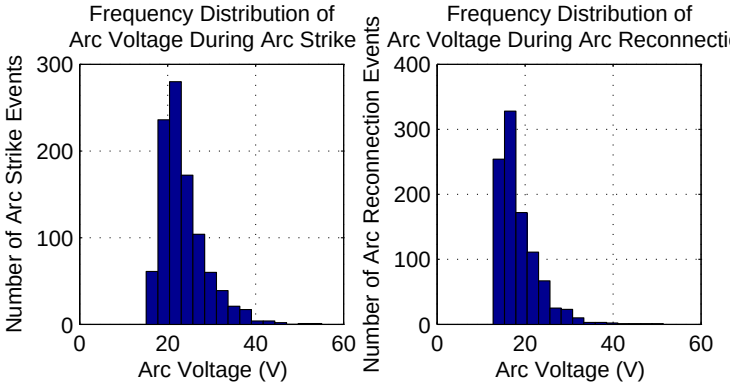


Figure A.17: Histogram Showing Strike, Quench and Reconnect Voltages for Test 2 (270VDC 2.5A Resistive Load)

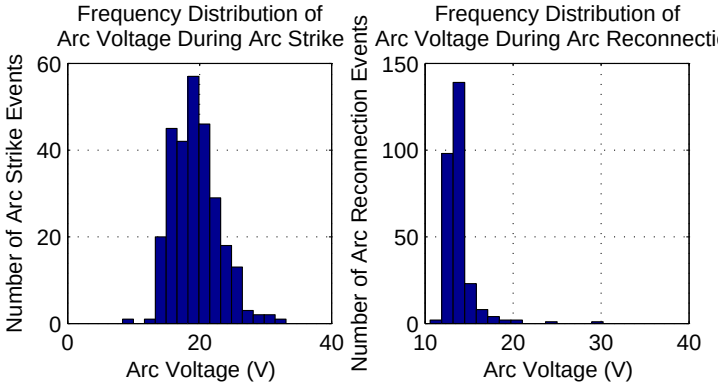


Figure A.18: Histogram Showing Strike, Quench and Reconnect Voltages for Test 3 (28VDC 20A Load)

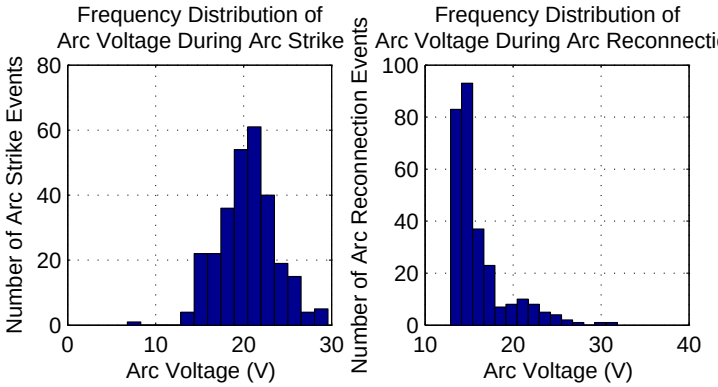


Figure A.19: Histogram Showing Strike, Quench and Reconnect Voltages for Test 4 (270VDC 25A Load)

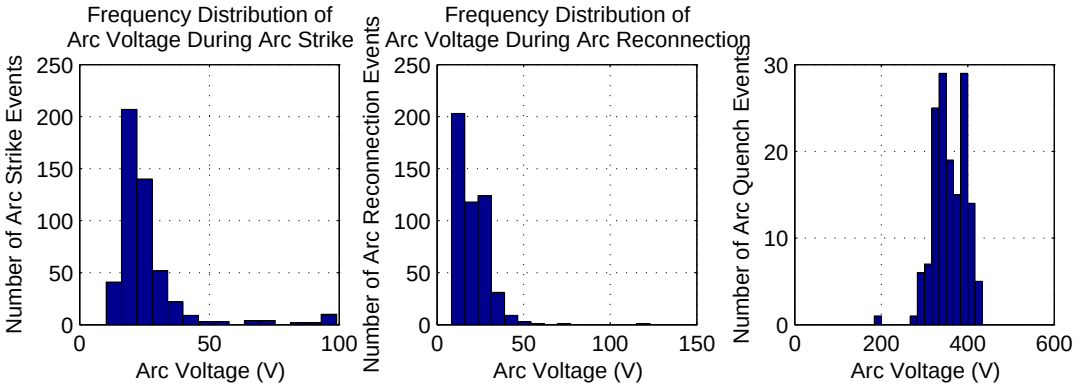


Figure A.20: Histogram Showing Strike, Quench and Reconnect Voltages for Test 5 (28VDC 2.5A//50μH Load)

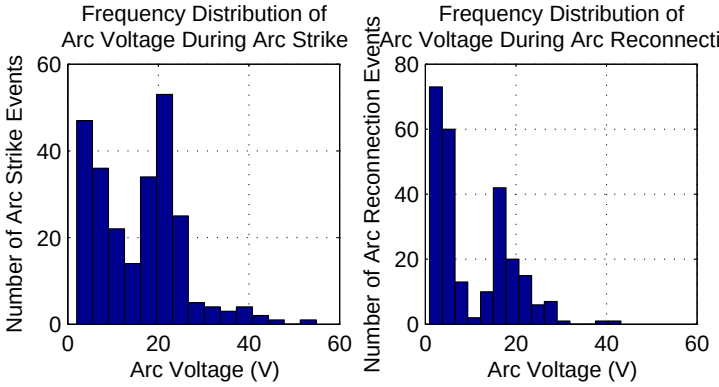


Figure A.21: Histogram Showing Strike, Quench and Reconnect Voltages for Test 6 (270VDC 2.5A//50μH Load)

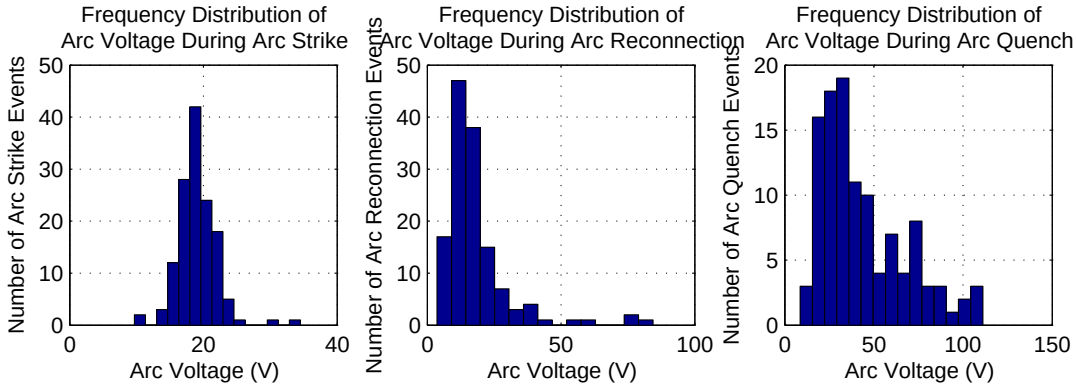


Figure A.22: Histogram Showing Strike, Quench and Reconnect Voltages for Test 8 (270VDC 2.5A//380μF Load)

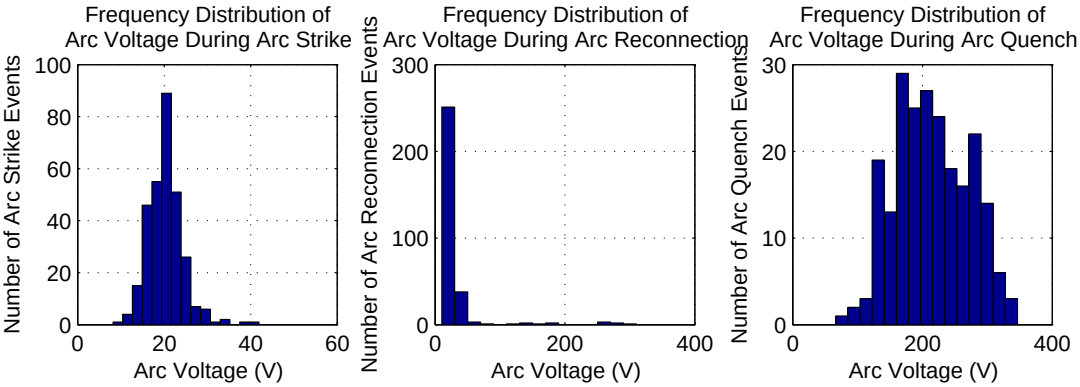


Figure A.23: Histogram Showing Strike, Quench and Reconnect Voltages for Test 9 (28VDC 2.5A//380μF//100μH Load)

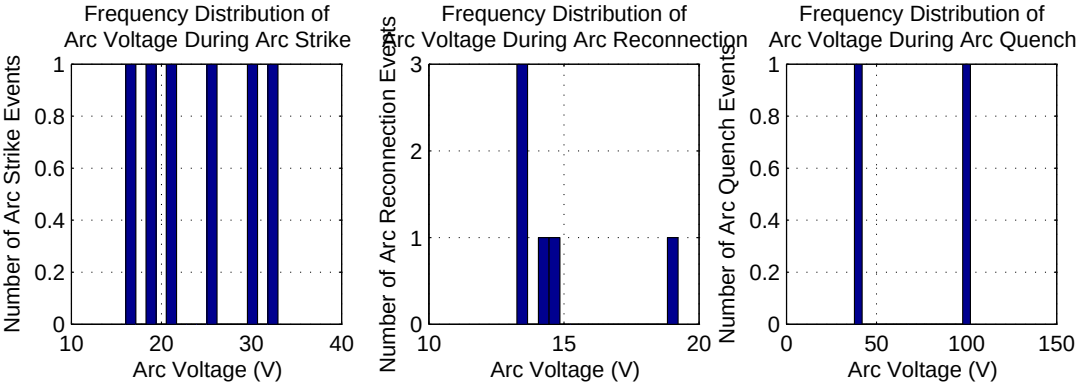


Figure A.24: Histogram Showing Strike, Quench and Reconnect Voltages for Test 10 (270VDC 2.5A//380μF//100μH Load)

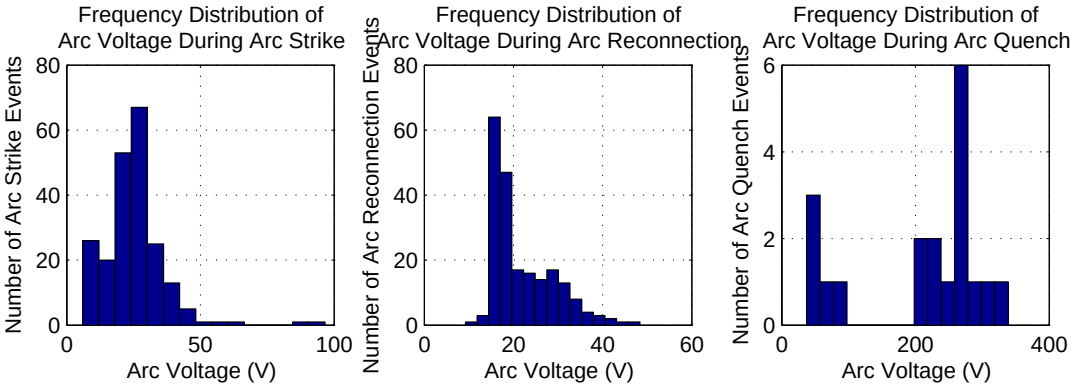


Figure A.25: Histogram Showing Strike, Quench and Reconnect Voltages for Test 11 (28VDC 2.5A w/50μH Upstream)

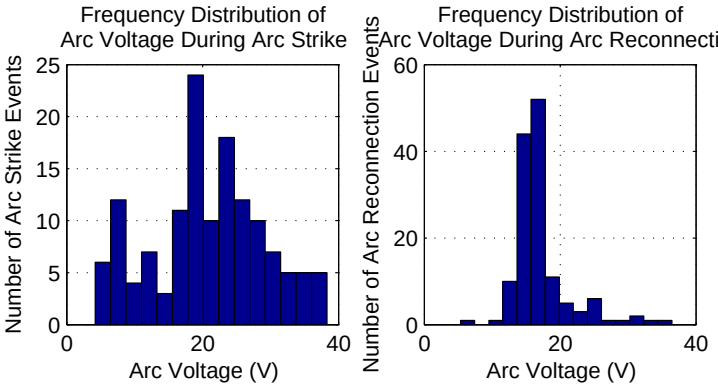


Figure A.26: Histogram Showing Strike, Quench and Reconnect Voltages for Test 12 (270VDC 2.5A w/50μH Upstream)

A.4.4 Summary of Extracted Arc Statistics

Test	Number of Arcs			Arc Period (ms)			Arc Duration (ms)		
	Total	Quench	Reconn.	Min	Mean	Max	Min	Mean	Max
1	598	208	390	0.0044	5.05	44.2	0.0044	1.98	23.4
2	1002	0	1002	0.0267	2.97	15.3	0.0133	1.37	12.1
3	280	0	280	0.0489	10.8	183	0.0089	2.13	54.1
4	283	0	283	0.0267	10.5	200	0.0133	0.440	3.00
5	499	151	348	0.0044	6.05	151	0.0044	2.92	151
6	251	0	251	0.0000	11.7	178	0.0200	2.41	100
8	137	112	25	0.0030	21.8	177	0.0010	0.649	25.7
9	305	222	83	0.0830	4.99	15.9	0.0030	0.538	11.1
10	6	2	4	0.7900	338	1020	0.3150	26.7	130
11	214	19	195	0.0089	14.1	320	0.0044	5.62	311
12	139	0	139	0.0400	21.7	188	0.0133	6.89	148

Table A.4: Summary of Arc Quantity, Period and Durations Statistics

Test	Arc Strike Voltage (V)			Arc Quench Voltage (V)			Arc Reconnect Voltage (V)		
	Min	Mean	Max	Min	Mean	Max	Min	Mean	Max
1	10.5	29.6	97.9	35.0	248	390	8.6	28.4	287
2	15.1	23.5	55.0	N/A	N/A	N/A	12.8	18.5	51.4
3	8.3	19.4	33.1	N/A	N/A	N/A	10.6	13.8	30.2
4	6.8	20.5	29.6	N/A	N/A	N/A	12.9	16.1	31.8
5	10.2	25.9	99.0	184	358	434	8.3	21.0	123
6	2.0	15.7	54.9	N/A	N/A	N/A	0.9	10.4	43.2
8	9.7	19.1	34.5	8.7	44.1	111	3.6	18.0	84.4
9	8.2	20.3	42.0	66.4	214	346	10.3	32.4	310
10	16.0	24.1	32.9	37.7	69.9	102	13.3	14.7	19.2
11	6.0	25.3	96.6	37.2	209	339	9.2	21.8	48.4
12	4.2	20.8	38.3	N/A	N/A	N/A	5.3	17.1	36.5

Table A.5: Summary of Arc Strike, Quench and Reconnect Voltage Statistics

A.5 Analysis and Discussion

The analysis of this experiment focusses on understanding the electrical behaviour of electric arcs within aircraft electrical power systems and the interaction of the mechanical system and electrical system. It is proposed that the requirements for a passive electrical arc fault detection system based on current / voltage waveform processing can be developed for each scenario. To achieve this the results presented in Section A.4 are related back to the theory and predictions presented in Section A.2.

The analysis section is split into six sections, the first two sections being observation of loop current behaviour and SSPC output voltage behaviour, which are intended to identify any deviations in loop current and SSPC output voltage that can be used for series arc fault detection purposes. The third section focusses on the effect of series arc faults on the load by observing load voltage behaviour. The fourth section analyses power dissipated in the arc for each test scenario in order to determine the relative severity of damage caused in each test scenario. The fifth section addresses arc voltage and electric arc stability, which is seldom discussed in the literature. Finally the sixth section remarks on the complexities of arc fault detection within power distribution panels where multiple loads are connected to the same bus bar.

A.5.1 Loop Current Behaviour

For aircraft DC secondary electrical power systems, minimum circuit breaker ratings of 2.5A are typical. Observing typical static arc characteristics for small arc lengths, indicated in Section A.2.1, a typical arc voltage V_{arc} for this current level with a small arc length of ∼1mm is approximately 15V. When an arc strikes a 15V voltage drop is introduced series with the 2.5A resistive load. In a 28VDC system the arc presents a significant increase in impedance seen by the power source and results in a reduction in loop current I_{loop} by current reduction ratio r, assuming that source

impedance Z_{src} and power feeder resistances R_{up} and R_{dn} are negligible. A generic equation for r is given by Equation (A.6), and values of r for the 28VDC and 270VDC configurations are given in Equations (A.7) and (A.8) respectively.

The results in Figures A.10(c) and A.10(d) show that the 28VDC 2.5A and 270VDC 2A load scenarios give reductions in loop current during arc strike of 1.3A and 0.1A respectively. These results align with the predictions given in Equations (A.18) and (A.19) respectively.

$$\Delta I_{loop(28V)} = r_{28V} \times I_{load} = 0.536 \times 2.5 = 1.3A \quad \text{(A.18)}$$

$$\Delta I_{loop(270V)} = r_{270V} \times I_{load} = 0.0556 \times 2.05 = 0.1A \quad \text{(A.19)}$$

Since arc voltage is supply voltage invariant and higher DC supply voltages are becoming more common on the More Electric Aircraft (MEA), the task of series arc fault detection using current measurement has become significantly more complex.

The rate at which the loop current I_{loop} changes with respect to time is determined by the arc voltage V_{arc} and the total circuit inductance L_{total} given in Equation (A.9). Assuming source inductance L_{src} is negligible, load inductance L_{load} is 12μH, and that the sum of upstream and downstream power feeders $L_{up} + L_{dn}$ is 16.25μH, total inductance L_{total} is equal to 28.25μH.

Now using Equation (A.10) which describes the electrical behaviour of an inductor, the rate of change of current I_{loop} with respect to time can be determined based on a step change in arc voltage from 0 to 15V and a total loop inductance L_{total}, and this is given in Equation (A.20).

$$\frac{dI_{loop}}{dt} = \frac{V_L}{L} = \frac{V_{arc}}{L_{total}} = \frac{15}{28.25 \times 10^{-6}} = 0.52 \times 10^6 A/s \quad \text{(A.20)}$$

It is important to note that since arc voltage V_{arc} is supply voltage V_{src} invariant, the rate of change of loop current I_{loop} with respect to time does not change when the supply voltage is varied from 28VDC to 270VDC.

This result agrees with the original prediction and therefore the requirements for an arc fault detection system based on rate of change of loop current can be defined from the maximum total loop inductance L_{total} and the minimum steady state loop current. The impact of this finding is that a maximum total loop inductance value is required in order to design a passive series arc fault detection system.

As the load current is increased in Test 3 to draw a higher steady state current of 20A at 28VDC, the introduction of a series arc into the current loop creates a higher magnitude current reduction. Figure A.11(c) shows that the loop current reduces to 10A when the arc strikes, and falls further to 7A over 1.5ms due to a small increase in

arc voltage. The predicted current reduction behaviour is calculated for a 20A load in Equation (A.21) and this correlates well with the experimental results.

$$\Delta I_{loop(28V)} = r_{28V} \times I_{load} = 0.536 \times 20 = 10.7A \tag{A.21}$$

Since the total loop inductance and line voltage within the circuit is consistent between Tests 1 and 3, the rate of change of current remains as per Test 1. The fall time of the current waveform upon striking of the arc increases due to the higher load current. This result agrees with the original prediction and means that a given passive series arc fault detection system can detect faults in systems with a range of current levels assuming that a $\frac{dI_{loop}}{dt}$ sensor with a suitable bandwidth is used.

In similarity with a comparison of Tests 1 and 3, for Tests 2 and 4 concerning a 270VDC system, where the load is increased from 2.5A to 25.25A, the reduction in loop current during a series arc fault increases. Figure A.11(d) shows a reduction in current of 1.3A during arc strike. This behaviour is predicted by Equation (A.22) for a 25A load and this closely matches the experimental results.

$$\Delta I_{loop(270V)} = r_{270V} \times I_{load} = 0.0556 \times 25 = 1.4A \tag{A.22}$$

The small difference of 0.1A between the actual and calculated current drop is caused by a variation in arc voltage V_{arc}. The significance of this finding is that the experimental results match the prediction that series arc faults in 270VDC systems cause a lower reduction in load current compared with the same series arc fault in a 28VDC system, thus making passive series arc fault detection in high voltage DC systems more difficult.

It was predicted that the introduction of inductance into any part of the current loop causes the rate of change of current during a series arc fault to decrease in accordance with Equation (A.20). The total inductance for the basic test circuits in Tests 1 and 2 can be verified by observing the fall time t_{fall} of the loop current when the arc strikes, and the fall time loop current in Test 2 is presented in Equation (A.23). Total loop resistance can be calculated by observing the source voltage and loop current and this is given approximately in Equation (A.24). Assuming that capacitance in the circuit is minimal then the circuit can be described using a first order RL model, where time constant τ is presented in Equation (A.25). The fall time in a first order RL circuit can be approximated to 5τ. Substituting Equation (A.23) into Equation (A.26) yields Equation (A.27) which allows the total loop inductance in Test 2 to be calculated.

$$t_{fall} = 0.8\mu s \tag{A.23}$$

$$R_{total} = \frac{V_{src}}{I_{loop}} = \frac{270}{2.5} = 108\Omega \tag{A.24}$$

$$\tau = \frac{L_{total}}{R_{total}} \tag{A.25}$$

$$t_{fall} = 5\tau = 5\frac{L_{total}}{R_{total}} \tag{A.26}$$

$$L_{total} = \frac{t_{fall}R_{total}}{5} = \frac{0.8 \times 108}{5} = 28.8\mu H \tag{A.27}$$

Equation (A.28) shows the fall time of loop current for Test 6, where an additional load inductance of 50μH was introduced. The total inductance is now calculated from the fall time $t_{fall(+50\mu H)}$, and is presented in Equation (A.29). Equation (A.30) verifies that the new total circuit inductance matches the introduced inductance.

$$t_{fall(+50\mu H)} = 6\mu s \tag{A.28}$$

$$L_{total(+50\mu H)} = \frac{t_{fall}R_{total}}{5} = \frac{6 \times 108}{5} = 78.8\mu H \tag{A.29}$$

$$L_{increase} = L_{total(+50\mu H)} - L_{total} = 78.8 - 28.8 = 50\mu H \tag{A.30}$$

Again the impact of this finding is that passive series arc fault detection technology which uses the rate of change of current to detect arcs is severely affected by circuit inductance, and therefore care should be taken to determine the range of system inductances which are likely to be encountered to ensure that inductive loads and long cables do not mask series arc faults from the detection system.

In similarity to the loop currents from Tests 5 and 6 featuring additional inductance downstream from the SSPC, in Tests 11 and 12 the rate of change of loop current is slower now that a 50μH inductance has been introduced upstream from the SSPC. As demonstrated earlier in this analysis, any increase in total loop inductance L_{total} results in a lower rate of change of loop current during arc strike. The fall times of the currents in Tests 11 and 12 with an additional 50μH of upstream inductance are approximately equal to the fall times in Tests 5 and 6 with an additional 50μH of downstream inductance, and therefore no further analysis is required here.

The results of Tests 7 and 8 illustrate the impact of introducing 380μF capacitive loads in parallel with the 28VDC 2.5A and 270VDC 2A loads from Tests 1 and 2 respectively. Figures A.13(a) and A.13(b) show multiple arcs striking and immediately quenching with the loop current descending to 0A in both the 28VDC and 270VDC test scenarios. It was qualitatively determined that the immediate arc quenching occurs because during arc strike, the capacitive load maintains the load voltage resulting in the inability of the upstream circuit inductance to provide sufficient voltage across the arc gap in order to maintain the arc. The original prediction does not cover capacitive load behaviour since the analysis of the test circuit was simplified to give a simple first order RL model. The introduction of a capacitive load yields a multiple order system and this finding drives the need for a SPICE simulation of the capacitive load test circuit, given in Chapter 3, to quantitatively understand this behaviour. When a reconnection of the ring tag and stud occurs the loop current rises

to a level of 15-25A, depending on the time period between extinction of the previous arc and the reconnection. A longer delay between extinction and reconnection causes a higher current peak at reconnection because the load capacitor has a longer time to discharge. It was observed that this current peak caused the ring tag and stud to flash violently due to vapourisation of the electrode material, as a result of the high current density present in the conductors at the time of reconnection, due to the low impedance of the partially discharged capacitor. After the initial current peak the loop current descends to the 2.5A steady state level of the resistive load. The high instantaneous currents cause visibly more violent series arc events, which cause damage to local wiring insulation and ring tags. Since these arcs quench immediately they are easier to detect since the change in arc current is similar in magnitude to the steady state load current.

The results of Tests 9 and 10 depicted in Figures A.14(a) and A.14(b) respectively show the effect of a series arc fault in a system employing a load with both 380μF capacitive and 50μH inductive elements. The single arc example shows how the arc duration is $\sim$250μs and how loop current then rapidly falls to zero. This effect can be seen in both the 28VDC and 270VDC power supply scenarios, and occurs due to the mechanism described in the previous paragraph. When a reconnection is made the loop current causes the inductive / capacitive load to resonate, resulting in a $\sim$22A peak and a bright flash caused by vapourisation of electrode material due to the high current density at the point of contact between electrodes.

An interesting observation in the 270VDC scenario at time 7ms in Figure A.14(b) is that the resonance of the circuit causes an arc to strike with current flowing in the anti-clockwise direction, immediately following quenching of the arc caused by loop current flowing in the clockwise direction. This is a feature which could be used to detect arcs in this scenario and as a general remark an inductive / capacitive filter is typically used at the input to each representative aircraft load in order to reduce EMC emissions and susceptibility, and therefore this effect could be investigated further.

Solid State Power Controllers (SSPCs) are protected by transient voltage suppressors, Schottky protection diodes and snubber devices, and these protection devices are designed to handle transients created by switching power at a relatively slow rate in the order of 20Hz. The series arc fault present during the capacitive and resonant load tests caused multiple transients at much higher frequencies, as determined by the arc period histograms, and as a result the SSPC protection circuitry is severely stressed. The effect of this phenomena was clearly audible in the ceramic snubber capacitors on the SSPC under test during this experiment.

A.5.2 SSPC Output Voltage Behaviour

During an arc strike event the rising edge of the arc voltage V_{arc} waveform creates an exponentially decaying transient at the output of the SSPC with a peak voltage proportional to the ratio of upstream inductance to total circuit inductance. The peak voltage at the SSPC output $\hat{V}_{sspcout}$ is given by Equation (A.12). This transient peak is caused by the instant increase in arc voltage through the total loop inductance.

$$\hat{V}_{sspcout[28V]} = 28 + 15\left[\frac{4.25}{12 + 4.25 + 12}\right] = 28 + 2.25 = 30.25V \quad \text{(A.31)}$$

$$\hat{V}_{sspcout[270V]} = 270 + 15\left[\frac{4.25}{12 + 4.25 + 12}\right] = 270 + 2.25 = 272.25V \quad \text{(A.32)}$$

In Test 1 with a source voltage of 28VDC and Test 2 with a source voltage of 270VDC, the voltage peaks caused by a series arc strike are given by Equations (A.31) and (A.32) respectively. The voltage peak is less visible in the Test 2 waveform in Figure A.10(d) due to power supply noise at a level of $3V_{p-p}$ and therefore dynamic range could be an issue with this approach. However, it should be noted here that the deviation in SSPC output voltage figure is both loop current I_{loop} and power supply voltage V_{src} invariant, and thus the peak SSPC output voltage $\hat{V}_{sspcout}$ behaviour is a characteristic which is exploitable for arc fault detection. This result supports the original predictions in Section A.2 and is important because this means that the change in voltage at the SSPC for a fixed wiring configuration is power supply voltage invariant and is a simple parameter which assists passive detection of series arc faults.

Since the voltage peak at the SSPC output $\hat{V}_{sspcout}$ is broadly loop current invariant, the voltage peaks seen for both Tests 1 and 3 in Figures A.10(c) and A.11(c) respectively are given by Equation (A.31). Similarly the voltage peaks seen for both Tests 2 and 4 in Figures A.10(d) and A.11(d) respectively are given by Equation (A.32).

Inductive loads reduce the peak seen on the SSPC output voltage $\hat{V}_{sspcout}$ since the value of the denominator in Equation (A.12) increases. Tests 5 and 6 illustrate the effect of introducing an additional 50μH of downstream inductance in the 28VDC and 270VDC scenarios respectively. The voltage peaks seen in Tests 5 and 6 are illustrated in Figures A.12(c) and A.12(d) respectively where Equations (A.33) and (A.34) provide the prediction for these two scenarios. The experimental results correlate well with the predicted voltage peak calculations.

$$\hat{V}_{sspcout[28V/50\mu H]} = 28 + 15\left[\frac{4.25}{12 + 4.25 + 62}\right] = 28 + 0.8 = 28.8V \quad \text{(A.33)}$$

$$\hat{V}_{sspcout[270V/50\mu H]} = 270 + 15\left[\frac{4.25}{12 + 4.25 + 62}\right] = 270 + 0.8 = 270.8V \quad \text{(A.34)}$$

The impact of this result is that the relatively low upstream inductance in this scenario makes detection of arc faults using this effect troublesome. In a more practical scenario where there are other SSPCs feeding multiple loads connected to the same SSPC input

bus, this will result in a further reduction of the voltage signal at the SSPC thus limiting the exploitation of this parameter for arc fault detection purposes. Power supply noise in Test 6 results in the low signal to noise ratio of the arc voltage peak with respect to the power supply noise. The power supply noise is $3V_{pk-pk}$ which represents 1.1% of the full scale source voltage, and although this is not ideal for scientific purposes, it remains an acceptable level and is within the requirements of RTCA DO-160G [49] Section 16 Power Input.

Since the series arcs within systems featuring highly capacitive loads quench very soon after they strike, the peak arc extinction voltage V_{arc} causes a much higher peak SSPC output voltage. The peak SSPC output voltage $\hat{V}_{sspcout}$ for Figure A.13(c) in Test 7 is 33V and for Figure A.13(d) in Test 8 is 277V. The peak arc voltage at quenching for Test 7 is 35V and for Test 8 is 40V, and with this information the peak SSPC output voltages can be calculated to validate the schematic model.

$$\hat{V}_{sspcout[28V/380\mu F]} = 28 + 35\left[\frac{4.25}{12+4.25+12}\right] = 28 + 5.3 = 33.3V \quad \text{(A.35)}$$

$$\hat{V}_{sspcout[270V/380\mu F]} = 270 + 40\left[\frac{4.25}{12+4.25+62}\right] = 270 + 6 = 276V \quad \text{(A.36)}$$

The positive peak SSPC output voltages during arc quench for Tests 7 and 8 are given by Equations (A.35) and (A.36) respectively, and these predicted values align well with the experimental results above. Note that the negative peaks at the SSPC output voltage in both Tests 7 and 8 are created by the reconnection of the loose terminal, and therefore the application of a partially discharged capacitive load, which creates a large positive loop current and a corresponding reduction in SSPC output voltage.

The results for Tests 9 and 10 demonstrate that excessive downstream inductance in the order of 100μH can prevent any significant influence of series arc faults on the SSPC output voltage. Care must therefore be taken when considering the use of SSPC output voltage for the purposes of series arc fault detection.

The results from Tests 11 and 12 show that it is possible to increase the peak SSPC output voltage during series arc strike compared with Tests 1 and 2 respectively by increasing the upstream inductance. The peak SSPC output voltage for Test 11 shown in Figure A.15(c) is 34V and for Test 12 shown in Figure A.15(d) is 272V (an increase of 4V from 268V steady state).

$$\hat{V}_{sspcout[28V/50\mu H_{upstream}]} = 28 + 15\left[\frac{54.25}{12+54.25+12}\right] = 38.4V \quad \text{(A.37)}$$

$$\hat{V}_{sspcout[270V/50\mu H_{upstream}]} = 270 + 15\left[\frac{54.25}{12+54.25+12}\right] = 280.4V \quad \text{(A.38)}$$

The predicted values for validation of the results for Tests 11 and 12 are higher than the actual values presented in the results. A suggested reason for this discrepancy is that the SSPC unit features a shunt resistor-capacitor (20Ω + 100nF) “snubber”

circuit which stabilises the line impedance during current limit / overload events. The snubber also limits the rate of change of SSPC output voltage, and therefore limits the peak voltage at the SSPC output for short events such as the arc strike transient. In similarity with capacitive loads, this effect can be understood by means of a SPICE modelling and simulation exercise and this is presented in Chapter 3.

In conclusion the experimental study on peak SSPC output voltage $\hat{V}_{sspcout}$ behaviour demonstrates that the results agree with the prediction and that the physical positioning of the SSPC within a given electrical system, and specifically the ratio of upstream to downstream system inductance, affects the signal level observed at the SSPC output. This implies that SSPCs positioned closer to the load than the power supply will see a relatively higher SSPC output voltage peak compared with those SSPCs positioned further from the load and closer to the power supply.

A.5.3 Load Voltage Behaviour

The load voltage prediction for each test can be expressed simply as per Equation (A.13). It was found that the experimental results for all tests agree with this prediction, where during a series arc fault the voltage across the load V_{load} falls by ∼15V. For 28VDC systems the load voltage during a series arc fault is given by Equation (A.39), and for 270VDC systems the load voltage during a series arc fault is given by Equation (A.40).

$$V_{load[28V]} = 28 - 15 = 13V \tag{A.39}$$

$$V_{load[270V]} = 270 - 15 = 255V \tag{A.40}$$

This decrease in load voltage is significant in 28VDC systems and causes the load voltage to fall below the 18VDC minimum level specified for 28VDC power quality in RTCA DO-160G [49] Section 16-23. Operation below 16VDC will typically cause an intelligent load to shut down, although this is dependent upon the length of interruption. The impact of a series arc fault is therefore likely to be seen at the load and the effects of the series arc fault are likely to be found by maintenance staff during the fault diagnosis process before persistent arcing causes severe damage.

A 270VDC load is typically specified to run down to an average voltage level of 235VDC as specified by RTCA DO-160G [49] Section 16-23. The effect of a series arc fault reduces the nominal 270VDC down to 255VDC, which is well within normal operation requirements. Given that series arc faults in 270VDC systems do not quench readily, it is likely that the effects of a series arc fault would not be noticed until severe damage has occurred, since the fault can continue undetected. This finding is a major contributor to the requirement for series arc fault detection in high voltage DC systems on the More Electric Aircraft (MEA) and/or All Electric Aircraft (AEA).

A.5.4 Power Dissipated in the Arc and Event Frequency

According to the prediction in Section A.2.6 the instantaneous power dissipated in the arc can be calculated approximately with Equation (A.14). Since arc power P_{arc} is supply voltage invariant and for small arc gaps (∼1mm) with loop currents greater than ∼1A the arc voltage remains at ∼15V, the power dissipated is comparable for series arcs in 28VDC and 270VDC systems given similar loop currents. The instantaneous arc power dissipated for the Test 1 and 2 example arcs illustrated in Figures A.10(c) and A.10(d) respectively can be calculated with Equation (A.41).

$$P_{arc} \quad = \quad 15 \times 1 = 15W \tag{A.41}$$

The corresponding energy dissipated by the example arc in Test 1 Figure A.10(c) can then be approximated using Equation (A.42). Similarly the corresponding energy dissipated by the example arc in Test 2 Figure A.10(d) can then be approximated using Equation (A.43).

$$Q_{arc[Test1]} \quad = \quad \int_{t_{strike}}^{t_{quench}} P_{arc}dt = 15 \times \left(3.1 \times 10^{-3}\right) = 46.5 \times 10^{-3}J \tag{A.42}$$

$$Q_{arc[Test2]} \quad = \quad \int_{t_{strike}}^{t_{quench}} P_{arc}dt = 15 \times \left(3.2 \times 10^{-3}\right) = 48.0 \times 10^{-3}J \tag{A.43}$$

Comparing Equations (A.42) and (A.43) shows that arcs in 28VDC and 270VDC systems with similar loop currents and durations dissipate a similar amount of energy and therefore cause a similar amount of damage. The results here match the prediction in Section A.2.6 and create a link between arc duration and damage caused, and also between arc frequency and the rate at which damage is caused, which interestingly is power supply voltage V_{src} invariant. However, it must be noted that systems with higher power supply voltages can sustain arcs for longer periods without quenching due to arc instability.

It was predicted in Section A.2.7 that event frequency is highly dependent on the random vibration power spectral density profile and the mechanical structure of the arc electrodes. The arc period and duration histograms are intended to be a basic relative method for determining how, for a fixed mechanical environment, variations in electrical configuration affect the distribution of arcs in a fixed three second time period. Comparing the three second histograms for Tests 1 and 2, representing 28VDC 2.5A and 270VDC 2A resistive load scenarios respectively, the 28VDC system exhibits 598 arcs compared with the 270VDC system where 1002 arcs were present. It can also be observed that the mean arc duration in the 270VDC system is 1.36ms, which is less than the 1.98ms mean arc duration in the 28VDC system.

For the 28VDC 20A resistive load scenario in Test 3 the loop current during the series arc fault is approximately 8A as determined in Figure A.11(c). For the 28VDC

2.5A resistive load scenario in Test 1 the loop current during a series arc fault is approximately 1A as illustrated in Figure A.10(c), and therefore the arc power and energy for a given arc in Test 3 is approximately eight times greater than that in Test 1 demonstrating that arc power and energy is proportional to the arc current.

Comparing the three second histograms for Tests 1 and 3 reveals that the 28VDC system with a 2.5A steady state load current experienced 598 arcs and the 28VDC system with a 20A steady state load current experienced 280 arcs. It can be observed that the mean arc durations for Tests 1 and 3 are comparable at 1.98ms and 2.13ms respectively, but arc periods vary more significantly with mean arc periods for Tests 1 and 3 of 5ms and 10.8ms respectively, where the variation is due to the interaction of the electrical and mechanical domains. The arcs created in Test 3 with a 20A load current were visibly more violent by comparison to those in Test 1 with a 2.5A load current due to the increased arc power, and it was visible during testing that the higher load current, and hence higher current density at the point of reconnection, resulted in localised spot welding of the electrodes during reconnection which prevented the consistent arcing behaviour seen during Test 1. This interaction explains the extended arc periods and reduced number of arcs seen in Test 3.

For the 270VDC system with a 25A resistive load in Test 4, the current during a series arc fault is approximately 24A as illustrated in Figure A.11(d). For the 270VDC system with a 2A resistive load in Test 2, the current during a series arc fault is approximately 1.95A as illustrated in Figure A.10(d) and therefore the arc power and energy for a given arc in Test 4 is approximately twelve times greater than that in Test 2.

Comparing the three second histograms for the Tests 2 and 4 reveals that the 270VDC system with a 2A steady state load current experienced 1002 arcs, and the 270VDC system with a 25A steady state load current experienced 283 arcs. The mean arc periods for Tests 2 and 4 are 10.5ms and 2.96ms respectively, and the mean arc durations are 0.44ms and 1.36ms respectively. It can be observed that arc durations are comparable between tests, but there is a greater spread of arc periods due to the interaction of electrical and mechanical domains. It was visible during testing that the higher load current, and hence higher current density at the point of reconnection, resulted in localised spot welding of the electrodes during reconnection which limited the consistent arcing behaviour seen during Test 2. It is proposed that this interaction caused the extended arc periods and reduced number of arcs seen in Test 4.

The arc power and energies for individual arcs with equal durations in both 28VDC and 270VDC systems, with and without 50μH inductive loads as per Tests 5 and 6, and Tests 1 and 2 are comparable since inductive loads affect transient arc behaviour and not the steady-state arc current and voltage.

Comparing the three second histograms for the Tests 1 and 5 reveals that the 28VDC system with a 2.5A steady state load current experienced 598 arcs, and the 28VDC system with a 2.5A steady state load current and a 50μH inductive load experienced 499 arcs. Similarly comparing the three second histograms for the Tests 2 and 6 reveals that the 270VDC system with a 2.5A steady state load current experienced 1002 arcs, and the 270VDC system with a 2.5A steady state load current and a 50μH inductive load experienced 598 arcs. The mean arc durations for Tests 5 and 6 were 2.9ms and 2.4ms respectively and these are comparable to Tests 1 and 2 which featured mean arc durations of 1.98ms and 1.36ms respectively. This is an important discovery which means that arcs in 270VDC systems with resistive loads have durations approximately 45% longer than those of arcs in 28VDC systems due to the additional stability provided by the higher power supply voltage. The introduction of 50μH inductive loads also increases arc duration in both 28VDC and 270VDC systems by approximately 46% and 20% respectively. The mean arc periods of series arcs in Tests 5 and 6 with 50μH inductive loads are 6ms and 11.7ms respectively, where these represent longer mean arc periods than the 5ms and 3ms in Tests 1 and 2. There is also a greater spread of arc periods in 270VDC systems with inductive loads compared to those with purely resistive loads.

The method of automated arc duration and arc period measurement which allows a statistical analysis to be presented was not run on Test 7 since the accuracy of this analysis is questionable under the given scenario. It was difficult to identify arcs visually when observing the recorded waveforms, and the chosen feature extraction method was not sufficient to extract the relevant data for very short arc durations.

Qualitatively the arc power and energies of individual equal duration arcs with power supply voltages of 28VDC and 270VDC and capacitive loads in Tests 7 and 8 are typically lower than the power and energies of those in Tests 1 and 2 with purely resistive loads because arcs in Tests 7 and 8 are of much shorter duration, and quench almost immediately after arc strike due to the load capacitance. Significantly more energy is delivered into the loose contact during contact reconnection, due to the low impedance of the partially discharge capacitor.

The mean arc duration for the 270VDC capacitive load scenario in Test 8 is 0.65ms which is significantly less than 1.36ms for the 2.5A resistive load scenario in Test 2. The arc periods in Test 8 show a greater spread compared with those in Test 2, where the mean arc period for Test 8 is 21.8ms compared with 2.97ms for Test 2.

The mean arc periods for the resonant LC load scenarios in Tests 9 and 10 are greater than those in Tests 1 and 2, with values of 337ms and 5ms as opposed to 5ms and 3ms respectively. The mean arc durations are also short with values of 1.98ms for Test 9 and 0.54ms for Test 10 where a resistive / capacitive load is fitted. The short arc durations are again due to the presence of the capacitive load.

Arc power and energies in experiments with inductive / capacitive loads are typically lower than those in tests with purely resistive loads since the the load capacitor prevents arcs from being maintained thus the arc durations are very short, and therefore the arc energies are not possible to measure using the technique proposed in the experimental method given in Section A.3.3.

The relevance of the findings in Tests 7 through 10 is that where arcs are difficult to identify in systems with resistive and inductive loads, the introduction of capacitance to the load allows arcs to quench more readily, thus providing a much larger loop current change during arc strike / quench which makes series arc faults easier to detect passively.

Arc power and energies in Tests 11 and 12 where upstream wiring inductance is increased are comparable to Tests 1 and 2 with purely resistive loads therefore no further analysis is required.

Arc periods and durations for Tests 11 and 12 are longer in comparison with those in Tests 1 and 2, with fewer arc in total. Mean arc duration for Tests 11 and 12 are 6.9ms and 5.6ms compared with 1.98ms and 1.37ms for Tests 1 and 2. Mean arc period for Tests 11 and 12 are 21.7ms and 14.1ms compared with 5.1ms and 3ms for Tests 1 and 2 respectively. For Test 11 there were 214 arcs, and for Test 12 there were 139 arcs compared with Test 1 with 882 arcs and Test 2 with 1238 arcs. In terms of damage caused, there were fewer arcs, but the arc durations were longer and therefore more energy was released.

In conclusion the analysis of the experimental data has determined that capacitive loads in particular affect arc periods and durations and thus the mechanical behaviour in the system. The impact of this finding is that any arc fault detection algorithm should be tolerant of varying arc periods and durations, and should consider that arc periods can vary significantly depending upon load characteristics.

A.5.5 Arc Voltage and Electric Arc Stability

Tests 1 and 2 cover 28VDC 2.5A and 270VDC 2A resistive load scenarios respectively. The experimental data shows that electric arcs within 270VDC power systems are significantly more stable when compared with electric arcs in 28VDC systems. Out of the 598 electric arcs present in the 3s window of series arcing in the 28VDC system 208 are quenched, whereas in the 270VDC system out of 1002 arcs present during the test run no arcs are quenched and this can be clearly seen in Figure A.10(b). Figure A.10(d) shows how a single arc within the 100ms window strikes, burns for 3.2ms and is finally extinguished upon reconnection of the two electrodes. Quenching arcs can be easily identified by a zero current event. The mean arc strike voltage for the 28VDC system is 29.6V, with a maximum arc strike voltage of 97.9V, in contrast with

the mean arc strike voltage of 23.5V and maximum arc strike voltage of 55V in the 270VDC system suggesting that stable arcs form more readily in higher voltage DC systems. The mean arc quench voltage in the 28VDC system in Test 1, Figure A.10(a) is 247.6V with peak arc extinction voltages reaching 390.4V. Note that the voltage across the arc can exceed the power supply voltage due to the fast change in loop current through the total system loop inductance. The peak arc extinction voltage measurements are likely to be inaccurate since the peak arc extinction voltage occurs only for a very short duration, the measurement system has a limited bandwidth of 50MHz and sampling period of 10ns, and furthermore the parasitic differential probe input capacitance and probe lead inductance used provides a leakage path between the arc electrodes thus limiting the peak arc voltage.

In contrast to Test 1 at 28VDC with a 2.5A loop current, the arcs illustrated for Test 3 with a 20A loop current illustrated in Figure A.11(c) do not quench due to the increased loop current, and therefore arc power which allows the arc to maintain temperature and continue burning, where the low current arc suffers from poor stability due to the lower arc temperature. Out of the 280 total arcs in Test 3 with a 20A loop current, none of the arcs quench with all arc electrodes reconnecting the circuit. The total number of arcs in the 28VDC 20A scenario is 280, which is approximately half that of the 598 arcs in the 28VDC 20A scenario. This implies that the higher current prevents arcs from striking and it is proposed that this is due to local and permanent welding of the arc electrodes at the point of reconnection which are then able to resist the vibration induced arcing. When this local welding occurred the author had to stop the vibration stimulus and apply significant force to free the ring tag from the bolt thread. The mean arc strike voltage for the 28VDC 2.5A scenario in Test 1 is 29.6V as opposed to 19.4V for the 28VDC 20A scenario in Test 2, suggesting that higher current loads lead to more stable arcs in 28VDC systems. The mean arc quench voltage in the 28VDC system at 2.5A in Test 1, Figure A.10(a) is 247.6V, and the mean arc reconnection voltage in the 28VDC system at 20A in Test 3 is 13.8V.

In similarity with Test 2 at 270VDC with a 2.5A loop current, the arcs illustrated for Test 4 with a 25A loop current illustrated in Figure A.11(d) do not quench. There is therefore consistent stability and arc behaviour for 270VDC series arcs across the range of current levels, which is ideal from an arc fault detection point of view, but is of concern since even 2.5A arcs consistently cause damage. The total number of arcs is 1002 in the 270VDC 2.5A scenario and 283 in the 270VDC 25A scenario, which again shows that the higher current prevents arcs from striking as described previously. The mean arc strike voltage for the 270VDC 2.5A scenario in Test 2 is 23.5V as opposed to 20.5V for the 270VDC 25A scenario in Test 4 suggesting that higher current loads lead to more stable arcs in 270VDC systems. In the absence of quenching arcs, the mean arc reconnection voltage in the 270VDC system at 2.5A in Test 2, Figure A.10(a) is 18.5V, and the mean arc reconnection voltage in the

270VDC system at 25A in Test 4 is 16.1V. This again suggests that higher current loads lead to more stable arcs in 270VDC systems.

The addition of a 50μH inductive load appears to significantly affect the arc stability of Test 5 at 28VDC compared with Test 1 at 28VDC in that only 151 out of 499 arcs quench as opposed to the 208 out of 348 arcs which quench to an open circuit in the absence of the additional inductive load which suggests that the stored magnetic energy in the increased loop inductance increases arc stability. The addition of a 50μH inductive load to Test 6 at 270VDC compared with Test 2 at 270VDC shows little difference in stability since none of the arcs present in either scenario quench. Of particular interest is that Test 6 with additional load inductance shows 251 total arcs as opposed to 1002 arcs present without load inductance. It is proposed that in similarity to higher current loads, the addition of load inductance creates a more violent arc at electrode reconnection which leads to a stronger spot weld which resists the effects of vibration induced arcing. The mean arc strike voltages for Tests 5 and 1 are 25.9V and 29.6V respectively and the mean arc strike voltages for Tests 6 and 2 are 15.7V and 23.5V respectively, this shows that arcs strike more stably when additional load inductance is present in the circuit under test. The mean arc quench voltage in Test 5 is 358V compared with 247.6V in Test 1, which is to be expected given the additional stored energy in the load inductance which helps to maintain arcing. In the absence of quenching arcs in Tests 6 and 2, the arc reconnection voltage with an inductive load is 10.4V as opposed to 18.5V without the additional load. Comparing the loop current waveform for Tests 5 and 1 also shows how during arc quench the curve representing current converges to zero current more slowly compared with the fast step shown in Test 1 Figure A.10(c) due to the energy storage in the inductor prolonging the arc and slowing the rate of change of loop current.

The addition of load capacitance to the 28VDC 2.5A resistive load Test 1 and 270VDC 2.5A resistive load Test 2 results in the behaviour captured in Tests 7 and 8 where arcs quench more readily following strike regardless of the 28VDC or 270VDC power supply voltage. For this reason the production of arc statistics for Test 7 in Tables A.4 and A.5 was not possible due to poor feature extraction. Out of 137 arcs present in Test 8, 112 arcs quenched and therefore the introduction of capacitive loads to the circuit causes instability since in the absence of the capacitive load there are no quenching arcs. The mean arc strike voltage for Test 8 was 19.1V, compared with 29.6V in the absence of the capacitive load. Upon quenching arcs in Test 8, the mean arc extinction voltage is in the order of 44.1V, with maximum values of 111V observed. The capacitive load also results in formation of a weld created by an arc at the point a reconnection occurs, and this can be seen in Figure A.13(d) at time 9.2ms. This result is of particular interest since the introduction of capacitance to 270VDC systems could be promoted in order to ensure that series arcs always quench

for the range of possible load configurations thus making passive arc fault detection a simpler operation.

The results of Tests 9 and 10 which test 28VDC and 270VDC inductive-capacitive load scenarios are comparable with the capacitive load test results in Tests 7 and 8 due to the presence of a common high load capacitance. The inductive-capacitive resonant load causes arcs in the 270VDC scenario to quench where before they were stable. The number of arcs experienced in Tests 9 and 10 are fewer than those arcs produced in Tests 1 and 2 respectively. Test 10 particularly shows that the resonant load causes welding of the arc electrodes which greatly reduces the number of arcs seen in this scenario. Figure A.14(d) shows an arc at time 2.25ms in Test 10 which creates a weld at the point of reconnection. The mean arc strike voltages are broadly similar in Tests 9 and 10 at 20.3V and 24.1V respectively, and in turn the arc strike voltages for Tests 1 and 2 are also similar at 29.6V and 23.5V respectively. Arcs quench more readily, and the arc quench voltages for Tests 9 and 1 are 241.1V and 247.6V respectively and are thus very similar. The reactive load causes arcs in the 270VDC scenario to reliably quench.

In similarity with the effect of increasing load inductance the 28VDC results in Test 11 and 270VDC results in Test 12 with an additional upstream inductance of 50μH are similar to the 28VDC and 270VDC resistive load results in Tests 1 and 2 respectively. Tests 11 and 1 feature 214 and 598 arcs respectively, and tests 12 and 2 feature 139 and 1002 arcs respectively therefore fewer arcs are produced in the scenarios with upstream inductance thus proving a strong interaction between the electrical and mechanical systems. The mean arc strike voltage for Tests 11 and 1 are 25.3V and 29.6V respectively, showing that increased upstream inductance or wiring creates a lower arc strike voltage and hence a more stable arc strike. For Tests 12 and 2 the mean arc strike voltages are 20.8V and 23.5V again showing that upstream inductance results in more stable arc strike. With regard to arc quenching behaviour, the addition of upstream inductance does not cause the 270VDC system to quench and therefore all the arcs in Test 12 reconnect without quenching. The mean arc quench voltages for Tests 11 and 1 are 208.8V and 247.6V respectively suggesting that the arc quench voltage is reduced by the increase in upstream inductance in the 28VDC system.

It was noted that the accuracy and validity of arc voltage measurements is limited due to the interaction between the arc voltage and the isolated differential voltage probe used for arc voltage measurement. This interaction was minimised by using high impedance probes, however the 10MΩ probe resistance and 10pF probe capacitance load the arc significantly during arc strike and arc quench where arc impedance is high and arc current is near zero. It is later shown during the modelling activity in Chapter 3 that the probe impedance results in over-reading of arc voltage by a factor of approximately two during arc strike due to the interaction of the probe lead

inductance and the 10pF probe capacitance. The presence of the differential probe also excites a short duration high frequency resonance (in the order of 5MHz) during arc strike and arc quench which is manifested by the presence of the arc voltage probe. Where other researchers have characterised high frequency content present in the arc voltage and arc current waveforms as a sign of electrical arcing, it was anticipated that this behaviour is influenced heavily by the presence of any measuring apparatus.

A.5.6 Effect of Multiple Loads on a Power Distribution Panel Bus

The results showed that increased downstream wiring and load inductance slowed the rate of change of current, and reduced the magnitude of the voltage spike seen at the SSPC output during arc strike thus making both current and voltage detection difficult. The addition of upstream wiring inductance also reduced the rate of change of current during arc strike thus complicating current detection, but increased the magnitude of the voltage spike seen at the SSPC output thus simplifying voltage based detection.

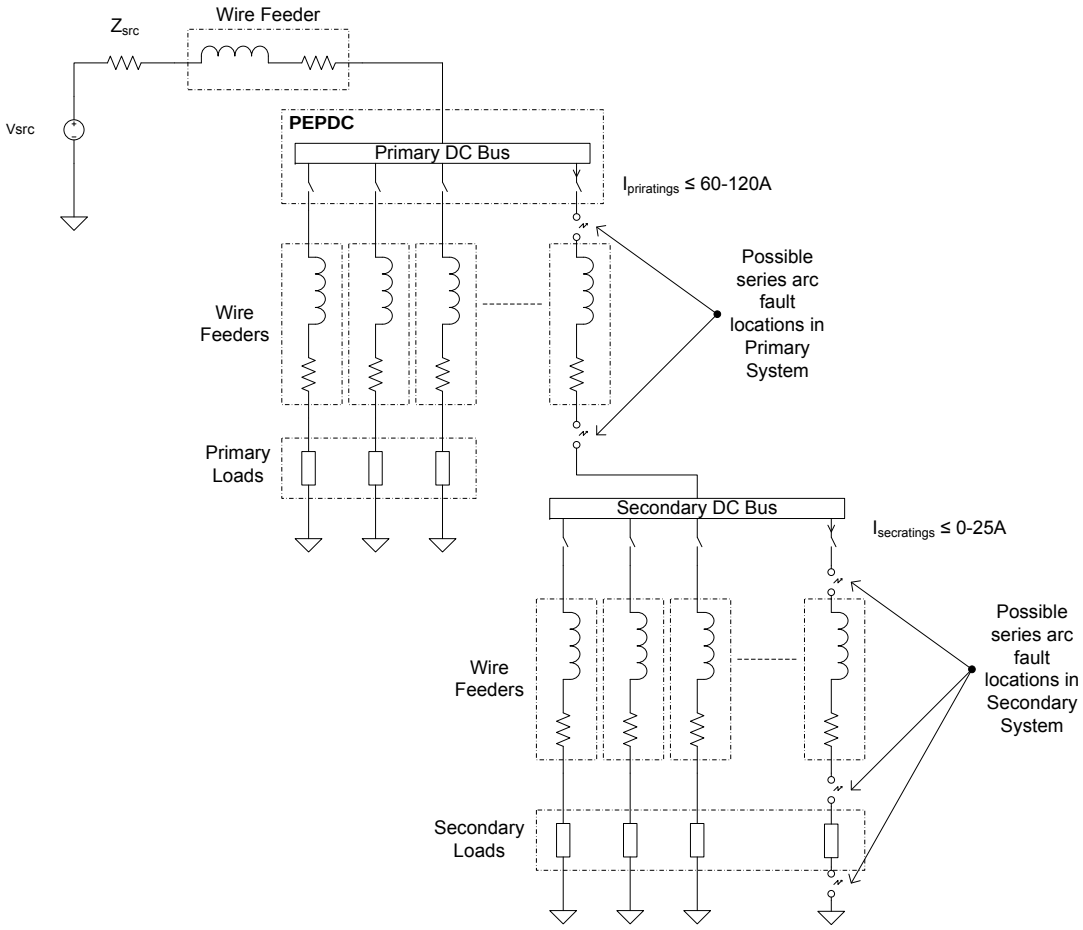


Figure A.27: Detecting Series Arc Fault in a Representative Architecture

These results tie in with the parallel issue of the physical electrical power distribution panel configuration facing series arc fault detection. Typical narrowbody and wide-body aircraft electrical power distribution systems have a dual-lane two tier fanout configuration. For the sake of illustration Figure A.27 shows a single lane system with a primary and secondary distribution panel.

The purpose of the work carried out to identify the effect of upstream and downstream inductance on series arc behaviour now becomes clear since arcs in the secondary system are easier to detect at the secondary SSPC outputs due to a high level of upstream inductance back through to the generator. Series arcs on primary loads are more difficult to detect at the primary SSPC outputs due to the lower ratio of upstream to total loop inductance, which in turn results in a smaller voltage signal at the SSPC output. The issue of series arc fault detection becomes further hampered by the presence of parallel loads on a given bus. The primary bus has several outputs and each output has a level of inductance, either provided by the given primary load itself, or by the wire feeders, which in turn load the primary bus and form a parallel inductance with the other inductive loads. This parallel inductance further reduces the level of arc voltage V_{arc} which is developed at the output of a given primary SSPC output, thus making the series arc faults more difficult to detect.

A.5.7 Additional Observations

Two interesting observations were made which were not part of the main scope of the characterisation activity. Firstly it was determined during testing that RLC loads and RL loads cause audible stress in the form of a "cracking" sound to the SSPC snubber components each time an arc strikes. This threat is not considered as part of the standard SSPC design process and thus excessive exposure to series arcing could cause damage to the SSPC hardware. Secondly during testing of resonant RLC loads it was observed during arc quench that the resonant nature of the load can result in the strike of a second arc in negative polarity during electrode reconnections due to the high stored energy levels in the circuit under test and the high current densities at the point of reconnection.

A.6 Chapter Summary

In this chapter the effects of series arc faults on a typical DC aircraft power distribution system have been evaluated using a simulated aircraft electrical power distribution system containing a representative loose terminal series arc fault.

Loop current behaviour was predicted from the test schematic and it was experimentally verified that, since arc voltage is consistent for the range of loop currents used in the experiments presented, the loop current reduces by 54% during series arc faults in 28VDC systems, and 5.6% during series arc faults in 270VDC systems. The rate of change of loop current was found to be directly proportional to total system inductance and line voltage. Higher line voltages and lower total system loop inductance lead to a faster rate of change of loop current, and conversely lower line voltages and higher inductances lead to a slower rate of change of loop current and make detection of these faults more complex.

Arc voltage was found to be line voltage invariant and therefore similar steady state arc voltages were seen in both 28VDC and 270VDC systems. Arc strike voltages appeared to be significantly higher than the predicted steady state conditions and therefore appeared to offer an opportunity for arc fault detection. However this is later found in Chapter 3 to be due to the interaction of the differential probe and the arc voltage. Mean arc strike voltages ranged from 15.7V through 29.6V across the different range of low / high current loads and differing reactive loads. Peak arc strike voltages of up to 97.9V were also seen in the case of unstable 28VDC 2.5A load tests and 28VDC capacitive load tests. Lower loop current, lower system inductance and higher load capacitance all promote unstable behaviour which results in higher arc strike voltages, and thus higher deviations in the SSPC output voltage waveforms during arc strike. Arc quench voltages tend to become higher for higher load inductances, and are lower for higher upstream inductance scenarios. Higher arc quench voltages assist in series arc fault detection since a proportion of the these are also present on the SSPC output voltage. Arc reconnection voltages occur when a given series arc does not quench and are approximately in line with the equivalent arc strike voltages. The mean arc reconnection voltages range from 13.8V through 28.4V for the full range of test conditions.

During arc strike a ratio of the arc voltage is presented at the SSPC output where the ratio of arc voltage presented on the SSPC output voltage is determined by dividing the upstream inductance value by the total system inductance. The experimental data showed that arc strike voltage can be in excess of the steady state arc voltage, and this provides the arc fault detection system with a larger signal for detection purposes. To ensure a suitable voltage transient magnitude at the SSPC output, downstream inductance should be minimised and upstream inductance should be maximised. The

location of the power distribution panel therefore affects the magnitude of the SSPC output voltage deflection present at arc strike. This implies that the power distribution panel should be mounted as close to the loads as possible to maximise the upstream to total inductance ratio, thus maximising the SSPC output voltage peak deflection due to a given series arc fault.

Load voltage was determined to be equal to the supply voltage minus the arc voltage, and in 28VDC systems with a typical 15V arc voltage, the load sees 13V for a given arc duration which creates an abnormal supply condition in line with RTCA DO-160G [49] Section 16. In 270VDC systems an arc voltage of 15V results in a load voltage of 255V which is within the normal operating range of a 270VDC bus in accordance with RTCA DO-160G [49] Section 16, and therefore the load may continue to function without any disruption or indication that a series arc fault is present in the system.

Under low current conditions in the order of 2.5A series arcs are more stable where higher supply voltages are used. Series arcs in 28VDC systems are not sustained and readily quench within a short time in contrast to 270VDC systems where 100% of arcs are sustained until reconnection of the loose terminal. Higher load currents increase stability within 28VDC systems and reduce the number of quenching arcs due to the availability of more energy to maintain arc stability. The introduction of upstream, downstream and/or load inductance improves the stability of series arcing in 28VDC and 270VDC systems due to the introduction of stored energy which maintains current flow through the arc in the event of loop current fluctuations thus avoiding instability.

An important discovery is that while series arcs exist in 28VDC and 270VDC systems with the same load currents they dissipate similar levels of power. Arcs in 270VDC systems do not quench as readily as those in 28VDC systems at equal current levels, thus determining that if a loose terminal continued arcing undetected there is a risk that a drawn arc could be established which may not quench.

The introduction of load capacitance promoted quenching of series arc faults in both 28VDC and 270VDC scenarios since the load capacitance maintained the load voltage during arc strike, and this resulted in arcs quenching rapidly immediately after striking. This effect reduced the energy dissipated in each arc and therefore reduced the damage caused by arcing.

The frequency (or period) of arcing events varied throughout the tests carried out and was most affected by the introduction of both capacitive and resonant loads. When the current level was raised from 2.5A to 25A, series arcs were less frequent due to welding of the electrodes during contact reconnection. The mean duration of arcs was also broadly consistent throughout the tests carried out, with the exception of the introduction of inductive loads, where arc durations were increased substantially due

to more stable arcs enabled by the magnetic energy stored in the system. Capacitive loads tended to reduce mean arc duration by destabilising the arcs.

The variation in frequency and duration of arcing events with loop current implies that there is an interaction between the electrical and mechanical systems. The configuration of the mechanical system including minor details such as cable gauge, cable fixings and cable terminations will affect the durations of and periods between arcs. Position of cable looms on the aircraft will also determine vibration levels which can vary wildly between different sections of the airframe. The mechanical scheme presented in this chapter allows baseline characteristics to be presented.

Where multiple SSPCs and loads are connected to the primary electrical distribution panel, this introduces additional load inductance and wire feeder inductance which loads the primary power bus. The effect of this parallel inductance is to reduce the voltage signal seen at a given primary SSPC output for a given series arc fault in the primary system thus making series arc fault detection more difficult. The speed of the $\Delta\hat{V}_{sspcout}$ pulse appears to be unaffected by the introduction of further load inductance, so detection of the fast edge is still worthy of investigation.

Since it was determined in the analysis of Tests 7, 8, 9 and 10 that the introduction of load capacitance causes series arc faults in both 28VDC and 270VDC systems to quench more readily, further work is recommended to characterise the minimum load capacitance required to consistently quench series arcs in 28VDC and 270VDC electrical power distribution systems under a representative range of cabling and load inductance. Designing the electrical distribution system to naturally quench arc faults will not only make series arc faults more easily detectable. High voltage DC electrical power system designers typically strive to reduce load capacitances in order to simplify generator design, and therefore there may be a conflict of interest between subsystem designers in realising this as a possible series arc fault detection solution.

A.7 MATLAB Script to Extract Arc Period and Duration, Arc Strike, Quench and Reconnection Voltages from Recorded Arc Data

Listing A.1: PlotGenesisDIDTArc_StateMachine_Histo_Test1.m

```
%%%
```

```
41
42 % Select the next recording number...
43 recnum = 372;
44
45 % Load offset compensation data...
46 load(['I:\Arc Fault Data\OffsetData.mat'],'offset');
47
48 % Load main arc fault recordings... Unzip if necessary...
49 %unzip(['Recording' num2str(recnum) '.zip'],'.');
50 load(['I:\Arc Fault Data\Recording' num2str(recnum) '.mat'],'Recorder1')
       ;
51 Ts = Recorder1.Channels.Segments.Data.dXstep;
52 Fs = int32(1/Ts);
53
54 % Define start and stop times for plot...
55 start_time_sec = 0.0;
56 stop_time_sec =  2.995;
57
58 startsample = ((start_time_sec*Fs)+1);
59 endsample = ((stop_time_sec*Fs));
60 Recorder1.Channels.Segments.Data.Samples = Recorder1.Channels.Segments.
       Data.Samples(1,startsample:endsample) - offset(1);
61 load(['Recording' num2str(recnum) '.mat'],'Recorder2');
62 Recorder2.Channels.Segments.Data.Samples = Recorder2.Channels.Segments.
       Data.Samples(1,startsample:endsample) - offset(2);
63 load(['Recording' num2str(recnum) '.mat'],'Recorder3');
64 Recorder3.Channels.Segments.Data.Samples = Recorder3.Channels.Segments.
       Data.Samples(1,startsample:endsample) - offset(3);
65 load(['Recording' num2str(recnum) '.mat'],'Recorder4');
66 Recorder4.Channels.Segments.Data.Samples = Recorder4.Channels.Segments.
       Data.Samples(1,startsample:endsample) - offset(4);
67 Recorder4=Recorder3;
68
69 % Open a statistics log file for output...
70 fid_log = fopen('I:\Arc Fault Data\Test1_Extracted.txt','wt');
71 % fprintf(fid_log, 'Total Arcs & Arcs Quenched & Arcs Reconnected & Min
       Arc Period & Mean Arc Period & Max Arc Period & Min Arc Duration &
       Mean Arc Duration & Max Arc Duration & Min Arc Strike Voltage & Mean
       Arc Strike Voltage & Max Arc Strike Voltage & Min Arc Quench Voltage
       & Mean Arc Quench Voltage & Max Arc Quench Voltage & Min Arc
       Reconnect Voltage & Mean Arc Reconnect Voltage & Max Arc Reconnect
       Voltage\\\\\n');
72
73 %%
74 % Initialise other variables...
75 periodcount_started = 0;
76 durationcountstarted = 0;
77 counter_period = 0;
78 counter_duration = 0;
79 perioddata = 0;
```

```
80  durationdata = 0;
81  periodtime = zeros(1,endsample-startsample+1);
82  durationtime = zeros(1,endsample-startsample+1);
83  periodarraycount = 1;
84  durationarraycount = 1;
85  last_recorded = 'none';
86
87  % Define state machine states...
88  state_start = 'state_start';
89  state_struck = 'state_struck';
90  state = state_start;
91
92  % Define state machine events...
93  event_posdvdtnegdidt = 'event_posdvdtnegdidt';
94  event_negdvdtposdidt = 'event_negdvdtposdidt';
95  event_noevent = 'event_noevent';
96  event = event_noevent;
97
98  % Define new sampling rate Fdec for analysis and decimate...
99  Fdec=225000;
100 n=Fs/Fdec;
101 y=decimate(Recorder1.Channels.Segments.Data.Samples(1,:),double(n),'FIR
        ');
102 z=decimate(Recorder4.Channels.Segments.Data.Samples(1,:),double(n),'FIR
        ');
103
104 % Differentiate the arc current and voltage signals...
105 a=[1];
106 b=[1 -1];
107 yd = filter(b,a,y);
108 zd = filter(b,a,z);
109
110 % Create state machine monitor signals...
111 arc_struck_monitor = zeros(1,length(yd));
112 arc_quenched_monitor = zeros(1,length(yd));
113 arc_reconnected_monitor = zeros(1,length(yd));
114
115 % For every sample in the afddata array...
116 for i=2:1:length(yd)
117
118     % DEBUG - Stop at a given time
119     %if (i/Fdec >= 0.0046)
120     %    f = 0;
121     %end
122
123     % Determine events...
124     if (yd(1,i-1) > 5.5)  && (zd(1,i-1) < -2) %&& (zd(1,i) < 5.5)&& (yd
            (1,i) > -2)
125         event = event_posdvdtnegdidt;
```

```
126     elseif (yd(1,i-1) < -5.5) && (zd(1,i-1) > 2) %&& (yd(1,i) < 5.5) &&
            (zd(1,i) > -2)
127         event = event_negdvdtposdidt;
128     else
129         event = event_noevent ;
130     end
131
132     % Switch on state...
133     switch(state)
134
135         % State 'start' - waiting for arc
136         case state_start
137
138             % Switch on event...
139             switch(event)
140
141                 % Positive dV/dt - Negative dI/dt...
142                 case event_posdvdtnegdidt
143
144                     % If last sample also showed a strike then ignore
                            arc...
145                     if (arc_quenched_monitor(i-1) ~= 1)
146
147                         % Store period counter and reset counter...
148                         if (periodcount_started == 1)
149                             % DEBUG - Stop at a given minimum period
150                             %if ((counter_period/Fdec) >= 0.16)
151                             %   counter_period/Fdec
152                             %   i/Fdec
153                             %end
154                             perioddata(periodarraycount) = (
                                    counter_period / Fdec) * 1000; % Scale
                                    histogram into milliseconds...
155                             periodtime(i) = 1;
156                             periodarraycount = periodarraycount + 1;
157                             counter_period = 0;
158                         end
159
160                         % First arc encountered...!
161                         periodcount_started = 1;
162
163                         % Arc struck...
164                         state = state_struck;
165
166                         % Create arc struck monitor pulse...
167                         arc_struck_monitor(i) = 1;
168                         last_recorded = 'struck';
169
170                     end
171
```

```
172                 % Negative dV/dt - Positive dI/dt...
173                 case event_negdvdtposdidt
174
175                     % Spurious event or reconnection of line voltage to
                            load...
176                     state = state_start;
177
178                     % If last event was a quench...
179                     if strcmp(last_recorded, 'quenched') == 1
180                         % Create arc reconnected monitor pulse...
181                         arc_reconnected_monitor(i) = 1;
182                         last_recorded = 'reconnected';
183                     end
184
185                 % No event...
186                 case event_noevent
187
188                     % Ensure that the first arc has occurred...
189                     if (periodcount_started == 1)
190
191                         % Increment counters...
192                         counter_period = counter_period + 1;
193
194                     end
195
196             end
197
198         % State 'struck' - arc struck
199         case state_struck
200
201             % Switch on event...
202             switch(event)
203
204                 % Positive dV/dt - Negative dI/dt...
205                 case event_posdvdtnegdidt
206
207                     % If last sample also showed a strike then ignore
                            arc...
208                     % AND the arc is not quenched if the absolute arc
209                     % voltage is not greater than 0.9 * Vline
210                     if ((arc_struck_monitor(i-1) ~= 1)) && (y(i) > (
                            Vline*0.9))
211
212                         % Arc quenched...
213                         state = state_start;
214
215                         % Store duration counter and reset counter...
216                         durationdata(durationarraycount) = (
                                counter_duration / Fdec) * 1000; % Scale
                                histogram into milliseconds...
```

```
217                         durationtime(i) = 1;
218                         durationarraycount = durationarraycount + 1;
219                         counter_duration = 0;
220 
221                         % Create arc quenched monitor pulse...
222                         arc_quenched_monitor(i) = 1;
223                         last_recorded = 'quenched';
224 
225                     end
226 
227                 % Negative dV/dt - Positive dI/dt...
228                 case event_negdvdtposdidt
229 
230                     % Contact reconnected...
231                     state = state_start;
232 
233                     % Store duration counter and reset counter...
234                     if (counter_duration > 0)
235                         durationdata(durationarraycount) = (
                                counter_duration / Fdec) * 1000; % Scale
                                histogram into milliseconds...
236                         durationtime(i) = 1;
237                         durationarraycount = durationarraycount + 1;
238                     end
239                     counter_duration = 0;
240 
241                     % Create arc reconnected monitor pulse...
242                     arc_reconnected_monitor(i) = 1;
243                     last_recorded = 'reconnected';
244 
245                 % No event...
246                 case event_noevent
247 
248                     % Ensure that the first arc has occurred...
249                     if (periodcount_started == 1)
250 
251                         % Increment counters...
252                         counter_period = counter_period + 1;
253                         counter_duration = counter_duration + 1;
254 
255                     end
256 
257             end
258 
259     end
260 
261 end
262 
263 % If tuning parameter has been set, then plot tuning aids...
264 if (TUNE > 0)
```

```
265 %%
266     figure('name',['Recording' num2str(recnum) '.mat'],'color','white');
267     h(1) = subplot(4,1,1);plot(Recorder1.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder1.Channels.Segments.Data.Samples(1,:))),
            Recorder1.Channels.Segments.Data.Samples(1,:),'color','red');
268     xlabel('Time (ms)');
269     ylabel({'Varc -';'Voltage Across the Arc (V)'});
270     grid minor;
271     axis([0 max(Recorder1.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder1.Channels.Segments.Data.Samples(1,:)))) min(Recorder1.
            Channels.Segments.Data.Samples(1,:)) max(Recorder1.Channels.
            Segments.Data.Samples(1,:))]);
272
273     h(2) = subplot(4,1,2);%plot(Recorder2.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder2.Channels.Segments.Data.Samples(1,:))),
            Recorder2.Channels.Segments.Data.Samples(1,:),'color','blue');
274     plot(decimate(Recorder1.Channels.Segments.Data.dXstep*1000*(1:length
            (Recorder1.Channels.Segments.Data.Samples(1,:))),double(n),'FIR')
            ,yd); % Plot
275     xlabel('Time (ms)');
276     ylabel({'dVarc/dt -';' Downsampled and differentiated (V/s)'});
277     grid minor;
278     axis([0 max(Recorder2.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder2.Channels.Segments.Data.Samples(1,:)))) 1.2*min(yd(100:
            length(yd))) 1.2*max(yd(100:length(yd)))]);
279
280     h(3) = subplot(4,1,3);%plot(Recorder3.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder3.Channels.Segments.Data.Samples(1,:))),
            Recorder3.Channels.Segments.Data.Samples(1,:),'color','green');
281     plot(decimate(Recorder4.Channels.Segments.Data.dXstep*1000*(1:length
            (Recorder4.Channels.Segments.Data.Samples(1,:))),double(n),'FIR')
            ,zd);
282     xlabel('Time (ms)');
283     ylabel({'dIloop/dt -';'Downsampled and differentiated (A/s)'});
284     grid minor;
285     axis([0 max(Recorder4.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder4.Channels.Segments.Data.Samples(1,:)))) 1.2*min(zd(100:
            length(zd))) 1.2*max(zd(100:length(zd)))]);
286
287     h(4) = subplot(4,1,4);plot(Recorder4.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder4.Channels.Segments.Data.Samples(1,:))),
            Recorder4.Channels.Segments.Data.Samples(1,:),'color','red');
288     xlabel('Time (ms)');
289     ylabel({'Iloop -';'Current Through the Arc (A)'});
290     grid minor;
291     axis([0 max(Recorder4.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder4.Channels.Segments.Data.Samples(1,:)))) min(Recorder4.
            Channels.Segments.Data.Samples(1,:)) max(Recorder4.Channels.
            Segments.Data.Samples(1,:))]);
292     linkaxes(h,'x');
```

```
293 %%
294     figure('name',['Recording' num2str(recnum) '.mat'],'color','white','
            Position',[0,0,1280,776]);
295     h(1) = subplot(4,1,1);plot(Recorder1.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder1.Channels.Segments.Data.Samples(1,:))),
            Recorder1.Channels.Segments.Data.Samples(1,:),'color','red');
296     xlabel('Time (ms)');
297     ylabel({'Varc -';'Voltage Across the Arc (V)'});
298     grid minor;
299     axis([0 max(Recorder1.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder1.Channels.Segments.Data.Samples(1,:)))) min(Recorder1.
            Channels.Segments.Data.Samples(1,:)) max(Recorder1.Channels.
            Segments.Data.Samples(1,:))]);
300     h(2) = subplot(4,1,2);%plot(Recorder2.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder2.Channels.Segments.Data.Samples(1,:))),
            Recorder2.Channels.Segments.Data.Samples(1,:),'color','blue');
301     stem(decimate(Recorder1.Channels.Segments.Data.dXstep*1000*(1:length
            (Recorder1.Channels.Segments.Data.Samples(1,:))),double(n),'FIR')
            ,arc_struck_monitor); % Plot
302     xlabel('Time (ms)');
303     ylabel({'Arc Struck';'Monitor'});
304     grid minor;
305     %axis([0 max(Recorder2.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder2.Channels.Segments.Data.Samples(1,:)))) min(Recorder2.
            Channels.Segments.Data.Samples(1,:)) max(Recorder2.Channels.
            Segments.Data.Samples(1,:))]);
306     h(3) = subplot(4,1,3);%plot(Recorder3.Channels.Segments.Data.dXstep
            *1000*(1:length(Recorder3.Channels.Segments.Data.Samples(1,:))),
            Recorder3.Channels.Segments.Data.Samples(1,:),'color','green');
307     stem(decimate(Recorder4.Channels.Segments.Data.dXstep*1000*(1:length
            (Recorder4.Channels.Segments.Data.Samples(1,:))),double(n),'FIR')
            ,arc_quenched_monitor);
308     xlabel('Time (ms)');
309     ylabel({'Arc Quenched';'Monitor'});
310     grid minor;
311     %axis([0 max(Recorder3.Channels.Segments.Data.dXstep*1000*(1:length(
            Recorder3.Channels.Segments.Data.Samples(1,:)))) min(Recorder3.
            Channels.Segments.Data.Samples(1,:)) max(Recorder3.Channels.
            Segments.Data.Samples(1,:))]);
312     h(4) = subplot(4,1,4);
313     stem(decimate(Recorder4.Channels.Segments.Data.dXstep*1000*(1:length
            (Recorder4.Channels.Segments.Data.Samples(1,:))),double(n),'FIR')
            ,arc_reconnected_monitor);
314     xlabel('Time (ms)');
315     ylabel({'Arc Reconnected';'Monitor'});
316     grid minor;
317     linkaxes(h,'x');
318
319 end
320
```

```
321 %%
322 % Generate arc quench, strike and reconnection statistics...
323 total_arcs_quenched = 0;
324 total_arcs_struck = 0;
325 total_arcs_reconnected = 0;
326 for a=1:1:length(arc_quenched_monitor)
327     total_arcs_quenched = total_arcs_quenched + arc_quenched_monitor(a);
328     total_arcs_struck = total_arcs_struck + arc_struck_monitor(a);
329     total_arcs_reconnected = total_arcs_reconnected +
          arc_reconnected_monitor(a);
330 end
331 total_arcs_struck
332 total_arcs_quenched
333 total_arcs_reconnected
334 discrepancy = total_arcs_struck - total_arcs_reconnected -
      total_arcs_quenched
335
336 if length(durationdata) > length(perioddata)
337     durationdata = durationdata(1:length(durationdata)-1);
338 end
339
340 % Calculate min, mean and max values of arc period and duration data...
341 maxperiod = max(perioddata)
342 minperiod = min(perioddata)
343 avgperiod = mean(perioddata)
344 maxduration = max(durationdata)
345 minduration = min(durationdata)
346 avgduration = mean(durationdata)
347
348 % Write arc quantity statistics to log file...
349 fprintf(fid_log, '%d & %d & %d & ', total_arcs_struck,
      total_arcs_quenched, total_arcs_struck-total_arcs_quenched);
350
351 % Write arc quantity statistics to log file...
352 fprintf(fid_log, '%.4f & %.4f & %.4f & %.4f & %.4f & %.4f & ', minperiod
      , avgperiod, maxperiod, minduration, avgduration, maxduration);
353
354 %%
355 % Plot frequency / duration histogram...
356 durationdata(durationdata >= DUR_HIST_WINDOW) = [];
357 perioddata(perioddata >= PER_HIST_WINDOW) = [];
358 h = figure('name',['Recording' num2str(recnum) '.mat'],'color','white','
      Position',[0,0,1280,776]);
359 subplot(2,1,1);
360 hist(perioddata,((PER_HIST_WINDOW/BUCKETS)/2):(PER_HIST_WINDOW/BUCKETS)
      :(PER_HIST_WINDOW-(PER_HIST_WINDOW/BUCKETS)),'color','red');
361 title(['Histogram (' num2str(BUCKETS) ' Bucket) Showing the Period
      Between Arcs - ' num2str(total_arcs_struck) ' total arcs']);
362 xlabel('Time (ms)');
363 ylabel('Period Between Arc Events');
```

```
364 grid minor;
365 subplot(2,1,2);
366 hist(durationdata,((DUR_HIST_WINDOW/BUCKETS)/2):(DUR_HIST_WINDOW/BUCKETS
    ):(DUR_HIST_WINDOW-1),'color','red');
367 title(['Histogram (' num2str(BUCKETS) ' Bucket) Showing the Duration of
    Arcs - ' num2str(total_arcs_struck) ' total arcs']);
368 xlabel('Time (ms)');
369 ylabel('Duration of Arc Events');
370 grid minor;
371 saveas(h,'I:\Arc Fault Data\Diagram_Test1_PerDurHist.pdf','pdf');
372
373 %%
374 % Determine peak arc voltages at strike...
375 m = 1;
376 for a=1:1:length(arc_struck_monitor)
377     if (arc_struck_monitor(a) == 1)
378         %time = double(a*n)*Ts;
379          peakarcstrikevolts(m) = 0;
380         %double((a-2.2)*n)*Ts
381              for b=((a-2.5)*n):1:((a)*n)
382                  if (Recorder1.Channels.Segments.Data.Samples(1,b) >
                        peakarcstrikevolts(m)) && (Recorder1.Channels.
                        Segments.Data.Samples(1,b) < 100) % Reject visually
                        invalid data
383                      peakarcstrikevolts(m) = Recorder1.Channels.Segments.
                            Data.Samples(1,b);
384                  end
385              end
386 %              if m == 68
387 %                  time
388 %              end
389          m = m + 1;
390     end
391 end
392
393 % If any arcs did strike...
394 if(m > 1)
395     % Calculate statistics...
396     maxstrikevolts = max(peakarcstrikevolts)
397     minstrikevolts = min(peakarcstrikevolts)
398     avgstrikevolts = mean(peakarcstrikevolts)
399
400     % Write arc quenched voltage statistics to log file...
401     fprintf(fid_log, '%.1f & %.1f & %.1f & ', minstrikevolts,
            avgstrikevolts, maxstrikevolts);
402 else
403     % Write N/A to log file...
404     fprintf(fid_log, 'N/A & N/A & N/A & ');
405 end
406
```

```
407 %%
408 % Determine peak arc voltages at quench... Will just be highest voltage
409 % over considerable range.
410 m = 1;
411 for a=1:1:length(arc_quenched_monitor)
412     if (arc_quenched_monitor(a) == 1)
413         %time = double(a*n)*Ts;
414         peakarcquenchedvolts(m) = 0;
415             for b=((a-5)*n):1:((a)*n)
416                 if Recorder1.Channels.Segments.Data.Samples(1,b) >
                        peakarcquenchedvolts(m)
417                     peakarcquenchedvolts(m) = Recorder1.Channels.
                            Segments.Data.Samples(1,b);
418                 end
419             end
420         m = m + 1;
421     end
422 end
423
424 % If any arcs did quench...
425 if(m > 1)
426     % Calculate statistics...
427     maxquenchedvolts = max(peakarcquenchedvolts)
428     minquenchedvolts = min(peakarcquenchedvolts)
429     avgquenchedvolts = mean(peakarcquenchedvolts)
430
431     % Write arc quenched voltage statistics to log file...
432     fprintf(fid_log, '%.1f & %.1f & %.1f & ', minquenchedvolts,
            avgquenchedvolts, maxquenchedvolts);
433
434 else
435     % Write N/A to log file...
436     fprintf(fid_log, 'N/A & N/A & N/A & ');
437 end
438
439 %%
440 % Determine peak arc voltages at reconnection...
441 m = 1;
442 for a=1:1:length(arc_reconnected_monitor)
443     if (arc_reconnected_monitor(a) == 1)
444         %time = double(a*n)*Ts
445         peakarcreconnectedvolts(m) = 0;
446             for b=((a-3)*n):1:((a-2)*n)
447                 if Recorder1.Channels.Segments.Data.Samples(1,b) >
                        peakarcreconnectedvolts(m)
448                     peakarcreconnectedvolts(m) = Recorder1.Channels.
                            Segments.Data.Samples(1,b);
449                 end
450             end
451         m = m + 1;
```

```
452     end
453 end
454
455 % If any arcs did reconnect...
456 if(m > 1)
457     % Calculate statistics...
458     maxreconnectedvolts = max(peakarcreconnectedvolts)
459     minreconnectedvolts = min(peakarcreconnectedvolts)
460     avgreconnectedvolts = mean(peakarcreconnectedvolts)
461
462     % Write arc quenched voltage statistics to log file...
463     fprintf(fid_log, '%.1f & %.1f & %.1f\\\\', minreconnectedvolts,
            avgreconnectedvolts, maxreconnectedvolts);
464 else
465     % Write N/A to log file...
466     fprintf(fid_log, 'N/A & N/A & N/A & ');
467 end
468
469 %%
470 % Plot histograms for arc strike, quench and reconnect voltages...
471 h2 = figure('color','white','Position',[0,0,1280,500]);
472 subplot(1,3,1);
473 hist(peakarcstrikevolts,15);
474 xlabel('Arc Voltage (V)');
475 ylabel('Number of Arc Strike Events');
476 title({'Frequency Distribution of', 'Arc Voltage During Arc Strike'});
477 grid on;
478
479 subplot(1,3,2);
480 hist(peakarcreconnectedvolts,15);
481 xlabel('Arc Voltage (V)');
482 ylabel('Number of Arc Reconnection Events');
483 title({'Frequency Distribution of', 'Arc Voltage During Arc Reconnection
        '});
484 grid on;
485
486 subplot(1,3,3);
487 hist(peakarcquenchedvolts,15);
488 xlabel('Arc Voltage (V)');
489 ylabel('Number of Arc Quench Events');
490 title({'Frequency Distribution of','Arc Voltage During Arc Quench'});
491 grid on;
492
493 % Print arc strike, quench and reconnect voltage histograms to PDF...
494 paperpos = get(h2,'PaperPosition');
495 paperpos(1,4) = paperpos(1,4) / 2.5;
496 set(h2,'PaperPosition', paperpos);
497 saveas(h2,'I:\Arc Fault Data\Diagram_Test1_StrQueRecVoltHist.pdf','pdf')
        ;
498
```

```
499 %%
500 % Plot statistics tuning aids...
501 if TUNESTAT==1
502     figure('name',['Recording' num2str(recnum) '.mat'],'color','white','
        Position',[0,0,1280,776]);
503     scatter(perioddata,durationdata);
504     %axis([0 15 0 15]);
505     title('Scatter Plot Showing Distribution of Arc Duration vs Arc
        Period');
506     xlabel('Arc Period (s)')
507     ylabel('Arc Duration (s)');
508     grid on;
509
510     figure('name',['Recording' num2str(recnum) '.mat'],'color','white','
        Position',[0,0,1280,776]);
511     scatter(perioddata-durationdata,durationdata);
512     %axis([0 15 0 15]);
513     title('Scatter Plot Showing Distribution of Arc Duration vs Arc
        Period');
514     xlabel('Arc Wait (s)')
515     ylabel('Arc Duration (s)');
516     grid on;
517 end
518
519 % Close log file...
520 fclose(fid_log);
```

Appendix B

Chapter 3 Support Material

B.1 Aircraft Wire Resistance Derivation

The wire resistance R can be calculated with Equation (B.1).

$$R = \frac{\rho\ell}{A} \quad (\Omega) \tag{B.1}$$

Equation (B.1) gives the total resistance for a wire length ℓ, whereas the per-unit-length resistance is given by Equation (B.2).

$$R = \frac{\rho}{A} \quad (\Omega/m) \tag{B.2}$$

Copper and aluminium are the two most common conductor materials used on modern aircraft, where resistivity ρ of these materials at 20°C is given by Cardarelli [264] thus.

$$\rho_{copper} = 1.7248 \times 10^{-8}\Omega.m$$
$$\rho_{aluminium} = 2.6548 \times 10^{-8}\Omega.m$$

Copper wire is currently the most common conductor material used in the aircraft EWIS, although aluminium has been used on some platforms for its improved conductivity-to-weight ratio in high current conductor applications such as those found in primary electrical distribution systems.

The total wire resistance is subsequently calculated by determining the cross-sectional area of the wire, which is dependent upon the wire gauge, and the total wire length, which is specific to the application of the wire feeder on a given aircraft platform.

Typically the American Wire Gauge system is used to define the gauge of wire required for a given load current. The American Wire Gauge system defined in standard ASTM B 258-02 [265] states that the wire diameter d_n for a wire whose gauge is n AWG is given by Equation (B.3). The cross-sectional area A_n of the n AWG wire can then be computed using Equation (B.4).

$$d_n = \left(1.27 \times 10^{-4}\right) \times 92^{\frac{36-n}{39}} \quad (m) \tag{B.3}$$

$$\begin{aligned} A_n &= \frac{\pi}{4} d_n^2 = \frac{\pi}{4} \left(\left(1.27 \times 10^{-4}\right) \times 92^{\frac{36-n}{39}} \right) \\ &= \left(1.2668 \times 10^{-8}\right) \times 92^{\frac{36-n}{19.5}} \quad \left(m^2\right) \end{aligned} \tag{B.4}$$

B.2 Aircraft Wire Inductance Derivation

To understand how magnetic fields interact in cylindrical wires Figure B.1 must first be considered. The figure shows a surface s adjacent to a cylindrical conductor which carries current I. The aim here is to calculate the total flux at the surface s.

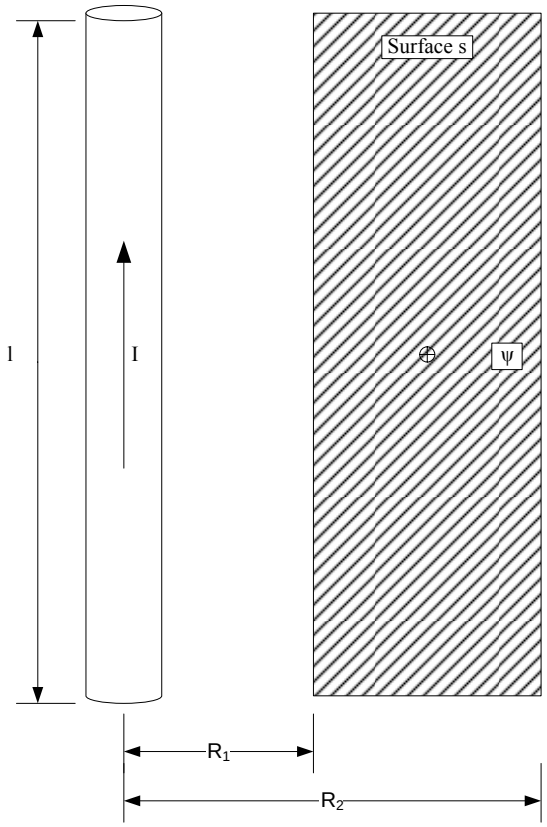


Figure B.1: Visual Representation of Total Flux ψ in Surface s, Created by Current I in a Single Cylindrical Conductor

Beginning with Ampere's Law in Equation (B.5) the transverse magnetic field intensity $\mathscr{H}_t$ around a cylindrical conductor of radius r which is conducting a current I can be derived.

$$I = \oint_c \overrightarrow{\mathscr{H}_t} d\overrightarrow{l} \tag{B.5}$$

$$\therefore \mathscr{H}_t = \frac{I}{2\pi r} \tag{B.6}$$

The magnetic flux density $\mathscr{B}_t$ can then be calculated in Equations (B.7) and (B.8) from the transverse magnetic field intensity $\mathscr{H}_t$ given in Equation (B.6).

$$\mathscr{B}_t = \mu \mathscr{H}_t \tag{B.7}$$

$$\therefore \mathscr{B}_t = \frac{\mu I}{2\pi r} \tag{B.8}$$

The total flux ψ can now be calculated by integrating the magnetic flux density $\mathscr{B}_t$ over the surface s.

$$\psi = \iint_s \overrightarrow{\mathscr{B}_t} d\overrightarrow{s} \tag{B.9}$$

$$= \Delta z \int_{R_1}^{R_2} \frac{\mu I}{2\pi r} dr \tag{B.10}$$

$$\therefore \psi = \Delta z \frac{\mu I}{2\pi r} \ln\left(\frac{R_2}{R_1}\right) \tag{B.11}$$

With an expression for total flux ψ within surface s given in Equation (B.11), the inductance per-unit-length for a wire-above-ground plane scenario can be calculated.

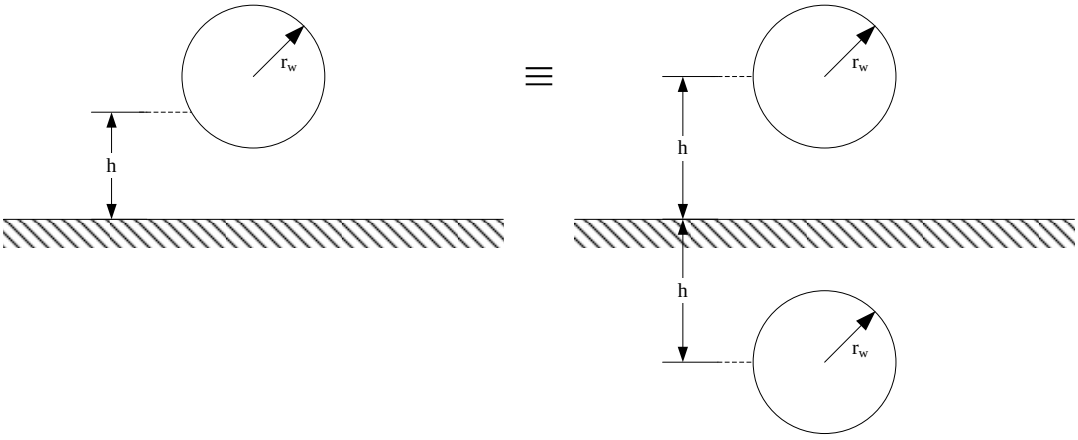


Figure B.2: Visual Representation of the Wire-Over-Ground Plane Transmission Line Scenario [7]

Paul describes the "method of images" which can be used to calculate the inductance per-unit-length of a wire-over-ground plane transmission line scenario and this approach is visualised in Figure B.2 [7]. The "method of images" assumes that there is

an image of the wire pictured on the left hand side of Figure B.2 within the ground plane region depicted on the right hand side of Figure B.2.

In contrast to the single wire configuration described in Figure B.1, the surface s now becomes the surface between the centres of the two wires illustrated in Figure B.2. The total flux ψ at the surface s can now be calculated from Equation (B.12).

$$\begin{aligned}\psi &= \frac{\mu I}{2\pi}\ln\left(\frac{2h-r_w}{r_w}\right)+\frac{\mu I}{2\pi}\left(\frac{2h-r_w}{r_w}\right) \\ &= \frac{\mu I}{2\pi}\ln\left(\frac{(2h-r_w)\,(2h-r_w)}{r_w^2}\right)\end{aligned} \tag{B.12}$$

Assuming that the separation between the main wire and the wire image is large with respect to the radius of the wire ($2h >> r_w$), Equations (B.13) and (B.14) can be obtained.

$$\begin{aligned}\psi &\backsimeq \frac{\mu I}{2\pi}\ln\left(\frac{(2h)^2}{r_w^2}\right) \\ &\backsimeq \frac{\mu I}{2\pi}\ln\left(\frac{2h}{r_w}\right)^2\end{aligned} \tag{B.13}$$

$$\therefore \psi \backsimeq \frac{\mu I}{\pi}\ln\left(\frac{2h}{r_w}\right) \quad (Wb/m) \tag{B.14}$$

From the total flux ψ, the inductance L of the transmission line can be calculated in Equations (B.15) and (B.16).

$$L \backsimeq \frac{\psi}{I} \tag{B.15}$$

$$\therefore L \backsimeq \frac{\mu}{\pi}\ln\left(\frac{2h}{r_w}\right) \quad (H/m) \tag{B.16}$$

B.3 Sample Digital Signal Source SPICE Model for "Loose Terminal" Modelling in SPICE Arc Model Subcircuit Code

Listing B.1: DigitalSignalSourceFile_Example.dig

```
1 * Autogenerated loose contact enable model based on arc
2 * duration / period Probability Distribution Functions...
3 * Generated on 09-03-2014 at 16:38:55...
4 * PDFs taken from file Recording353.mat
5 .subckt loose_contact_enable out
6 Aloose_contact [out] arc_model
7 .MODEL arc_model d_source input_file = Recording353.dig
8 .ends loose_contact_enable
```

B.4 Drawn Arc Generator Assembly Diagram

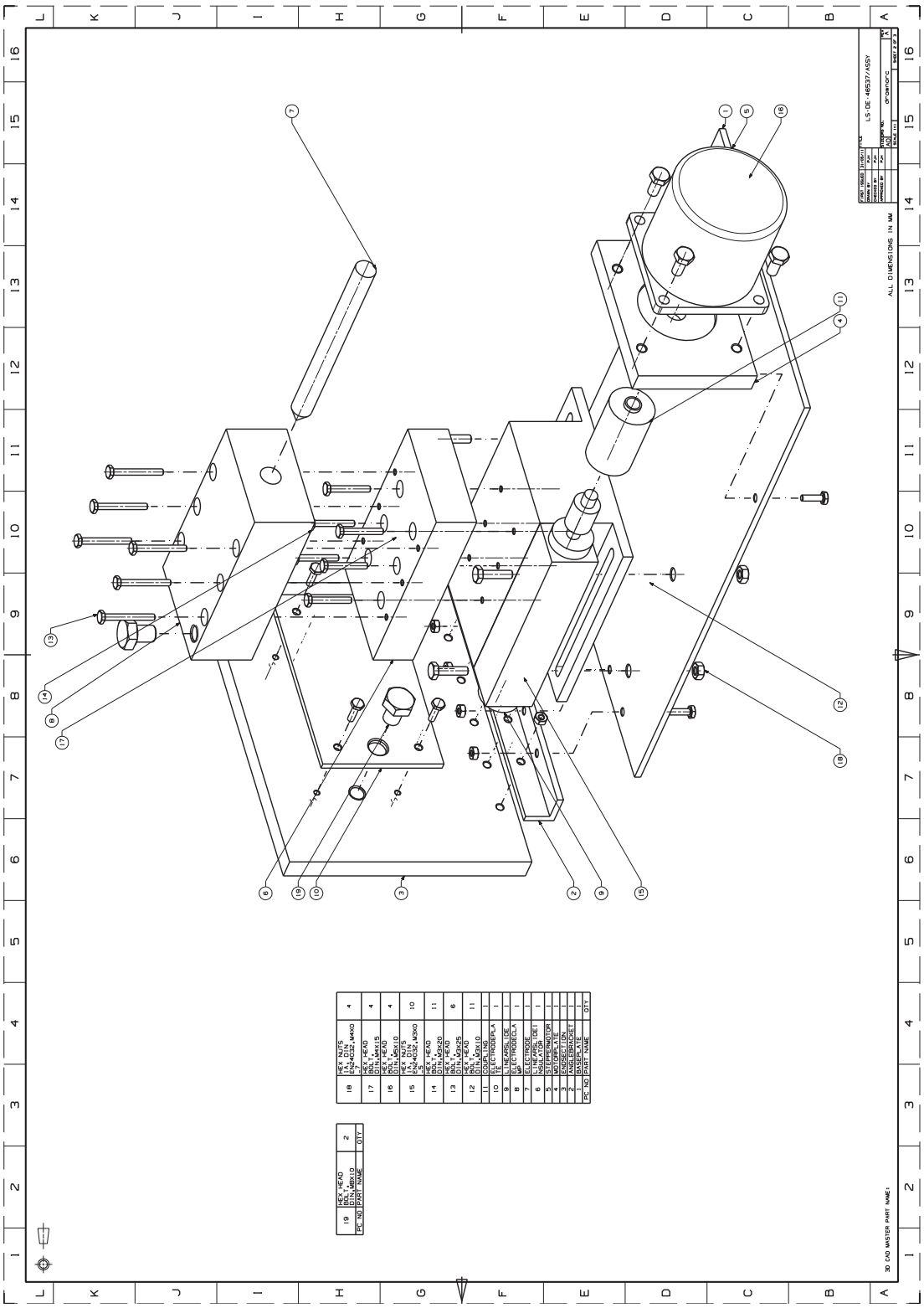


Figure B.3: Drawn Arc Generator Assembly Diagram (Isometric)

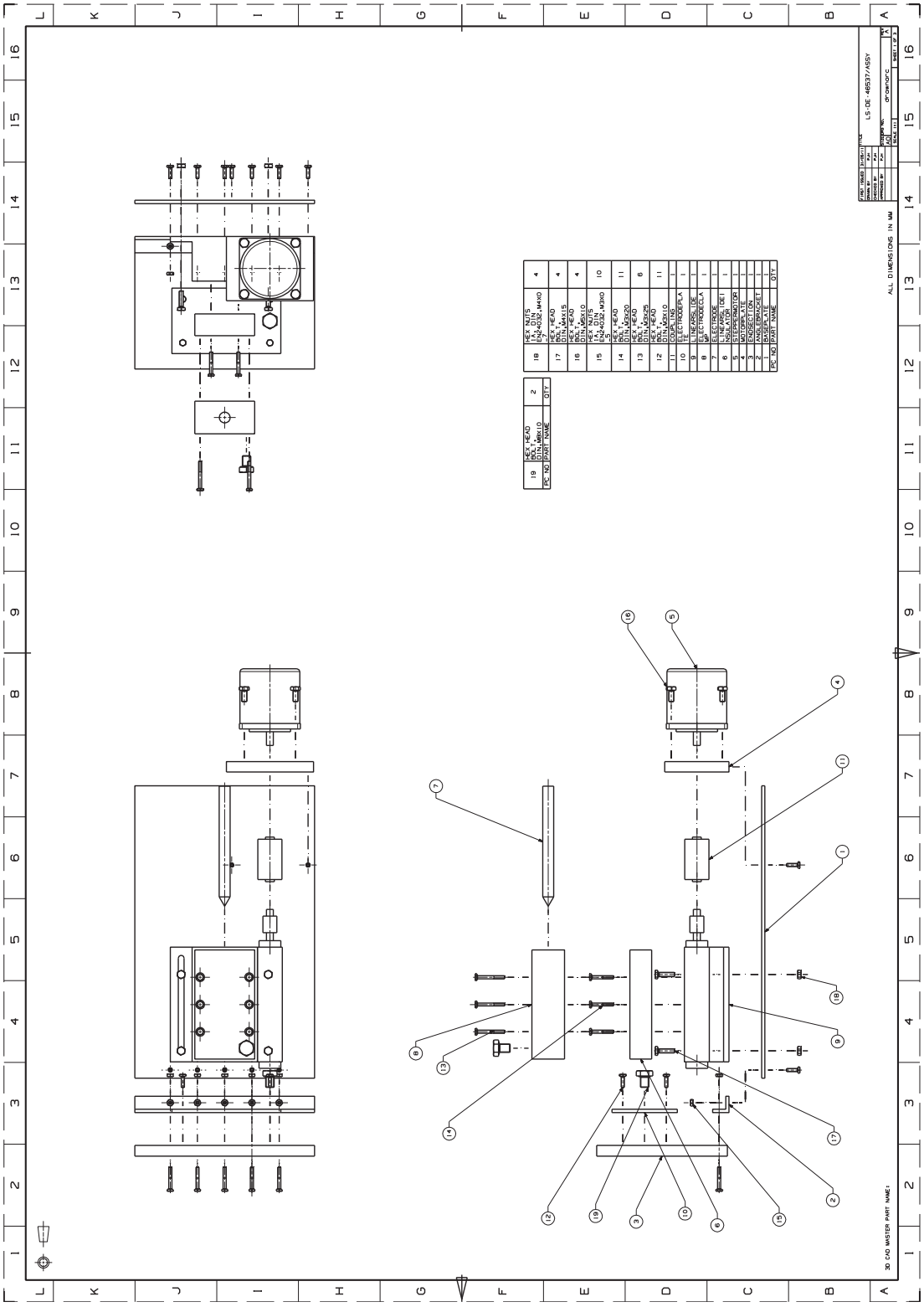


Figure B.4: Drawn Arc Generator Assembly Diagram (Third Angle Projection)

B.5 Non-Linear Continuous SPICE Arc Model Subcircuit Code Listing

Listing B.2: Arc_SPICE_Linear.cir

```
1  ******************************
2  * Model Name: ARC_SPICE_Linear *
3  * Author:     Peter Handy      *
4  * Revision:   1                *
5  * Date:       20/02/2014       *
6  ******************************
7
8  * Declare Arc_SPICE_Linear subcircuit.
9  * t1  : Arc Terminal 1
10 * t2  : Arc Terminal 2
11 * vc+ : Switch Control Voltage (5V with respect to vref enables the arc,
       0V with respect to vref disables the arc)
12 * vl+ : Voltage with respect to vref sets the arc length (1 Volt per
      metre)
13 * vref : Reference for vc+ and vl+
14 .SUBCKT Arc_SPICE_Linear t1 t2 vc+ vl+ vref
15
16 * Declare inverted and standard low on-impedance, high off-impedance
      switches...
17 .model switch sw(Ron=0.000000001, Roff=1000000000, Von=2.5001, Voff
      =2.4999)
18 .model invswitch sw(Ron=0.000000001, Roff=1000000000, Von=2.4999, Voff
      =2.5001)
19
20 * Set arc parameters as per the Ayrton model...
21 .param A 20
22 .param B 1
23 .param C 20
24 .param D 1
25 .param N 1.05
26
27 * Declare the arc voltage dependent voltage source...
28 Earc int2 t2 VALUE { ( I(Vsense) / ( ABS(I(Vsense)) + 1E-6 ) ) * ( {A} +
       ( {B} * V(vl+,vref) ) + ( ( {C} + ( {D} * V(vl+,vref) ) ) / ( ( ABS(
      I(Vsense))^{N} + 1E-3 ) ) ) ) }
29
30 * Declare a dummy 0V voltage source, used for current sensing...
31 Vsense int int2 DC 0
32
33 * Declare the switch pair, used to enable and disable the arc model...
34 Se t1 int vc+ vref switch
35 Sd t1 t2 vc+ vref invswitch
36 .ENDS
```

B.6 Sample Digital Signal Source Data File for "Loose Terminal" Modelling in SPICE Arc Model Subcircuit Code, First 35 Lines of Listing

Listing B.3: DigitalSignalSourceFile_Example.dig

```
1  * Shaped PDF autogenerated loose contact arc duration/frequency data...
2  * Generated on 25-02-2014 at 11:22:43...
3  0.00 0s
4  1.00m 1s
5  2.88m 0s
6  7.75m 1s
7  13.63m 0s
8  16.50m 1s
9  16.63m 0s
10 30.25m 1s
11 30.38m 0s
12 63.00m 1s
13 64.13m 0s
14 66.75m 1s
15 70.88m 0s
16 71.00m 1s
17 72.38m 0s
18 75.25m 1s
19 80.38m 0s
20 84.00m 1s
21 84.88m 0s
22 90.25m 1s
23 90.38m 0s
24 98.00m 1s
25 98.88m 0s
26 111.75m 1s
27 115.13m 0s
28 126.00m 1s
29 127.38m 0s
30 129.25m 1s
31 130.63m 0s
32 131.50m 1s
33 134.13m 0s
34 146.75m 1s
35 148.13m 0s
36 168.50m 1s
37 169.88m 0s
38 170.25m 1s
```

B.7 MATLAB Script to Auto-code SPICE Subcircuit Model and Auto-generated a SPICE "Digital Signal Source" From Arc Signal Recordings

Listing B.4: SPICEGenPeriodDuration.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Script Name :    SPICEGenPeriodDuration                                      %
%                                                                              %
% Filename :       SPICEGenPeriodDuration.m                                    %
%                                                                              %
% Purpose :        To generate a SPICE-compatible time domain arc              %
%                  strike/reconnect waveform with values taken                 %
%                  directly from a real-world waveform.                        %
%                                                                              %
% Author :         Peter Handy                                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Define when the arc fault waveform should start (in ms)...
time_arcstart = 0;

% Scrutinise the durationdata and perioddata signals for events where the
% duration data is equal to zero (an event where the feature detector
% detects a strike and a quench at a time comparable to the sampling period
% 1/Fd, and where the duration time is greater than the period time. If any
% discrepancies occur then remove them from the data set...
i = 1;
while (i < length(durationdata))
    if ((durationdata(i) >= perioddata(i)) | ~(durationdata(i) > 0))
        durationdata(i) = [];
        perioddata(i) = [];
        durationtime(i) = [];
        periodtime(i) = [];
    end
    i = i + 1;
end

% Generate the '.dig' file which contains the arc time domain waveform ...
filename = ['Recording' num2str(recnum) '.dig'];
fid = fopen(filename,'w+');

% Write description into the start of the file...
fprintf(fid,['* Recorded loose contact arc duration/frequency data from Recording' num2str(recnum) '.dig...\n']);
```

```
38 fprintf(fid,['* Generated on ' datestr(now,'DD-mm-YYYY') ' at ' datestr(
       now,'HH:MM:ss') '...\n']);
39
40 % If the desired arc start time is greater than zero then set state '0'
41 % until the arc begins...
42 if (time_arcstart > 0)
43     fprintf(fid,'0.00 0s\n'); % Set 0 at startup
44 end
45
46 % Start the first arc at time_arcstart...
47 fprintf(fid,'%0.5fm 1s\n',time_arcstart); % Start of first arc
48
49 % Read data out of the periodtime and durationtime vectors and write
       them into the '.dig' file, normalising to the decimated sampling
       period used for the feature extraction...
50 for i = 1:1:length(periodtime)
51    if (periodtime(i) > 0)
52        fprintf(fid,'%0.5fm 1s\n',time_arcstart+((i-1)*1000/double(Fdec))
              );
53    elseif (durationtime(i) > 0)
54        fprintf(fid,'%0.5fm 0s\n',time_arcstart+((i-1)*1000/double(Fdec))
              );
55    end
56 end
57
58 % Close the '.dig' file...
59 fclose(fid);
60
61 % Generate the model file which references the the '.dig' arc time
       domain waveform...
62 fid = fopen('loose_contact_enable.cir','w+');
63
64 % Write description into the start of the file...
65 fprintf(fid,'* Autogenerated loose contact enable model based on arc\n')
       ;
66 fprintf(fid,'* duration / period Probability Distribution Functions...\n
       ');
67 fprintf(fid,['* Generated on ' datestr(now,'DD-mm-YYYY') ' at ' datestr(
       now,'HH:MM:ss') '...\n']);
68 fprintf(fid,['* PDFs taken from file Recording' num2str(recnum) '.mat\n
       ']);
69 fprintf(fid,'.subckt loose_contact_enable out\n');
70 fprintf(fid,'Aloose_contact [out] arc_model\n');
71 fprintf(fid,['.MODEL arc_model d_source input_file = Recording' num2str(
       recnum) '.dig\n']);
72 fprintf(fid,'.ends loose_contact_enable\n');
73
74 % Close the '.dig' file...
75 fclose(fid);
```

B.8 MATLAB Script to Create Arc Enable Signal From Arc Signal Recordings

Listing B.5: ArcGenShapedPDF2D_Rev1.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Script Name :    ArcGenShapedRandom                                          %
%                                                                              %
% Filename :       ArcGenShapedRandom.m                                        %
%                                                                              %
% Purpose :        To generate a SPICE-compatible time domain arc              %
%                  strike/reconnect waveform with similar arc                  %
%                  duration and period Probability Distribution                %
%                  Functions.                                                  %
%                                                                              %
% Author :         Peter Handy                                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Declare input data...
recnum = 353;
plot = 1;
time_arcstart = 1;

% Declare how many arc durations and periods are required...
N_duration = 50000;
N_period = 50000;

% Declare how many arcs are required in the SPICE model...
N_required = 10000;

% Round N_duration, N_period and N_required to ensure that they are
    integer
% numbers...
N_duration = round(N_duration);
N_period = round(N_period);
N_required = round(N_required);

% Run PlotGenesisDIDTArc_StateMachine_Histo.m first...
% Then take perioddata and durationdata and generate period and duration
% histograms...
[P_period, Period_bin_centre] = hist(perioddata,((PER_HIST_WINDOW/100)/2)
    :(PER_HIST_WINDOW/100):(PER_HIST_WINDOW-(PER_HIST_WINDOW/100)),'color
    ','red');
[P_duration, Duration_bin_centre] = hist(durationdata,((DUR_HIST_WINDOW
    /100)/2):(DUR_HIST_WINDOW/100):(DUR_HIST_WINDOW-1),'color','red');

% Normalise probability density function...
Pnorm_duration = [0 P_duration] / sum(P_duration);
Pnorm_period   = [0 P_period]   / sum(P_period);

```

```
42 % Compute cumulative duration and period distribution...
43 Pcum_duration = cumsum(Pnorm_duration);
44 Pcum_period = cumsum(Pnorm_period);
45
46 % Create random (type double between 0 to 1) matrices for durations
47 % and periods...
48 R_duration = rand(1,N_duration);
49 R_period = rand(1,N_period);
50
51 % Calculate V matrices for durations and periods...
52 V_duration = 1:length(P_duration);
53 V_period = 1:length(P_period);
54
55 % Count the number of random points in R_duration that fall between the
56 % points given in Pcum_duration, and write bin numbers into which the
57 % random numbers fall into T_duration...
58 [~,T_duration] = histc(R_duration,Pcum_duration);
59 [~,T_period] = histc(R_period,Pcum_period);
60
61 % Convert T_duration and T_period row vectors into column vectors...
62 T_duration = T_duration';
63 T_period = T_period';
64
65 % Generate histogram data to verify that the algorithm has generated
       data
66 % correctly...
67 Dist_duration = hist(T_duration(T_duration > 0), 1:length(P_duration));
68 Dist_period = hist(T_period(T_period > 0), 1:length(P_period));
69
70 % Normalize Distibutions...
71 Distnorm_duration = [0 Dist_duration]/sum(Dist_duration);
72 Distnorm_period = [0 Dist_period]/sum(Dist_period);
73
74 % This loop ensures that the difference period - duration is greater
       than
75 % zero to ensure that the arc reconnects before the next arc strikes up
       to
76 % N_required...
77 diff_data = period_data - duration_data;
78 for i=1:1:N_required
79     while (diff_data(i) <= 0)
80         duration_data = [duration_data(1:i-1) circshift(duration_data(i:
               end),[0 -1]) ];
81         diff_data = period_data - duration_data;
82     end
83 end
84
85 % Generate the '.dig' file which contains the arc time domain waveform
       ...
86 filename = ['Recording' num2str(recnum) '.dig'];
```

```
87  fid = fopen(filename,'w+');
88
89  % Write description into the start of the file...
90  fprintf(fid,'* Shaped PDF autogenerated loose contact arc duration/
        frequency data...\n');
91  fprintf(fid,['* Generated on ' datestr(now,'DD-mm-YYYY') ' at ' datestr(
        now,'HH:MM:ss') '...\n']);
92  fprintf(fid,'0.00 0s\n'); % Set 0 at startup
93
94  % Start the first arc at time_arcstart...
95  fprintf(fid,'%0.2fm 1s\n',time_arcstart); % Start of first arc
96
97  % Read data out of the duration_data and period_data vectors and write
        them
98  % into the '.dig' file...
99  for i = 1:1:N_required
100     time_arcstart = time_arcstart + duration_data(i);
101     fprintf(fid,'%0.2fm 0s\n',time_arcstart);
102     % Not currently computing period, but time until next arc...
103     time_arcstart = time_arcstart + (period_data(i) - duration_data(i));
104     fprintf(fid,'%0.2fm 1s\n',time_arcstart);
105 end
106
107 % Close the '.dig' file...
108 fclose(fid);
109
110 % Generate the model file which references the the '.dig' arc time
        domain waveform...
111 fid = fopen('loose_contact_enable.cir','w+');
112
113 % Write description into the start of the file...
114 fprintf(fid,'* Autogenerated loose contact enable model based on arc\n')
        ;
115 fprintf(fid,'* duration / period Probability Distribution Functions...\n
        ');
116 fprintf(fid,['* Generated on ' datestr(now,'DD-mm-YYYY') ' at ' datestr(
        now,'HH:MM:ss') '...\n']);
117 fprintf(fid,['* PDFs taken from file Recording' num2str(recnum) '.mat\n'
        ]);
118
119 fprintf(fid,'.subckt loose_contact_enable out\n');
120 fprintf(fid,'A loose_contact [out] arc_model\n');
121 fprintf(fid,['.MODEL arc_model d_source input_file = Recording' num2str(
        recnum) '.dig\n']);
122 fprintf(fid,'.ends loose_contact_enable\n');
123 % Close the '.dig' file...
124 fclose(fid);
125
126
127 % If plotting is enabled then plot data...
```

```
128 if (plot == 1)
129
130     % Create a new figure...
131     figure('Color','white');
132
133     % Plot Normalised Probability Distribution Functions for
            Experimental and Synthesised Arc Period Data
134     subplot(2,1,1);
135     hold on;
136     grid on;
137     title('Normalised Probability Distribution Functions for
            Experimental and Synthesised Arc Period Data');
138     h = bar(Distnorm_period,'b');
139     %ch = get(h,'child');
140     %set(ch,'facea',0.5);
141     h = bar(Pnorm_period,'r');
142     %ch = get(h,'child');
143     %set(ch,'facea',0.5);
144     xlabel('Time (ms)');
145     ylabel('Normalised PDF for Arc Periods');
146     legend('Synthesised','Experimental');
147
148     % Plot Normalised Probability Distribution Functions for
            Experimental and Synthesised Arc Duration Data
149     subplot(2,1,2);
150     hold on;
151     grid on;
152     title('Normalised Probability Distribution Functions for
            Experimental and Synthesised Arc Duration Data');
153     h = bar(Distnorm_duration,'b');
154     %ch = get(h,'child');
155     %set(ch,'facea',0.5);
156     h = bar(Pnorm_duration,'r');
157     %ch = get(h,'child');
158     %set(ch,'facea',0.5);
159     xlabel('Time (ms)');
160     ylabel('Normalised PDF for Arc Durations');
161     legend('Synthesised','Experimental');
162
163 end
```

B.9 Series Arc Fault / SSPC Simulation Results

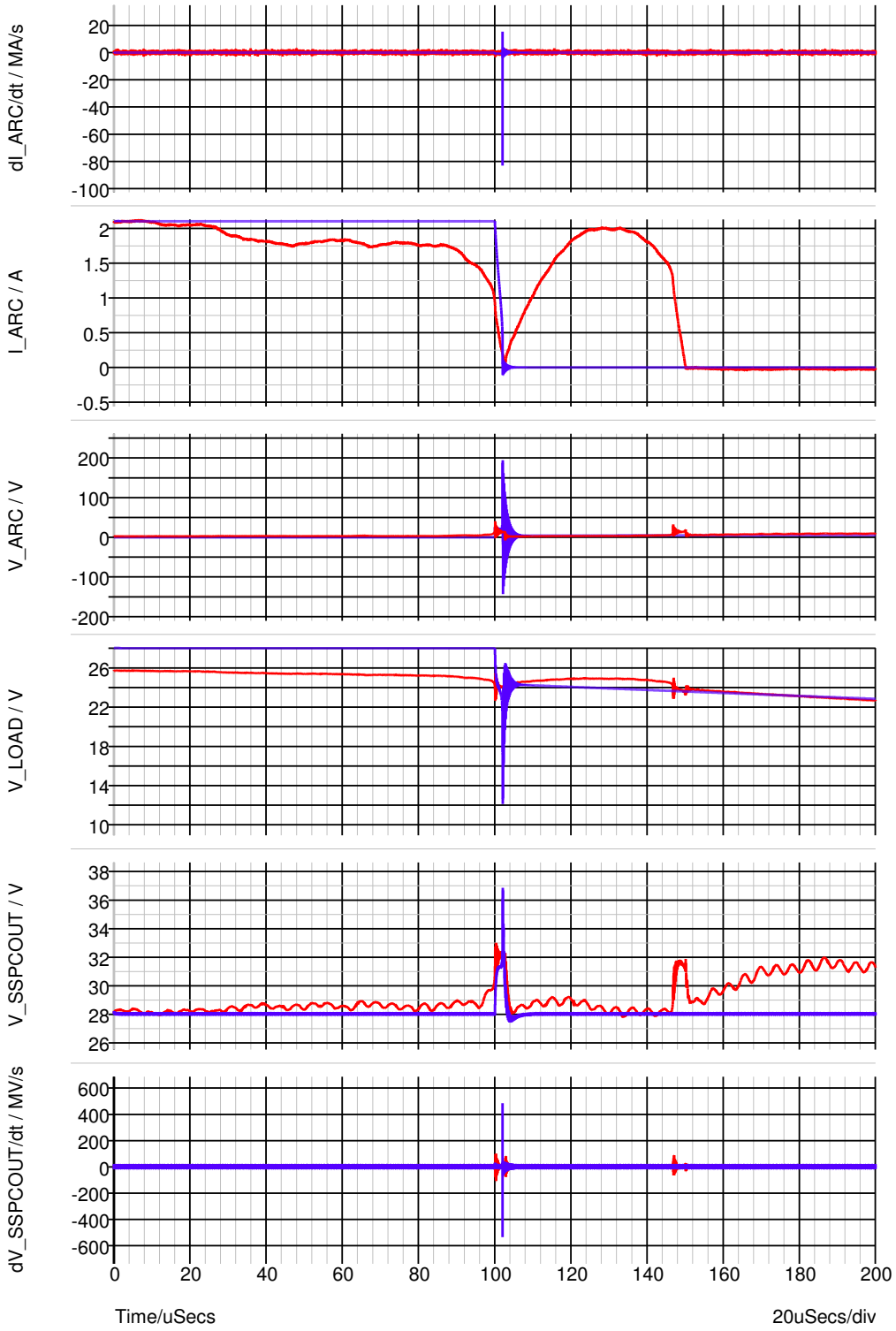


Figure B.5: Scenario 4 - Comparison of Simulation and Experimental Results for Series Arc Fault - 28VDC Line, 2.5A Resistive Load / 100μF Capacitive Load (Blue - Simulated, Red - Experimental)

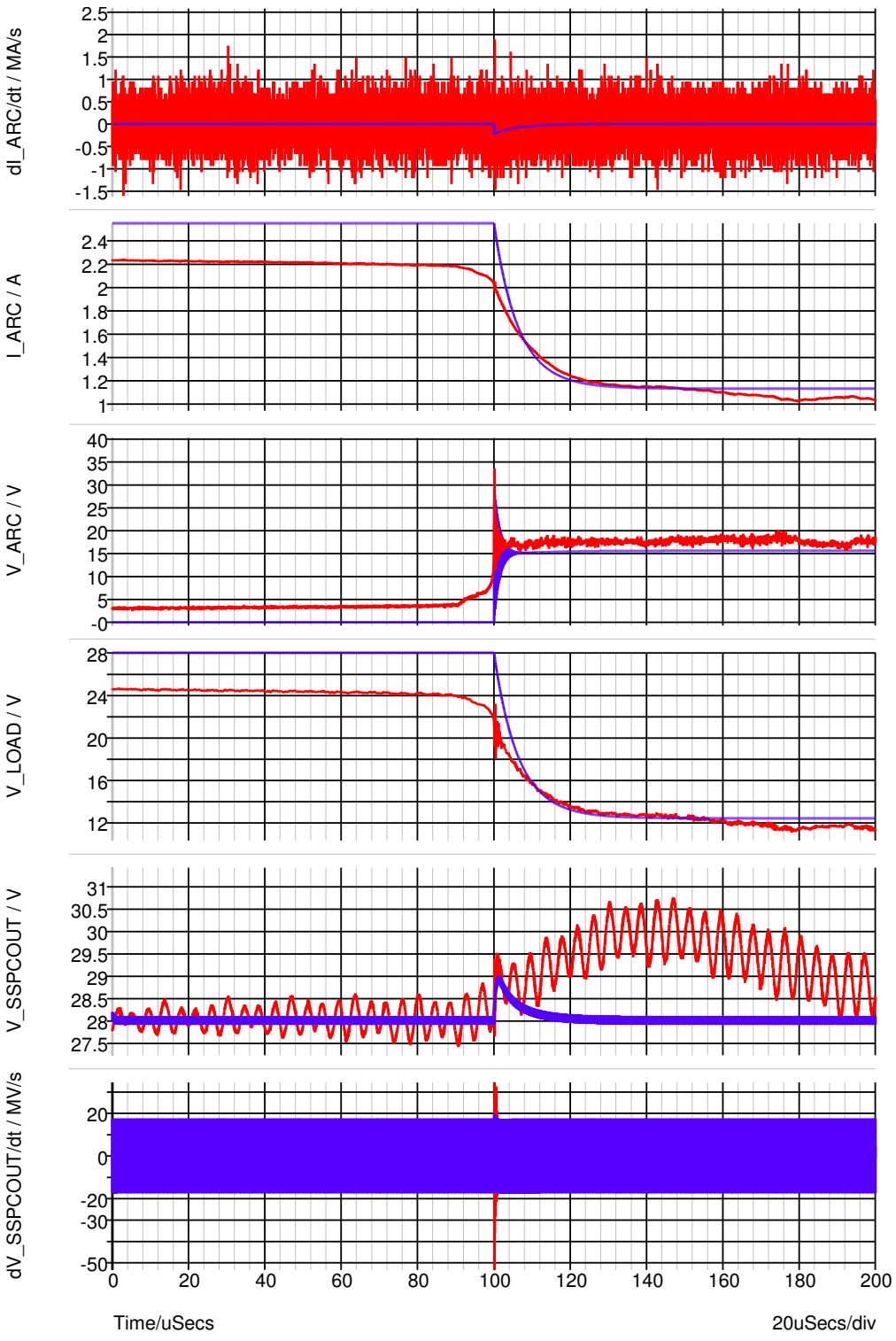


Figure B.6: Scenario 5 - Comparison of Simulation and Experimental Results for Series Arc Fault - 28VDC Line, 2.5A Resistive Load / +50μH Downstream Inductance (Blue - Simulated, Red - Experimental)

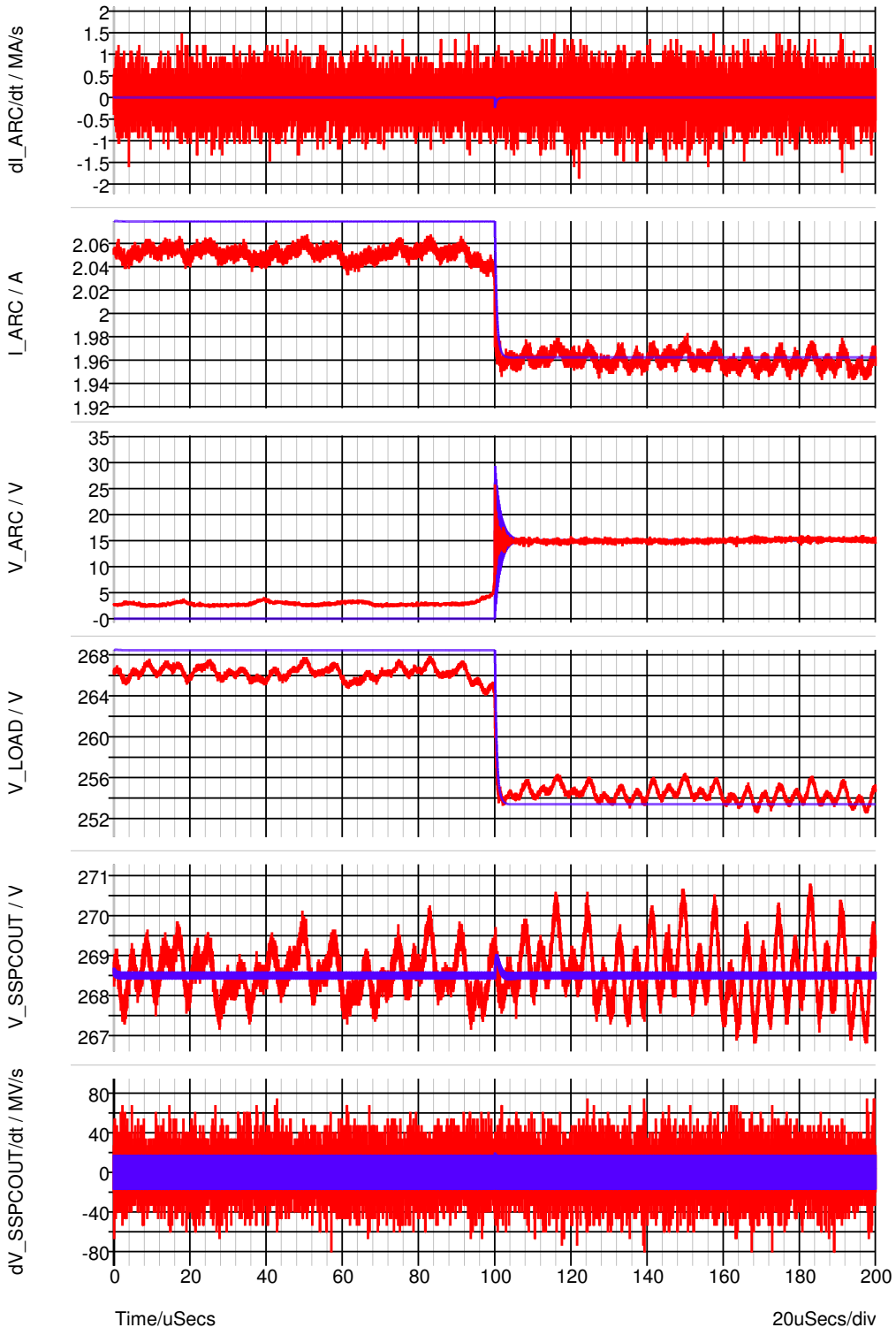


Figure B.7: Scenario 6 - Comparison of Simulation and Experimental Results for Series Arc Fault - 270VDC Line, 2.5A Resistive Load / +50μH Downstream Inductance (Blue - Simulated, Red - Experimental)

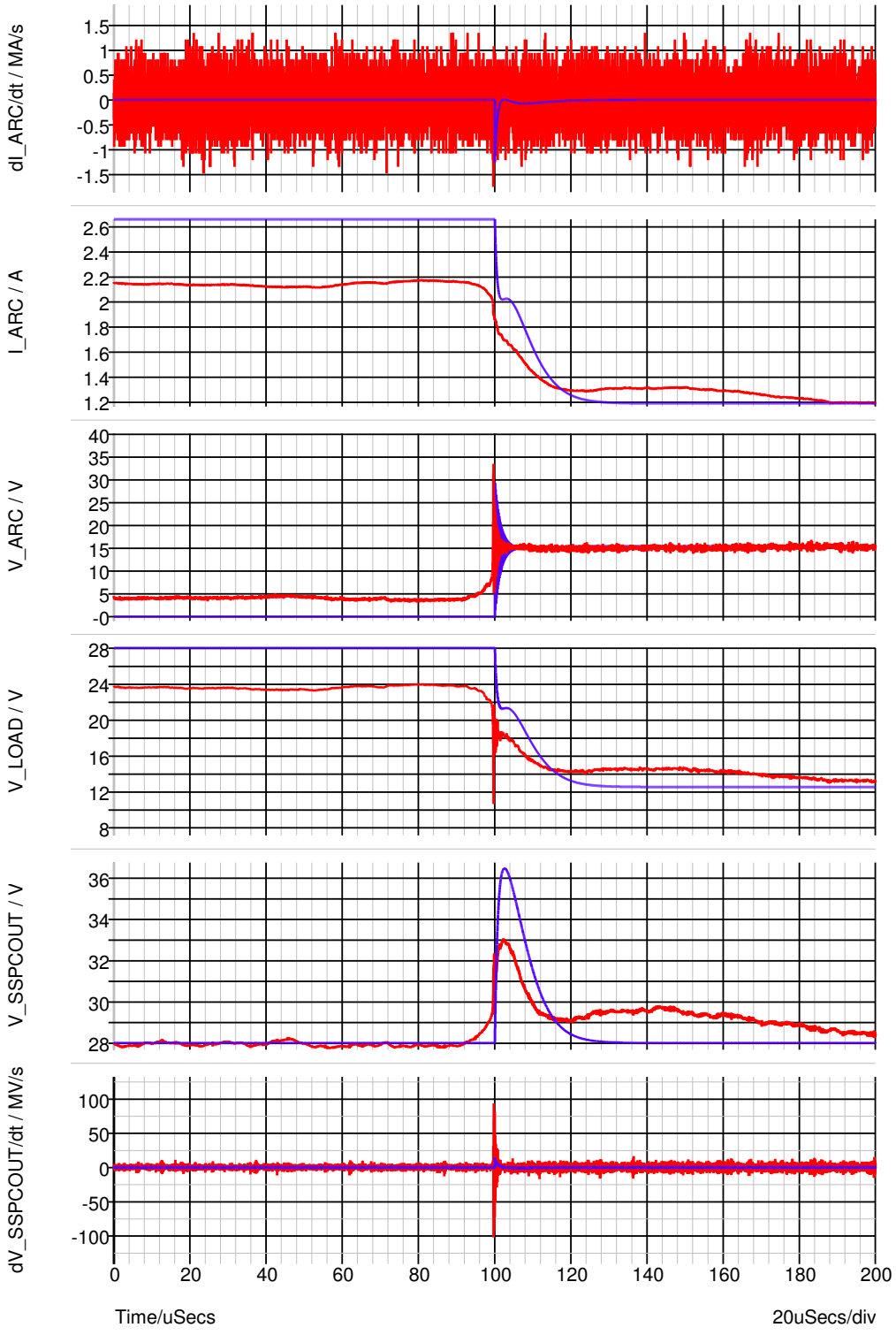


Figure B.8: Scenario 7 - Comparison of Simulation and Experimental Results for Series Arc Fault - 28VDC Line, 2.5A Resistive Load / +50μH Upstream Inductance (Blue - Simulated, Red - Experimental)

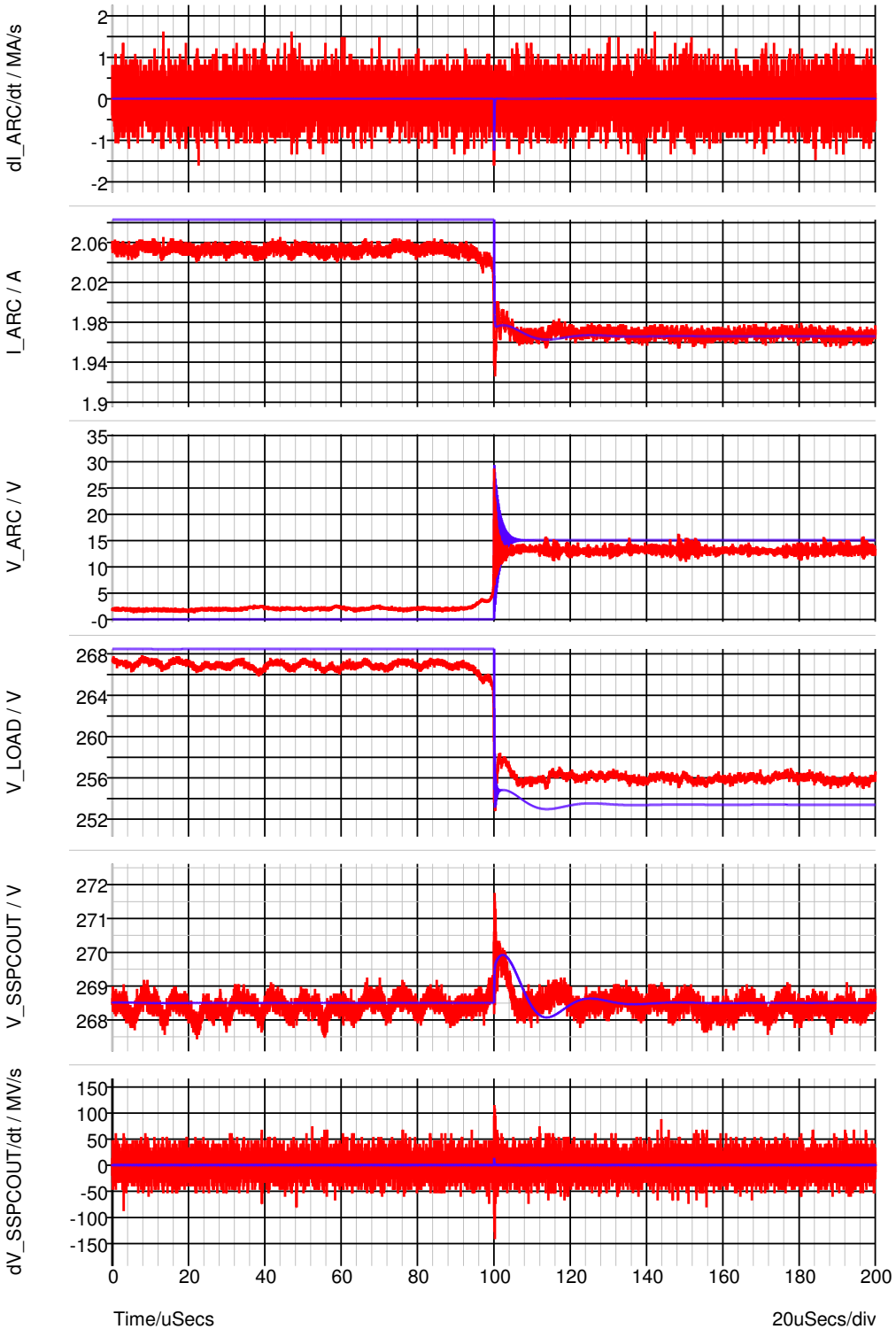


Figure B.9: Scenario 8 - Comparison of Simulation and Experimental Results for Series Arc Fault - 270VDC Line, 2.5A Resistive Load / +50μH Upstream Inductance (Blue - Simulated, Red - Experimental)

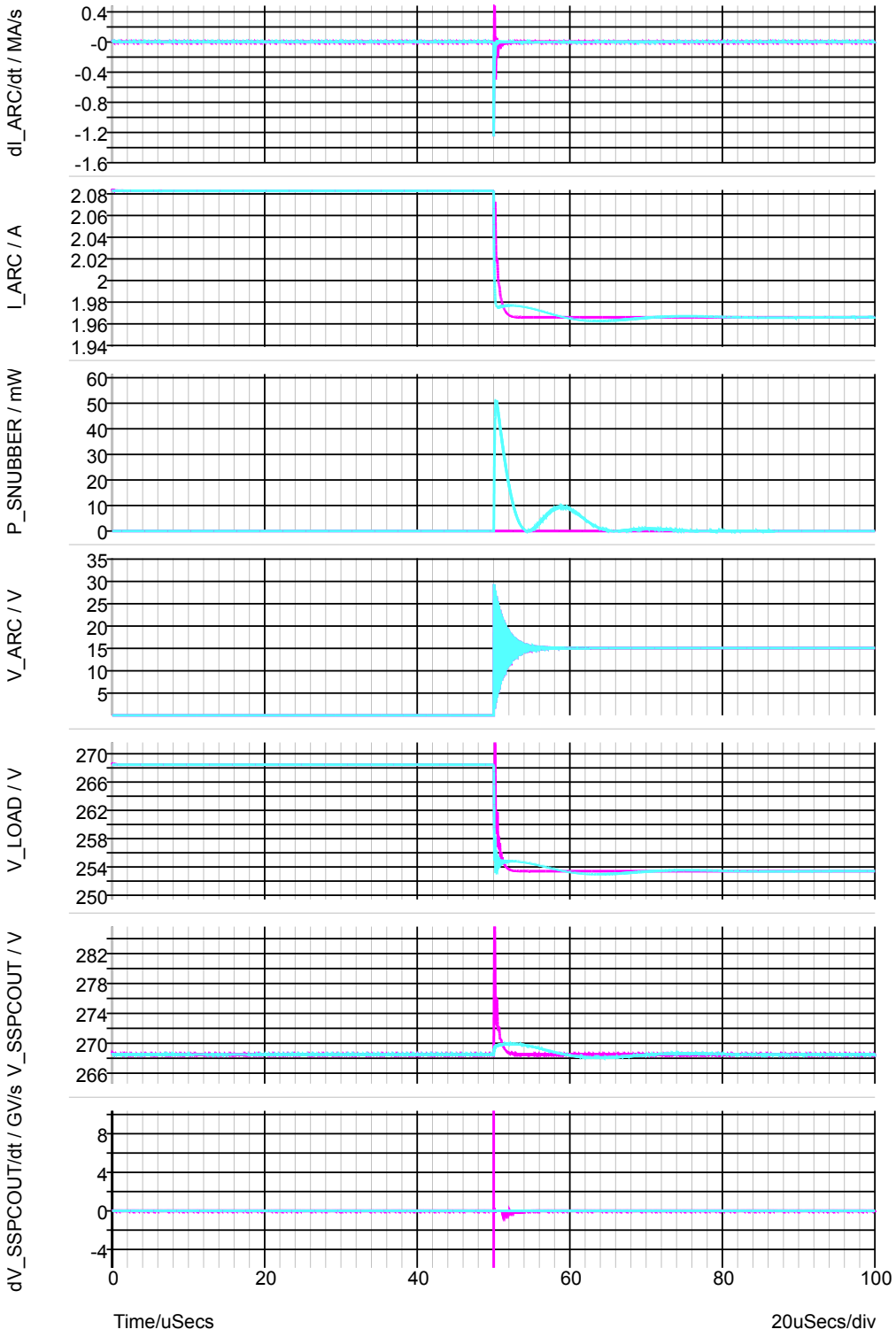


Figure B.10: Scenario 8 - Comparison of Simulation Results for Series Arc Fault - 270VDC Line, 2.5A Resistive Load / +50μH Upstream Inductance (Cyan - Simulated With Snubber, Magenta - Simulated Without Snubber)

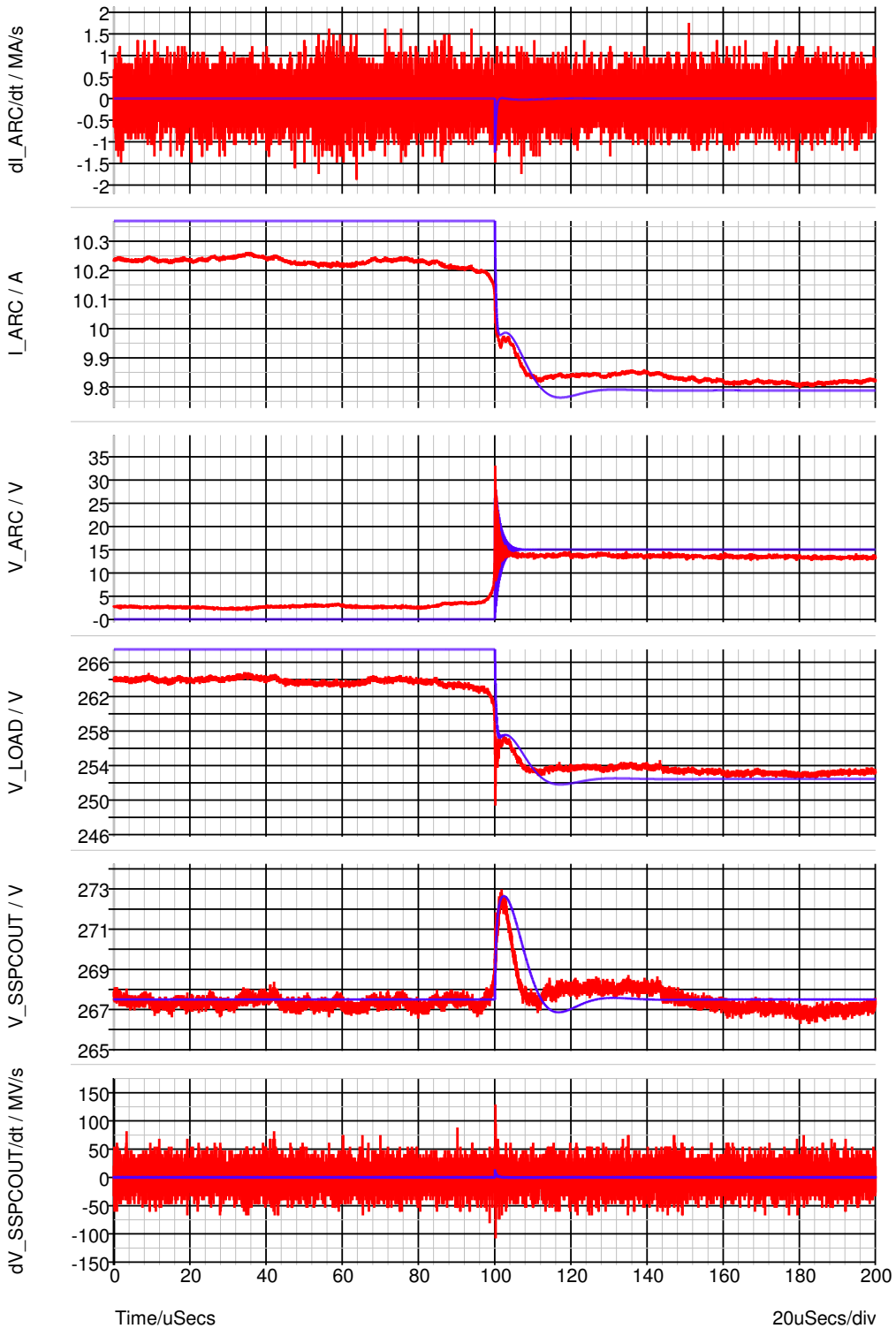


Figure B.11: Scenario 9 - Comparison of Simulation and Experimental Results for Series Arc Fault - 270VDC Line, 10A Resistive Load / +50μH Upstream Inductance (Blue - Simulated, Red - Experimental)

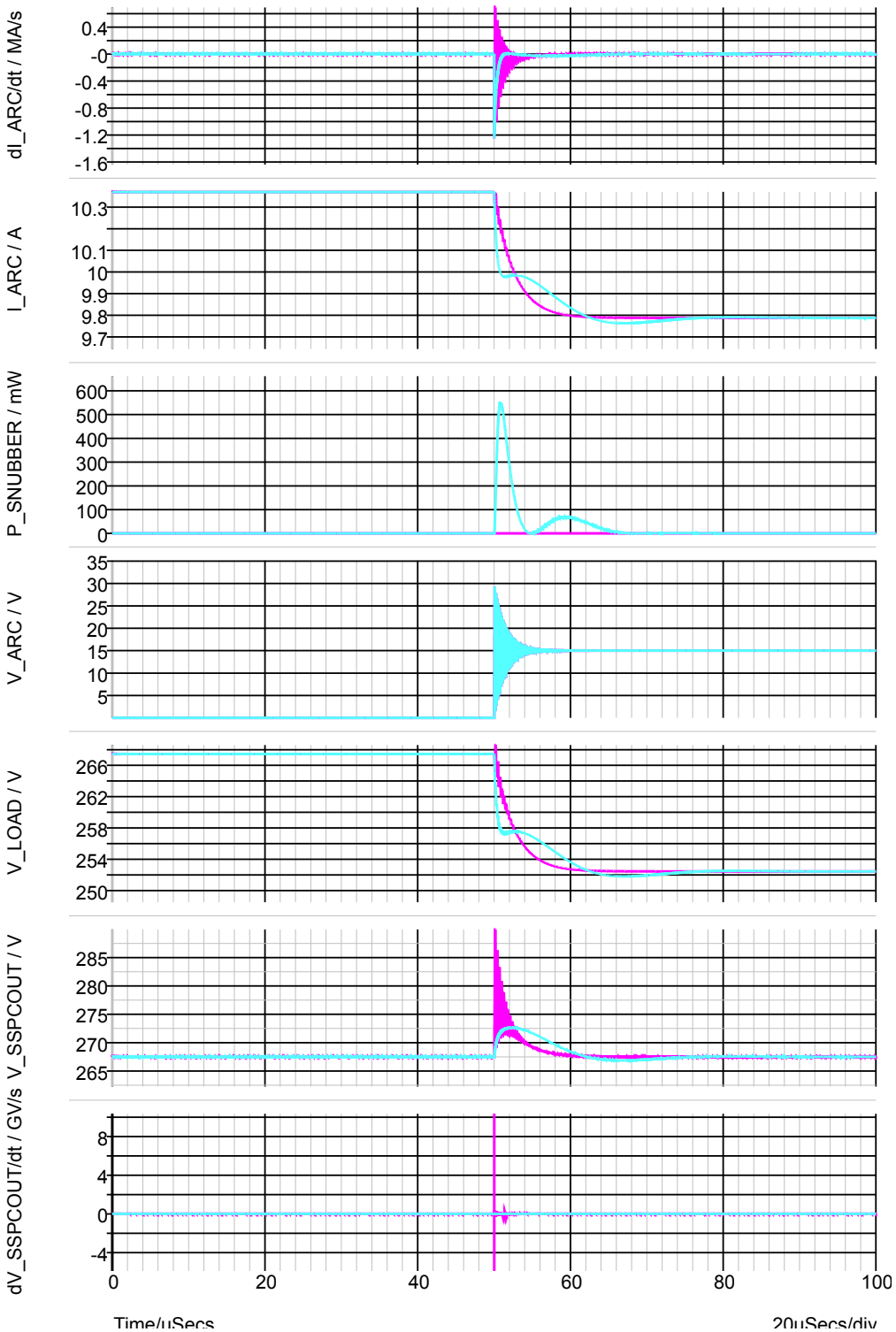


Figure B.12: Scenario 9 - Comparison of Simulation Results for Series Arc Fault - 270VDC Line, 10A Resistive Load / +50μH Upstream Inductance (Cyan - Simulated With Snubber, Magenta - Simulated Without Snubber)

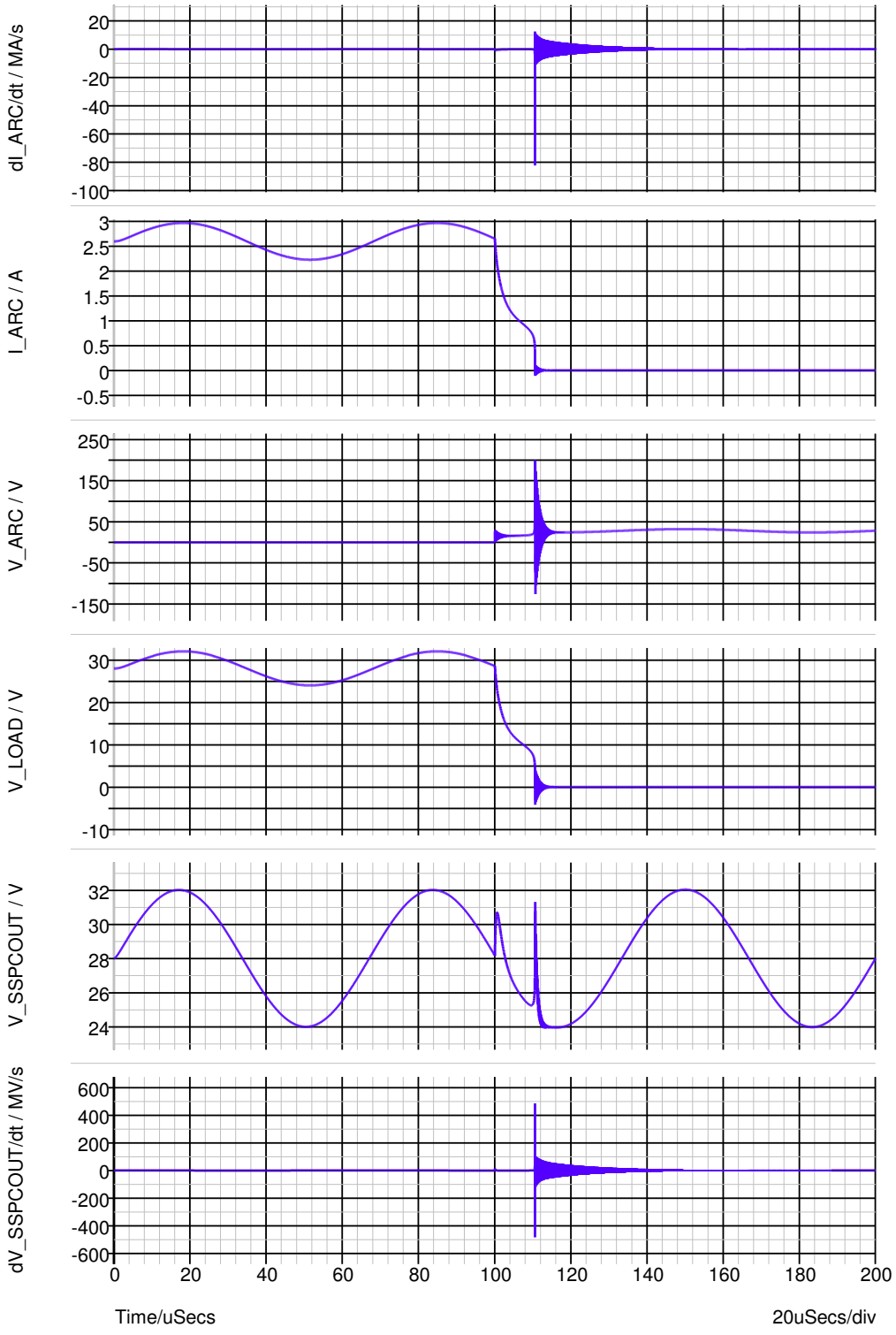


Figure B.13: Scenario 10 - Comparison of Simulation and Experimental Results for Series Arc Fault - 28VDC Line + $4V_{pk-pk}$ 15kHz, 2.5A Resistive Load (Blue - Simulated, Experimental Data Not Available)

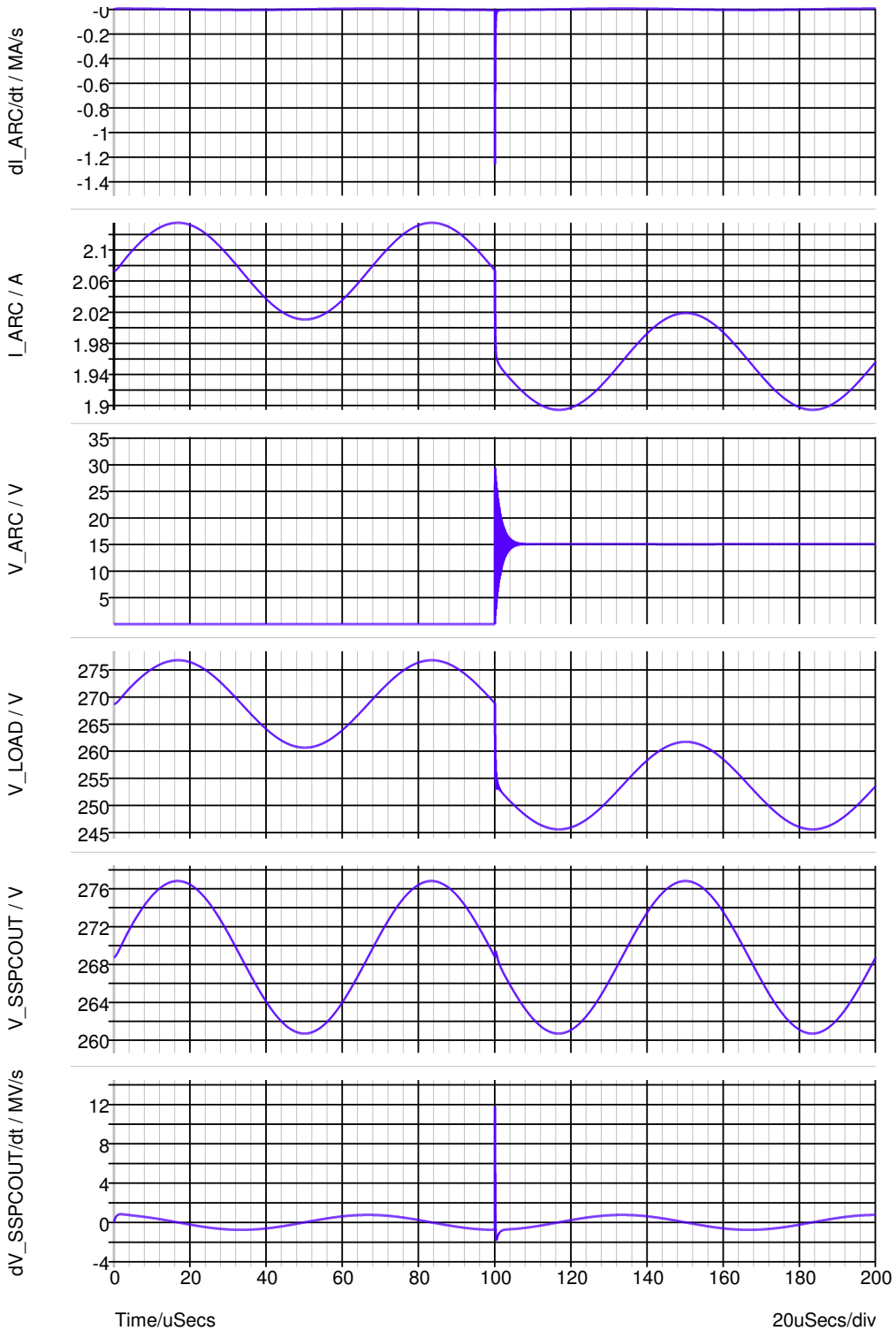


Figure B.14: Scenario 11 - Comparison of Simulation and Experimental Results for Series Arc Fault - 270VDC Line + $16V_{pk-pk}$ 15kHz, 2.1A Resistive Load (Blue - Simulated, Experimental Data Not Available)

Appendix C

Chapter 4 Support Material

C.1 Series Arc Fault Current Sensor Trade Study

The first step in the series arc fault current sensor trade study is to identify potential sensor technologies that could be deployed in the PEPDC SSPC module, and the second step is to compare the sensors to select a technology for the candidate series arc fault current sensor.

As described in Section 4.3.2 the PEPDC SSPC main current monitor uses sense resistor technology for simplicity and robustness purposes. One consideration is that the dynamic range issue that was identified could be mitigated by using a second amplifier with a higher gain parameter in order to amplify the voltage across the low impedance sense resistor. However, there is a concern that the introduction of any additional hardware must not affect the stability of the semiconductor control and monitoring electronics. The PEPDC SSPC in particular has sensitive drive electronics used to current limit during fault conditions and any hardware changes in this area must consider stability, where small PCB routing changes could have dramatic results.

A second consideration is the introduction of an additional sense resistor to the SSPC current path. This would cause further power dissipation that would detriment the SSPC thermal design. An increase in switch resistance also introduces an associated voltage drop within the SSPC hardware, where voltage drops are restricted due to both direct customer requirements and strict power quality requirements given in aerospace standards such as RTCA DO-160G [49] and MIL-STD-704F [204].

Giant Magnetoresistance is a Magnetoresistance effect found in thin-film structures composing alternating ferromagnetic and non-magnetic conductive layers. GMR devices are widely used to read hard disk drive platters [266]. Kim et al use a GMR device in a planar power module for current monitoring purposes [267]. However, the author is concerned that under high steady state magnetic fields caused by the 100%

SSPC rated current, the GMR device may suffer from saturation effects. Manufacturer NVE quote the magnetic field intensity required for saturation of their GMR products [268], and while the device can be moved away from the SSPC current carrying conductors to prevent saturation, this would reduce the signal encountered during a series arc fault. The hysteresis associated with GMR devices may also reduce sensitivity to the small field fluctuations created by the change in load currents described in Section 4.3.2, and while Mease et al propose a method of countering hysteresis this leads to a complex solution which is not suitable for aerospace [269].

Hall effect sensors are appropriate for low current DC systems, but in higher current systems where high steady-state magnetic fields are present, it is difficult to avoid core saturation. Hall effect sensors have been used in electrical power distribution systems at GE Aviation Systems Ltd for many years where they function well in a lab environment. However, they are susceptible to radiated and conducted EMC and the final engineering solution following EMC fixes is not elegant.

Rogowski coil devices are air-cored current transformers consisting of wire wound on a non-magnetic toroidal core (relative permeability $\mu_r = 1$), where the core is placed around the conductor whose currents are to be measured [270]. The use of a non-magnetic core material leads to poor coupling between the primary and secondary windings of the Rogowski coil and hence the need for many turns in order to obtain a usable transfer function. This results in the ability of the Rogowski coil to process high dI/dt currents over large ranges [257]. One disadvantage of Rogowski coils is that the many secondary windings can occupy a large volume and lead to a heavy unit. Numerous activities to create planar Rogowski coil solutions have been carried out and these tend to use multiple PCBs arranged to give the profile of a toroidal core [257; 271]. These approaches often lead to a solution that occupies a volume comparable to the toroidal core option, while achieving a minor weight saving. Moffat et al propose a printed coil which is very compact and quite high cost due to its micro-fabrication [256]. The author assumes that the micro-fabricated coil is for parallel arc fault detection based on the very small nature of the coil and associated low mutual inductance, since there appears to be insufficient coupling for detection of the small current signals created by series arc faults. A larger implementation of the planar printed coil may provide a simple solution that meets the requirements for the PEPDC series arc fault detection system.

A current transformer typically takes the form of a toroidal magnetic core (relative permeability $\mu_r > 1$), and is commonly used for bus current monitoring applications in AC electrical power distribution systems [272]. The magnetic core gives improved coupling between primary and secondary conductors, but a typical core will saturate under the high steady state magnetic fields caused by high DC currents (up to 120A

in the PEPDC SSPC). Current transformer technology is therefore of limited use in this application.

The fluxgate magnetometer was invented by Victor Vacquier in the 1930s during his time working for Gulf Research Laboratories where he applied the technology to submarine detection [273]. This technology has later been applied to current sensing in areas where a wide current measurement range is required, and a popular application is that of battery current monitoring where large ranges of DC currents can occur. The technology utilises the saturation state of a magnetic circuit which limited the usefulness of the current transformer described earlier. Jerez et al propose a toroidal core wound with both a sense winding and an excitation winding. The goal of this is to achieve a null magnetic field in the magnetic circuit, and in order to achieve this the excitation coil must be excited sufficiently to cancel out the flux generated by the sense winding [274; 275]. The fluxgate system therefore requires significant power to supply the excitation coil and additional signal processing circuitry, which in turn leads to higher cost, weight and volume which is of particular interest when considering the application of this technology to each switched output in an electrical power distribution system.

Note: Since carrying out this trade study in 2011, Texas instruments have demonstrated an integrated circuit solution for fluxgate sensing which draws a maximum quiescent current of 11mA at 3.3VDC supply voltage and this could be explored for future designs [276; 277].

Table C.1 shows the author's subjective ratings in a simple evenly-weighted matrix trade study where 5 indicates good relative performance and/or a low risk, and 1 indicates relatively bad performance and/or a high risk. This data is based on the author's review of existing products within GE Aviation Systems Ltd, industry and academic papers (the basic principles from these are covered earlier in this section) and supplier presentations. The evaluation criteria for the trade study have come from the top level system requirements presented in Section 4.2 which are cost, weight, volume, thermal and EMC/EPV risk. As mentioned in Section 4.2, stability of the PEPDC SSPC current monitor is also important where no hardware introduced shall affect the stability of the existing system. The derived hardware requirements outlined in Section 4.3.1 define the requirements for series arc fault current sensor sensitivity, measurement range, bandwidth and high voltage isolation. Since a number of magnetic sensors have been reviewed and considered, saturation, hysteresis and temperature stability also need to be considered. Finally in aerospace ageing is also a consideration where parts are expected to function without failure for 25+ years.

Technology	Weight	SSPC Control Stability	Volume	Cost	EMC/EPV Risk	Thermal	Saturation	Hysteresis	Bandwidth	Sensitivity	Temperature Stability	Ageing	Isolation	Total
SSPC Sense Resistor	5	1	5	5	5	1	5	5	3	1	3	3	1	43
Extra Sense Resistor	3	5	3	4	5	5	5	5	3	3	3	3	1	48
GMR	4	5	4	2	1	1	1	1	4	3	3	3	5	37
Hall Effect	2	5	3	3	1	4	1	5	1	1	1	1	5	33
Rogowski Coil	**4**	**5**	**3**	**4**	**1**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**57**
Current Transformer (CT)	2	5	3	3	1	4	1	5	5	5	5	1	5	45
Fluxgate Transducer	1	5	1	1	1	1	4	5	5	5	5	1	5	45

Table C.1: Simple Evenly-Weighted Series Arc Fault Current Monitor Trade Study

Table C.1 further shows that the Rogowski Coil solution scores highest in the simple trade study where its limiting features in order of severity are EMC/EPV risk where interfering RF fields could cause nuisance trips, volume and weight where the number of secondary windings required is unknown, and finally cost which is significant since the existing SSPC current monitor cannot be exploited.

Rogowski coils have been implemented using PCB technology [257; 271] and attempts have been made to microfabricate planar current transformers [256], however, the author is concerned that small coils would not have the necessary coupling / mutual inductance to obtain a sufficient series arc fault signal based on the characterisation work carried out in Appendix A. A planar multi-layer PCB solution would address the cost, weight and volume requirements since compact planar current transformers can easily be incorporated into the proposed 8 layer, 2oz/ft^2 copper construction for the PEPDC SSPC module with little impact on the weight and volume of the module. The 8 layer construction also allows multi-layer current transformers to be designed if necessary. Assuming the use of four coils (one pair of coils on the PEPDC SSPC input busbar, and another pair on the output busbar) where each coil is 20mm $\times$ 12mm in area and all six inner layers on the PCB are used with 50% copper coverage then the mass of the coils m can be estimated. The mass per unit area d for each copper layer is 6.1×10^{-4} g/mm^2. First calculate the Copper area a using Equation

(C.1), and second calculate the coil mass m using Equation (C.2).

$$a = 4 \times 6 \times (20 \times 12) \times 0.5 = 2880mm^2 \quad \text{(C.1)}$$

$$m = ad = 2880 \times \left(6.1 \times 10^{-4}\right) = 1.8g \quad \text{(C.2)}$$

The increase in mass for the printed coils is negligible, and therefore this concept is feasible assuming that the associated signal conditioning circuitry has a similar mass.

C.2 Rectangular Bus Bar B-Field Plot Code Listing

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Script Name :    RectangularField                                             %
%                                                                               %
% Filename :       RectangularField.m                                           %
%                                                                               %
% Purpose :        To compute the B-field generated by a rectangular            %
%                  busbar, and to display the data on a surface plot.           %
%                                                                               %
% Author :         Peter Handy                                                  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all

% Declare the permeability of free space...
mu0 = 4 * pi * 10^-7;

% Declare busbar dimensions and input current...
I = 1;
w = 0.018;
t = 0.0015;

% Declare x and y size and resolution of surface plot in meters...
minelement = 0.00025;
x = -0.05:minelement:0.05;
y = -0.05:minelement:0.05;

% Scan both the x and y plot area and calculate field for each matrix
% element...
for j = 1:1:length(x)

    for i = 1:1:length(y)

        % Calculate W1...
    W1(i) = (((w + (2*x(j)))/4) * log(((w/2 + x(j))^2 + (t/2 - y(i))^2)/((w/2 + x(j))^2 + (
        t/2 + y(i))^2))) + (((w - (2*x(j)))/4) * log(((w/2 - x(j))^2 + (t/2 - y(i))^2)/((w
        /2 - x(j))^2 + (t/2 + y(i))^2))) + ((t/2 - y(i)) * (atan((w - 2*x(j))/(t - 2*y(i)))
         + atan((w + 2*x(j))/(t - 2*y(i))))) - ((t/2 + y(i)) * (atan((w - 2*x(j))/(t + 2*y(
        i))) + atan((w + 2*x(j))/(t + 2*y(i)))));

        % Calculate W1...
    W2(i) = (((t + (2*y(i)))/4) * log(((w/2 - x(j))^2 + (t/2 + y(i))^2)/((w/2 + x(j))^2 + (
        t/2 + y(i))^2))) + (((t - (2*y(i)))/4) * log(((w/2 - x(j))^2 + (t/2 - y(i))^2)/((w
        /2 + x(j))^2 + (t/2 - y(i))^2))) + ((w/2 - x(j)) * (atan((t - 2*y(i))/(w - 2*x(j)))
         + atan((t + 2*y(i))/(w - 2*x(j))))) - ((w/2 + x(j)) * (atan((t - 2*y(i))/(w + 2*x(
        j))) + atan((t + 2*y(i))/(w + 2*x(j)))));

    % Calculate x-component of B-field...
    Bx(i,j) = ((mu0 * I)/(2*pi*w*t)) * W1(i); % set to zero to see only y field
         contribution...

    % Calculate y-component of B-field...
    By(i,j) = -((mu0 * I)/(2*pi*w*t)) * W2(i);

    % Calculate magnitude of B-field...
    Bmag(i,j) = sqrt(By(i,j)^2 + Bx(i,j)^2);

    end
end
```

```
%%
% Create a new figure area...
figure('color','white');

% Plot the magnitude of the B-field in the left hand area...
subplot(1,3,1); surface(1000*x,1000*y,Bmag);
shading interp
c1=colorbar('SouthOutside');
hold on;
grid minor;
axis square;
xlabel('X Dimension (mm)');
ylabel('Y Dimension (mm)');
xlabel(c1,'Magnitude of B Field (T)')
title('Magnitude of B Field');

% Plot rectangular busbar shape outline...
view(2)
linex = [1000*(-w/2), 1000*(w/2), 1000*(w/2), 1000*(-w/2), 1000*(w/2)];
liney = [1000*(t/2), 1000*(t/2), 1000*(-t/2), 1000*(-t/2), 1000*(-t/2)];
plot3(linex,liney,repmat(max(max(Bmag)),1,5),'color','black');

% Plot the y-component of the B-field in the centre area...
subplot(1,3,2); surface(1000*x,1000*y,By);
shading interp
c2=colorbar('SouthOutside');
hold on;
grid minor;
axis square;
xlabel('X Dimension (mm)');
ylabel('Y Dimension (mm)');
xlabel(c2,'By Field Component (T)')
title('By Field Component');

% Plot rectangular busbar shape outline...
view(2)
linex = [1000*(-w/2), 1000*(w/2), 1000*(w/2), 1000*(-w/2), 1000*(w/2)];
liney = [1000*(t/2), 1000*(t/2), 1000*(-t/2), 1000*(-t/2), 1000*(-t/2)];
plot3(linex,liney,repmat(max(max(Bmag)),1,5),'color','black');

% Plot the x-component of the B-field in the right hand area...
subplot(1,3,3); surface(1000*x,1000*y,Bx);
shading interp
c3=colorbar('SouthOutside');
hold on;
grid minor;
axis square;
xlabel('X Dimension (mm)');
ylabel('Y Dimension (mm)');
xlabel(c3,'Bx Field Component (T)')
title('Bx Field Component');

% Plot rectangular busbar shape outline...
view(2)
linex = [1000*(-w/2), 1000*(w/2), 1000*(w/2), 1000*(-w/2), 1000*(w/2)];
liney = [1000*(t/2), 1000*(t/2), 1000*(-t/2), 1000*(-t/2), 1000*(-t/2)];
plot3(linex,liney,repmat(max(max(Bmag)),1,5),'color','black');

% Set figure window to a know size...
set(gcf, 'OuterPosition', [50,50,1000,600]);
% Note... Print on A3 actual size, centered...
```

C.3 Rogowski Coil De-risk Rig Drawing

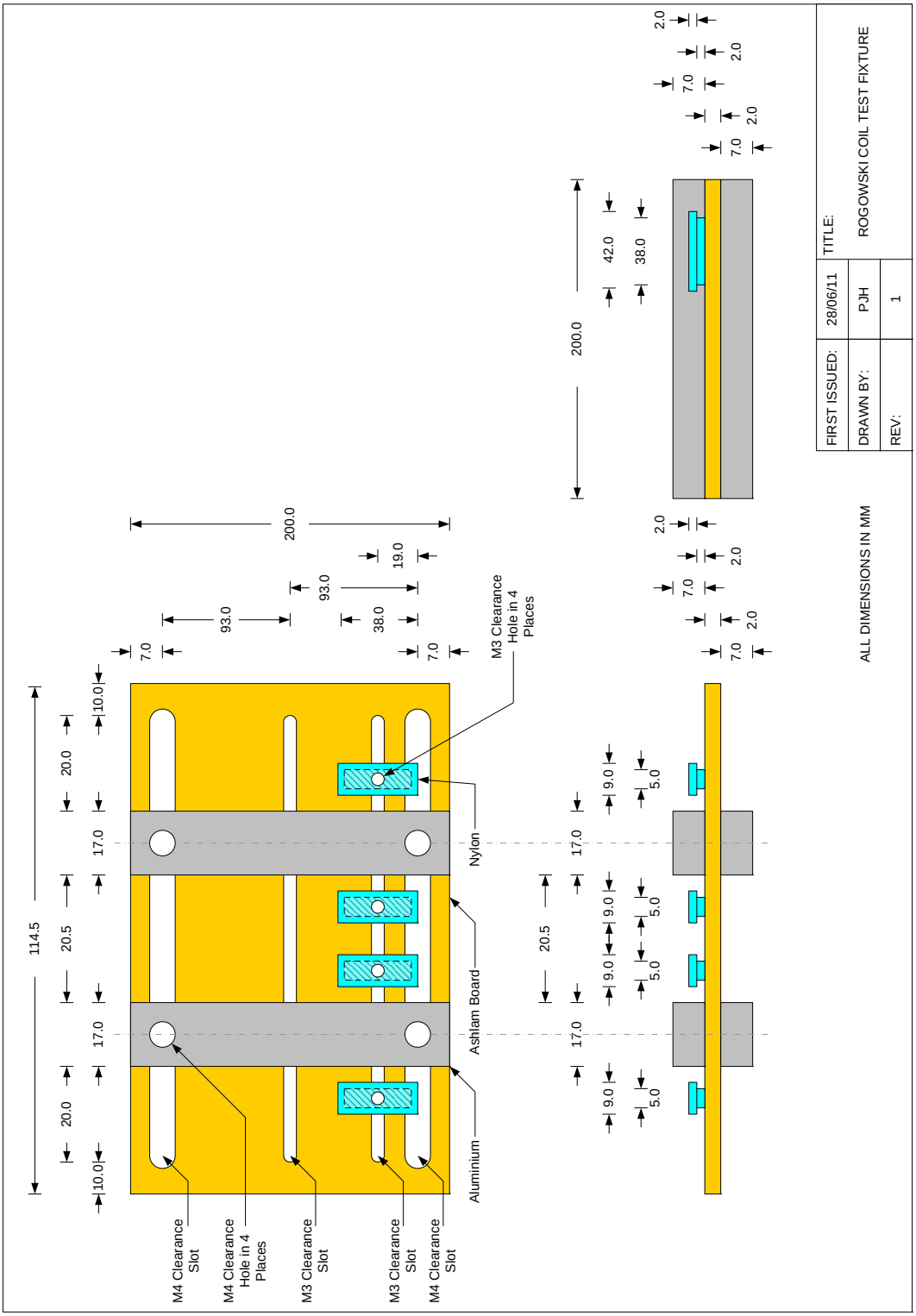


Figure C.1: First Rogowski Coil Hardware De-risk Rig

C.4 Rogowski Coil Frequency Domain Performance

C.4.1 Frequency Domain Test Configurations

The frequency domain testing of the planar coil designs can be broadly split into two parts, input return loss (S_{11}) and forward transmission (S_{21}). The input return loss is of interest in order to determine the self-resonant properties of the planar current transformers, and the forward transmission characteristics are important in order to estimate coupling between the bus bars and the planar current transformers. The frequency sweep used was 5Hz through 500MHz consisting of 801 data points, with an Intermediate Frequency (IF) bandwidth of 4kHz and a source power of 0dBm.

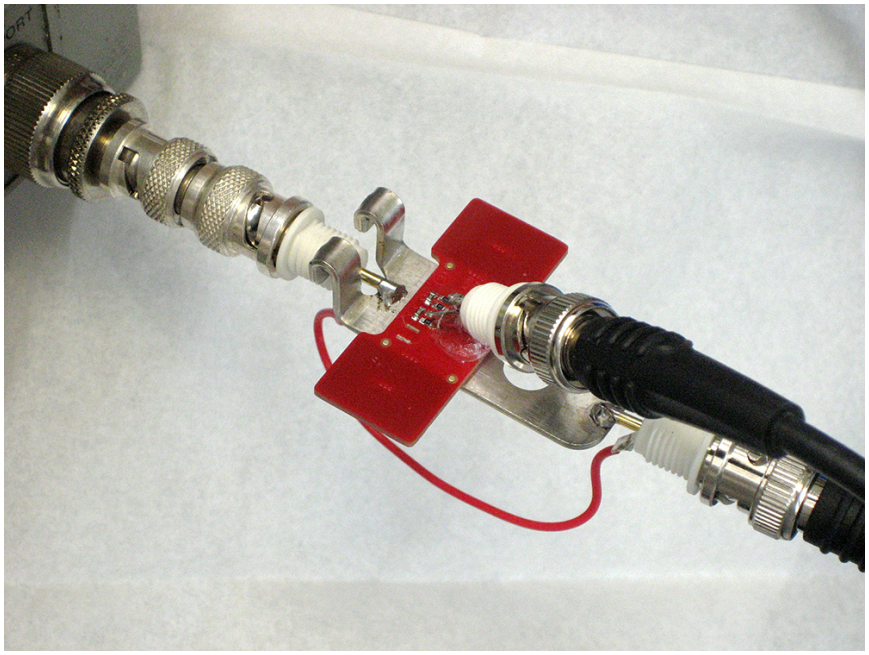


Figure C.2: PEPSC Network Analyser Configuration (Photograph)

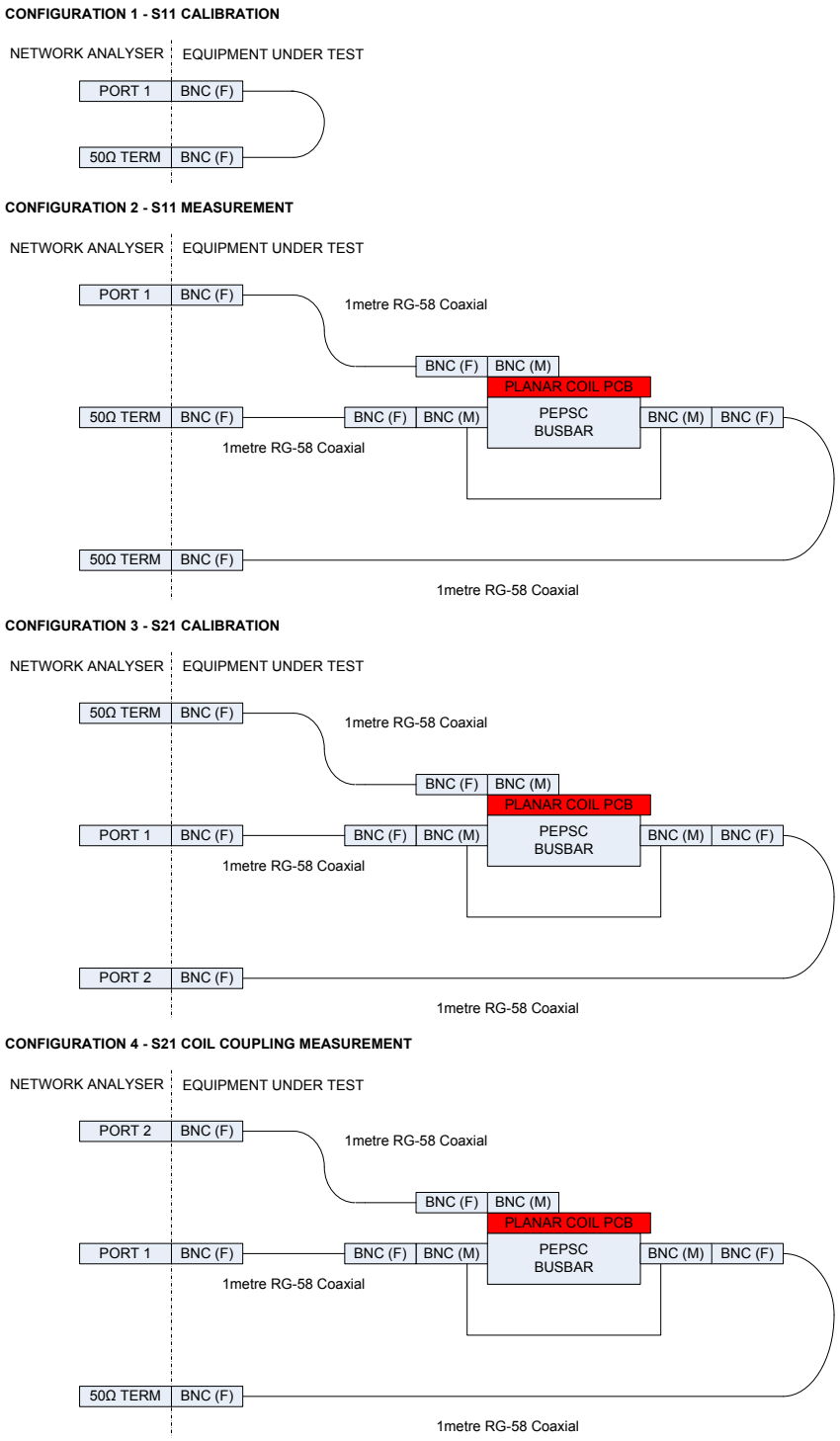


Figure C.3: PEPSC Network Analyser Configuration (Schematic)

Figures C.2 and C.3 show how the PEPSC busbar and planar current transformer board were configured during the input return loss (S_{11}) and forward transmission (S_{21}) measurements. Considerable thought was put into the validation of the test methodology here, paying particular care to the calibration of the network analyser

instrument used to determine the current transformer performance. The network analyser used for all frequency domain testing was the Agilent 8751A.

Configuration 1 was designed to enable calibration of the input return loss (S_{11}) measurement scheme. During the input return loss (S_{11}) calibration the Agilent 8751A requires connection of a short circuit, open circuit and 50Ω load termination. Port 1 of the network analyser was connected via a 1 meter RG-58 coaxial cable to an open, short and 50Ω termination resistor as required, thus calibrating out the effect of the coaxial cable in future measurements.

Configuration 2 was designed to perform the calibrated input return loss (S_{11}) measurement. During measurement of the input return loss (S_{11}), Port 1 is connected to the planar coil PCB. The PEPSC busbar is connected to two 1 meter lengths of RG-58 coaxial cable. Since the planar coil PCB does not feature a large interface connector, connection is made via a male BNC connector soldered across the input burden resistors.

Configuration 3 was designed to enable calibration of the forward transmission (S_{21}) measurement scheme. Measurement of the forward transmission (S_{21}) characteristics is somewhat more complex since the current-to-voltage transfer characteristics are of interest here. Whilst the PEPSC busbar could be connected across a single network analyser port, the author was concerned that the current through the busbar was uncontrolled and therefore a three port scheme was devised. In order to calibrate the three port system, Port 1 is connected to the input of the PEPSC busbar and Port 2 is connected to the output of the PEPSC busbar during the S_{21} response calibration on the network analyser. This normalises the busbar frequency response to 0dB across the frequency range.

Finally Configuration 4 was designed to perform the calibrated forward transmission (S_{21}) measurement. During measurement of the forward transmission (S_{21}) characteristics and following calibration, Port 2 of the network analyser is replaced by a 50Ω load termination, and Port 2 is now connected to the planar coil PCB thus allowing calibrated measurement of the coupling between the input busbar and planar coil PCB to be made.

Figures C.4 and C.5 show how the PEPDC PCB assembly is configured during the input return loss (S_{11}) measurements. The network analyser used for all frequency domain testing was the Agilent 8751A. For PEPDC S_{11} measurements, the network analyser was calibrated using the technique described under Configuration 1.

During measurement of the input return loss (S_{11}) in Configuration 5, Port 1 is connected to the planar coil which is embedded in the PEPDC SSPC PCB. Since the planar coils on the PEPDC do not feature a large interface connector, connection is

made via a male BNC connector soldered across the input burden resistors. Figure C.4 illustrates the test equipment configuration for the testing of input return loss (S_{11}) for Coil 2, which is also depicted by the photograph of the physical PEPDC hardware in Figure C.5.

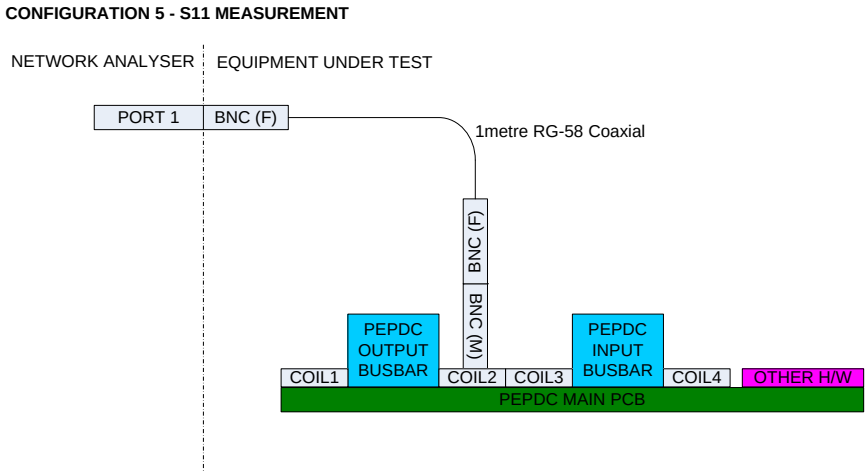


Figure C.4: PEPDC Network Analyser Configuration (Schematic)

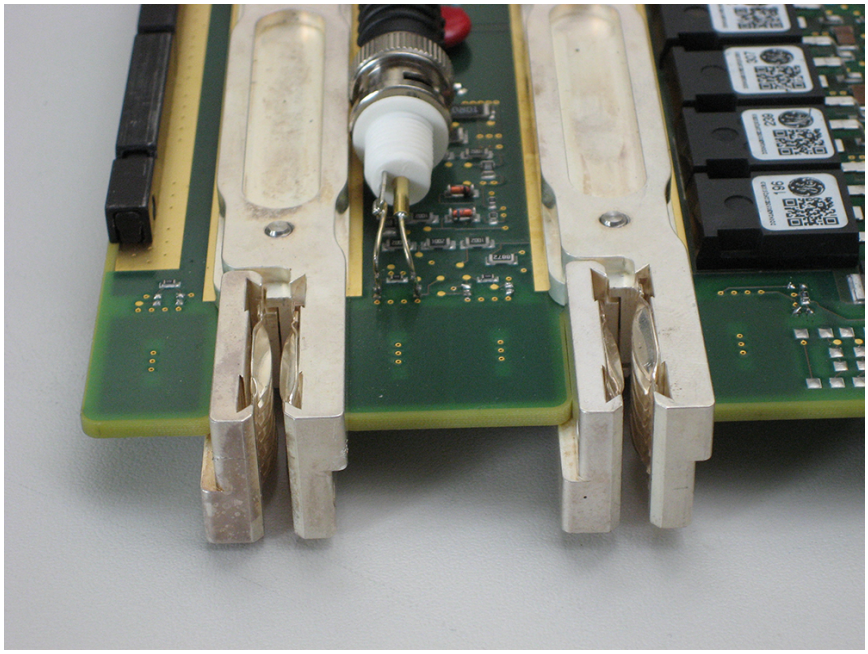


Figure C.5: PEPDC Network Analyser Configuration (Photograph)

C.4.2 Frequency Domain Performance Results

PEPSC Input Return Loss, S_{11}

Figure C.6 shows the input return loss S_{11} for the PEPSC planar current transformer. To verify consistency between each of the coils on the PEPSC Rogowski coil board, input return loss measurements were taken for left and right hand coils with and without 100Ω burden resistors in parallel with each coil. The Results between left and right hand coils are consistent. Any variation is likely to be caused by the non-isotropic nature of the FR-4 PCB laminate material and the non symmetric routing used to connect the left and right hand coils to the burden resistor network.

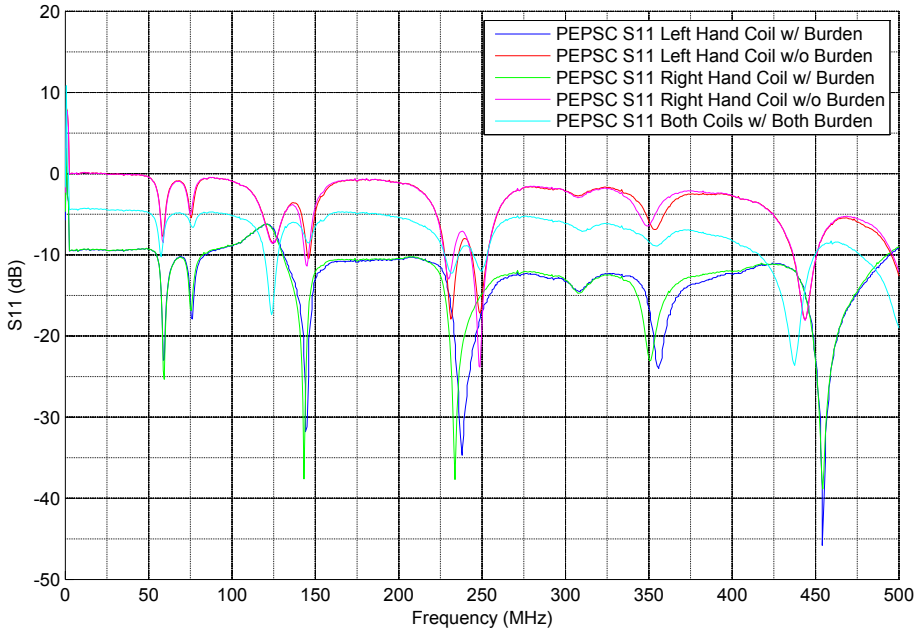


Figure C.6: PEPSC Planar Coil S_{11} Measurements

Input return loss measurements identify the resonant frequencies of the coils. The plot showing S_{11} for both coils with both burden resistors fitted indicates resonances at frequencies of 60MHz, 75MHz, and 125MHz. Further resonances are seen as the stimulation frequency is swept up to 500MHz and this behaviour is consistent with the complex PEEC model presented earlier in this section. The resonant frequency of the coils could be increased by minimising interlayer capacitance but this would result in fewer turns on each coil thus resulting in lower mutual inductance thus reducing sensitivity.

PEPSC Forward Transmission, S_{21}

Forward transmission characteristics S_{21} are included in the analysis of the current transformer to understand the coupling between the primary and secondary current transformer windings. The graph of the forward transmission characteristics S_{21} in Figure C.7 shows that the resonances seen in the input return loss S_{11} are comparable to those seen in the S_{21} response.

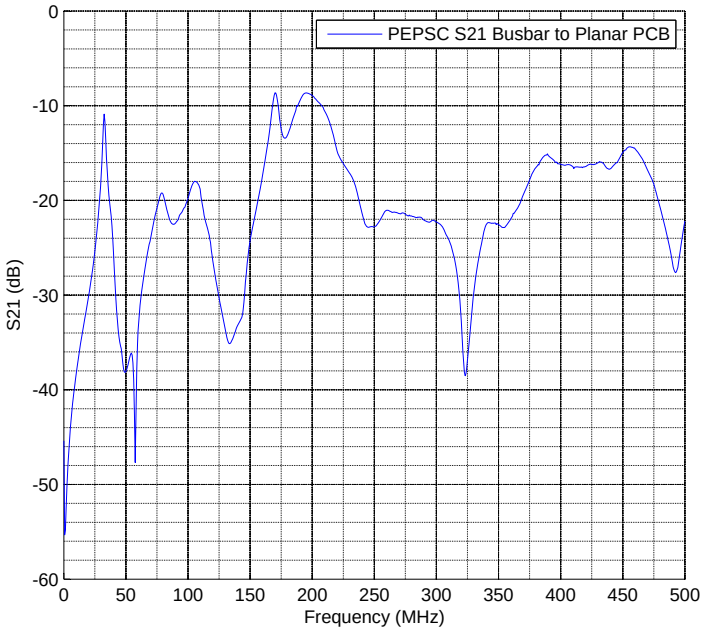


Figure C.7: PEPSC Planar Coil S_{21} Measurements

This is a far less than an ideal response for a linear current sensor, however this sensor should still perform well as a $\frac{dI}{dt}$ detector. If the resonances become an issue for time domain measurements then a two layer coil could be created to verify that the resonances are caused predominantly by interlayer capacitance, and that two layers featuring offset coils minimises this interlayer capacitance.

PEPDC Input Return Loss, S_{11}

Figures C.8 and C.9 show the input return loss S_{11} for the PEPDC planar current transformers. To verify consistency between each of the coils on the PEPDC main PCB assembly, input return loss measurements were taken for each of the four coils with and without 100Ω burden resistors in parallel with each coil. The Results between left and right hand coils are consistent.

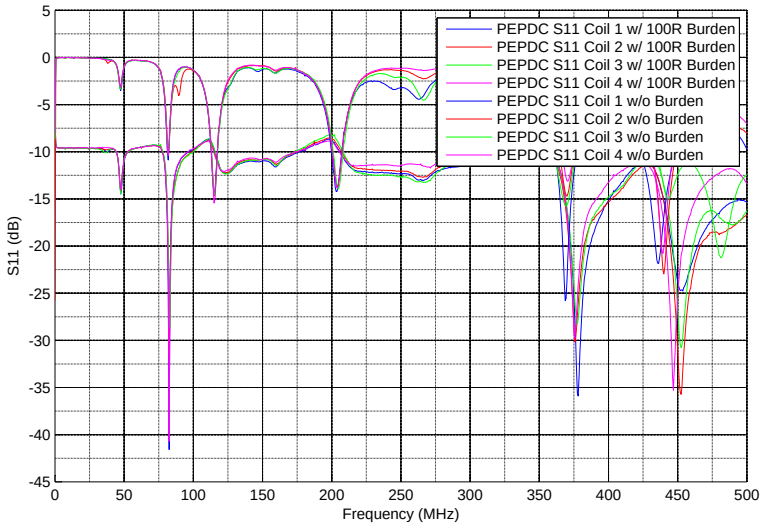


Figure C.8: PEPDC Planar Coil S_{11} Measurements, Individual Coils

The input return loss for unburdened coils shows that there are resonances at 45MHz, 80MHz, 135MHz and 210MHz, where no further resonances are seen until >350MHz. The lowest return loss is seen at 80MHz, and given that linearity is not an issue for this dI/dt sensor, this should be adequate. It can be observed that the 45MHz, 80MHz and 135MHz resonances are present with and without burden resistors, however the resonance at 210MHz is greatly reduced with the addition of the 100Ω burden resistors. This shows how burden resistors have the effect of reducing resonances at the expense of reduced sensitivity.

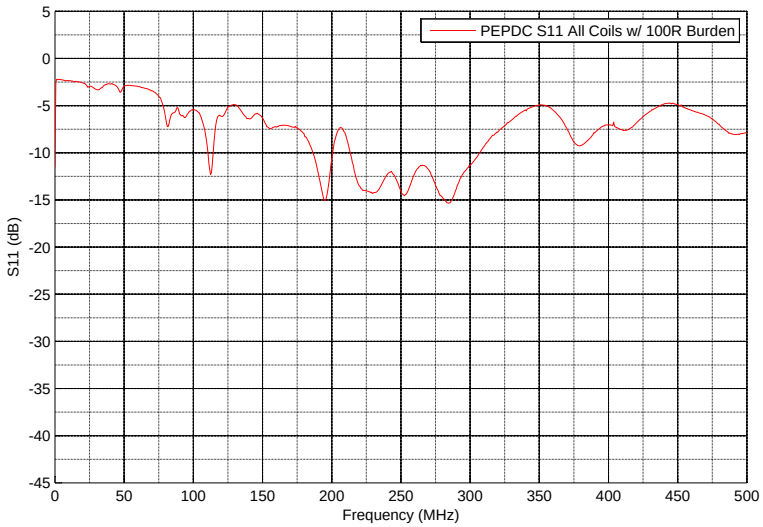


Figure C.9: PEPDC Planar Coil S_{11} Measurements, All Coils in Series

Observing Figure C.9 where each of the four coils are wired in a series configuration the resonant circuit behaviour is affected by the impedance of each coil and the resonant peak at 45MHz is now less visible. Higher magnitude peaks are now present at 110MHz and 195MHz, where these peaks should not affect the time domain performance significantly. When EMC susceptibility testing the PEPDC unit these resonances should be considered in the event of outages.

The resonances seen in the PEPDC coil results are lower in frequency than those seen in the PEPSC coil results and this is due to the reduced number of turns on each layer of the PEPSC design. The fewer turns in the PEPSC design results in both reduced self inductance and reduced parasitic capacitance which in turn produces higher frequency resonances.

PEPDC Forward Transmission, S_{21}

Given the results obtained during PEPSC forward transmission (S_{21}) measurements, it was determined that this parameter is of little use compared with the time domain characterisation activity and therefore this measurement was not carried out on the PEPDC PCB assembly. In addition to this it is not possible to measure this performance without an unpopulated PCB since the power switching components, in particular the load / line snubbers, load the output of the sweep generator in the network analyser leading to inaccurate results.

C.5 Full PEPDC Planar Current Transformer Design

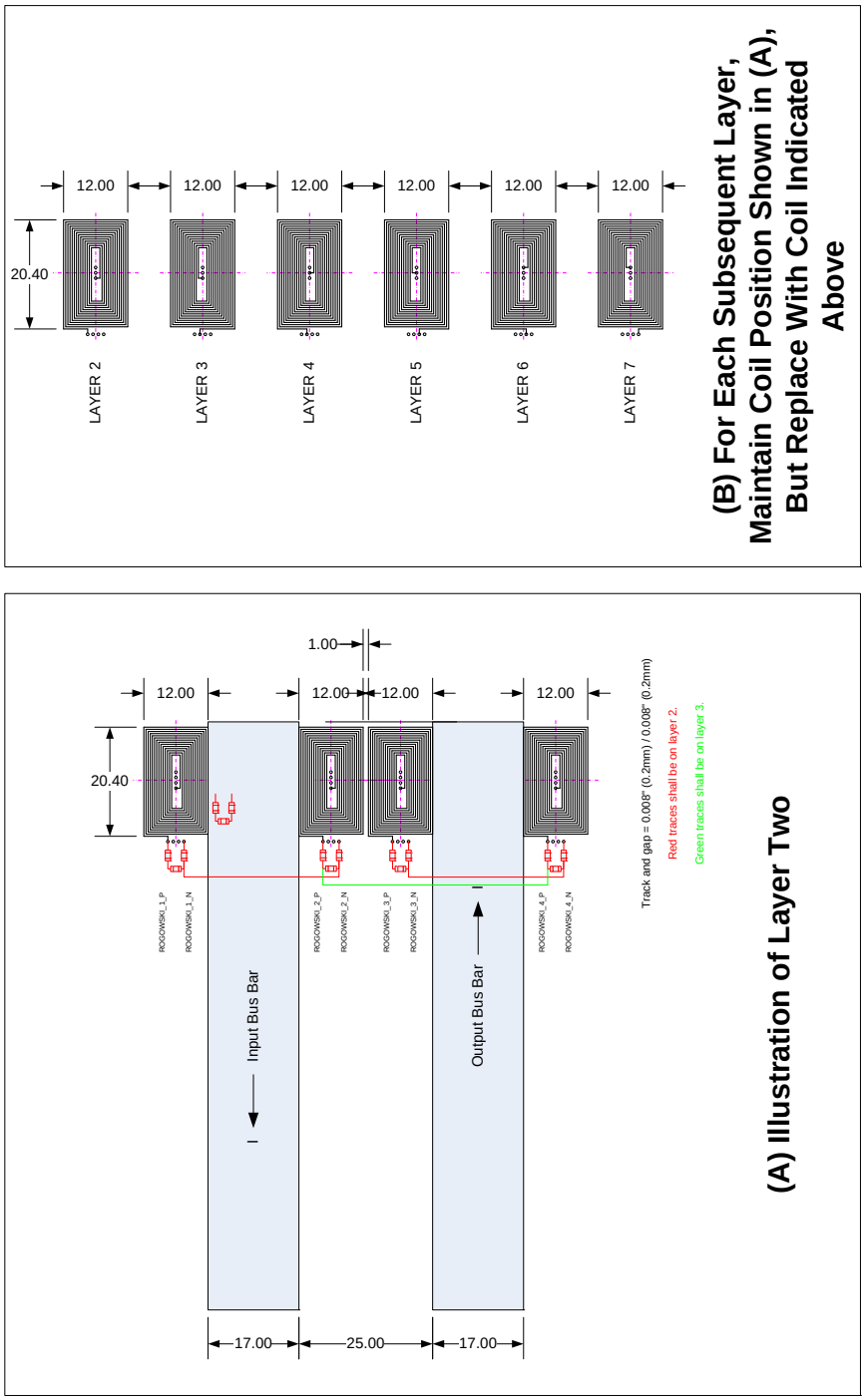
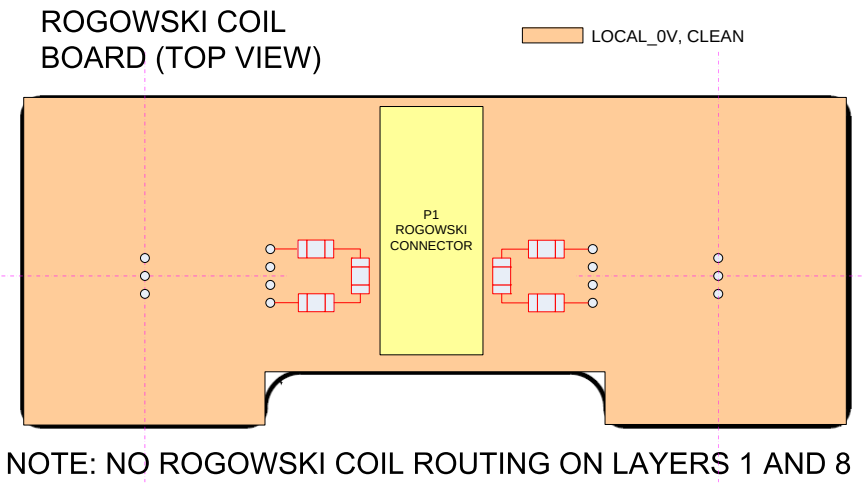


Figure C.10: Full PEPDC Arc Fault Current Monitor Current Transformer Design

C.6 Full PEPSC Planar Current Transformer Design



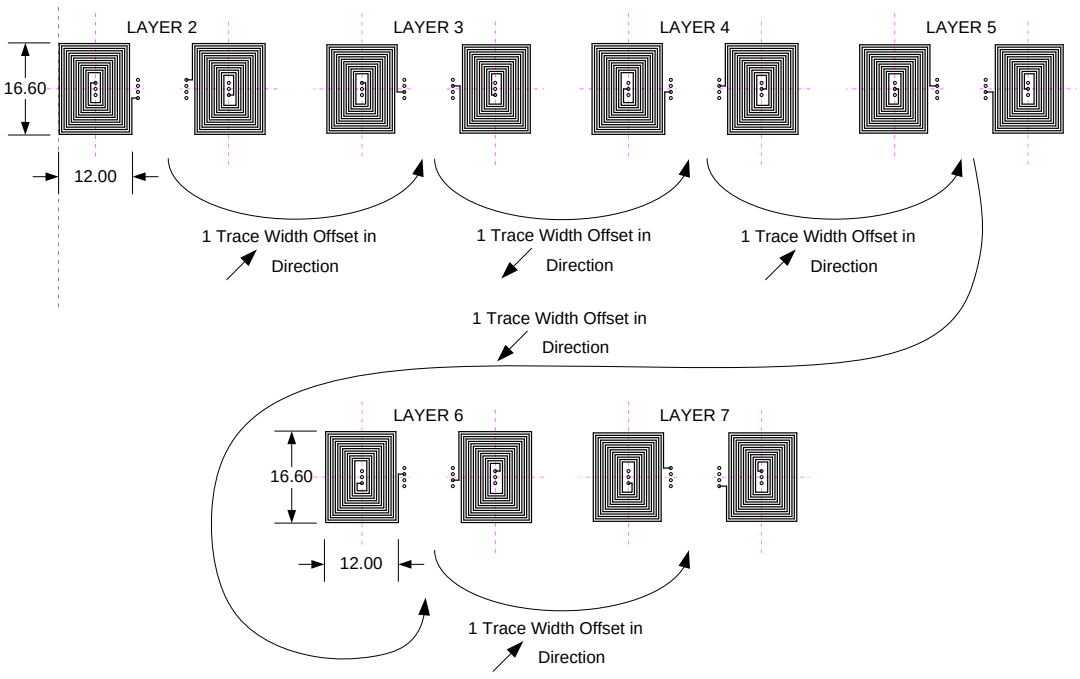


Figure C.11: Full PEPSC Arc Fault Current Monitor Current Transformer Design

C.7 Full PEPDC Arc Fault Current Monitor

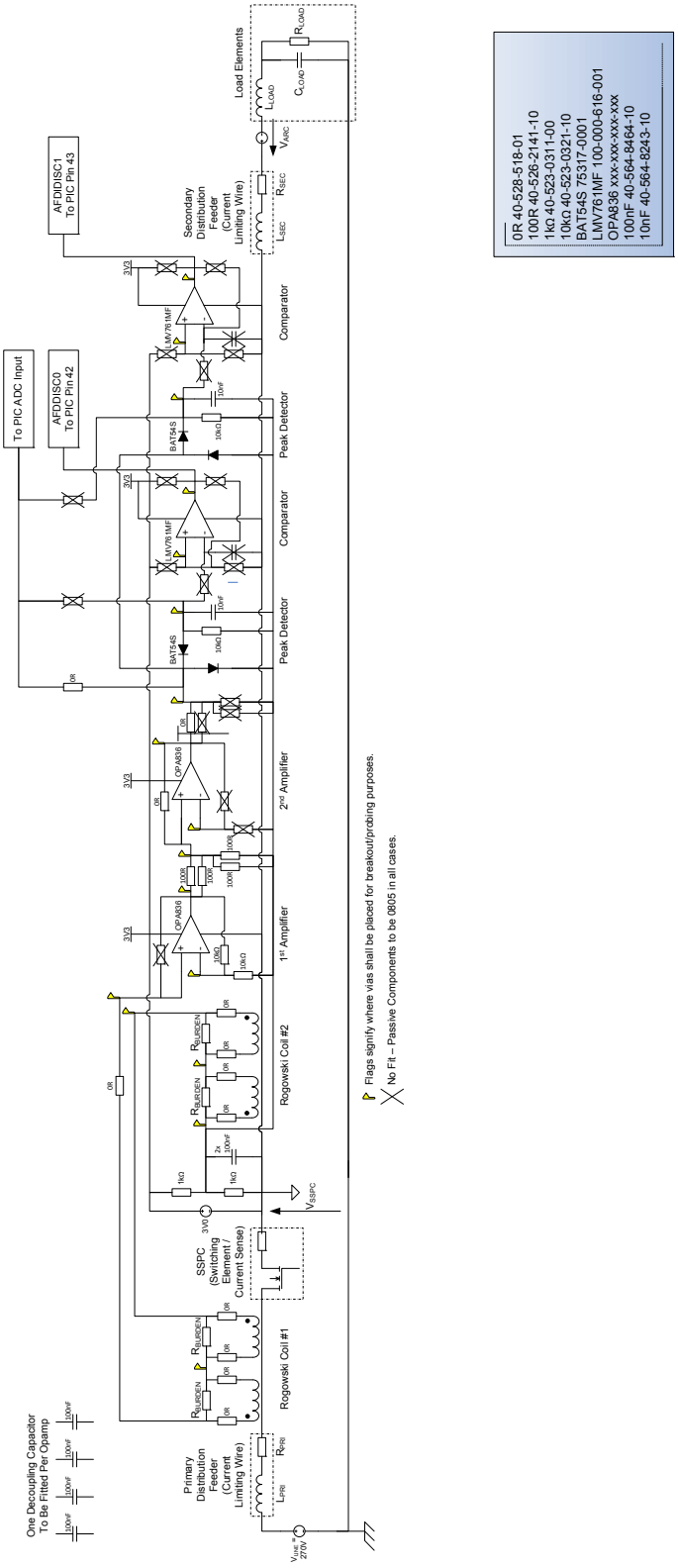


Figure C.12: Full PEPDC Arc Fault Current Monitor Schematic

C.8 Full PEPDC Arc Fault Voltage Monitor

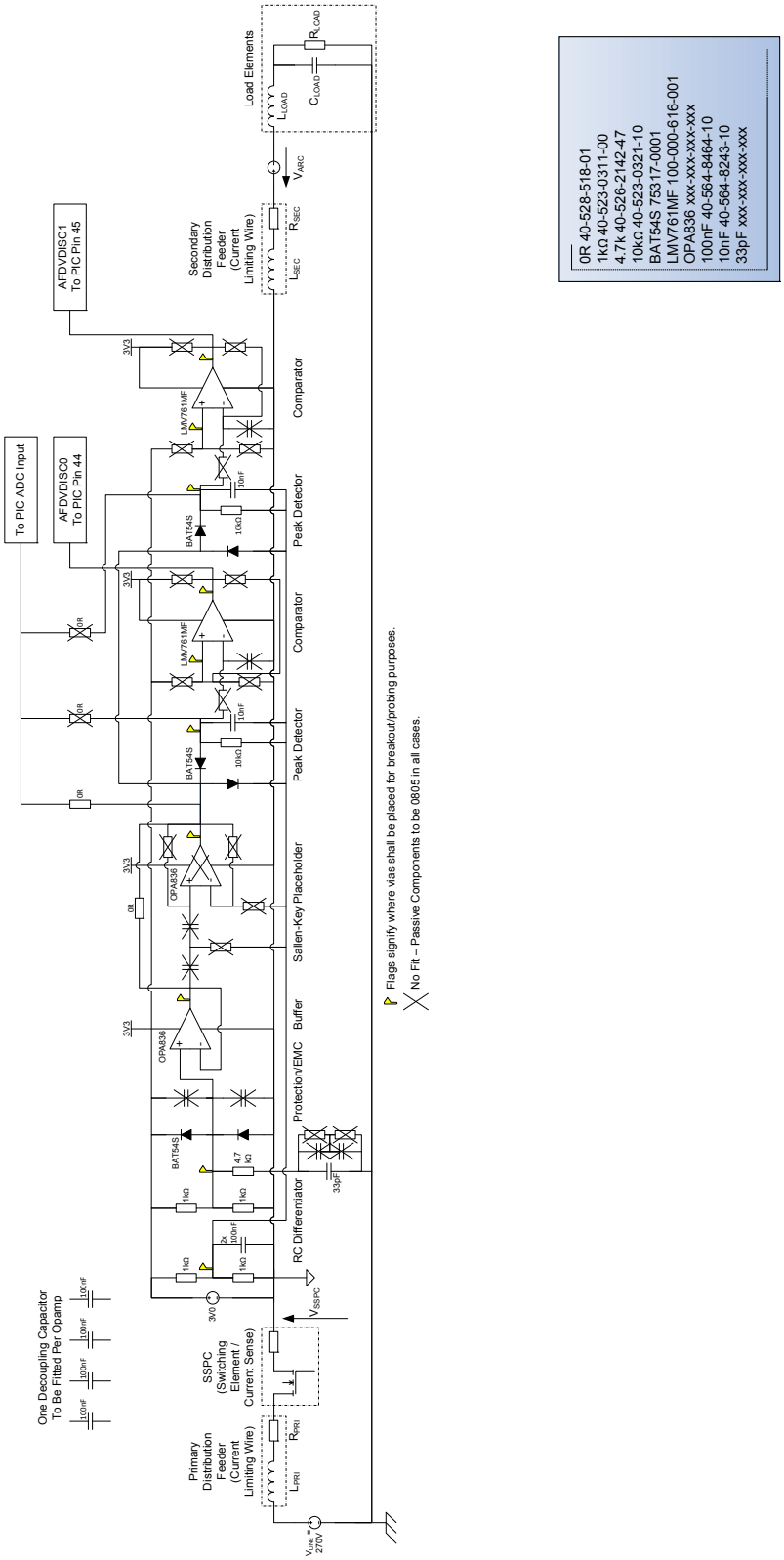


Figure C.13: Full PEPDC Arc Fault Voltage Monitor Schematic

C.9 PEPDC / PEPSC Statistical Software Algorithm

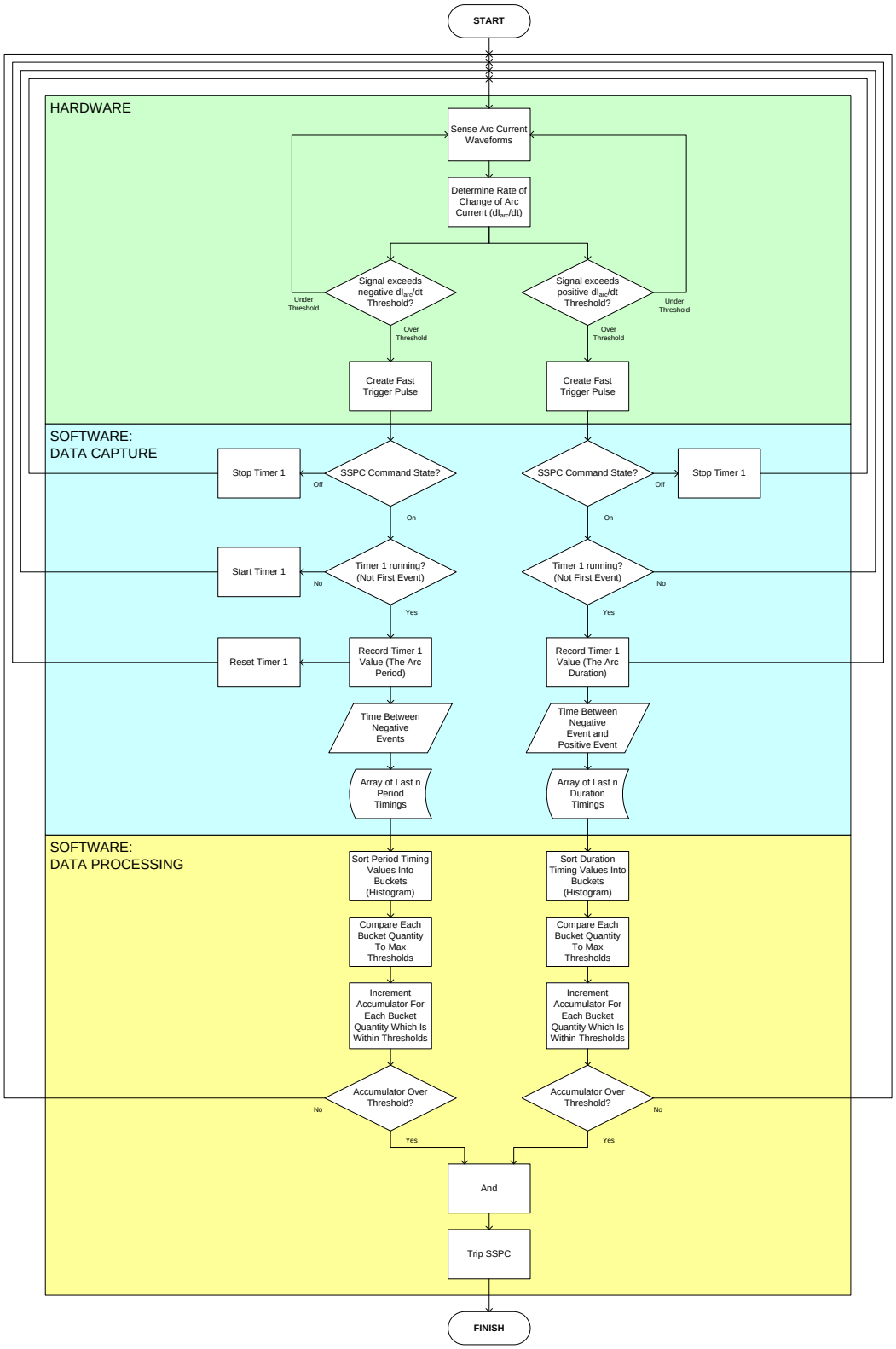


Figure C.14: PEPDC / PEPSC Statistical Software Algorithm